SGS-THOMSON MICROELECTRONICS

ST18940/41

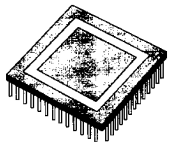
DIGITAL SIGNAL PROCESSOR

MAIN FEATURES

- 100ns MACHINE CYCLE TIME (1.2 CMOS Technology)
- PARALLEL HARVARD ARCHITECTURE
- TRIPLE DATA BUSES STRUCTURE
- 3 DATA MODES . SINGLE PRECISION
  . DOUBLE PRECISION
  . COMPLEX
- 32-BIT INSTRUCTION
- MULTIPLIER 16 x 16 —> 32, SIGNED AND UNSIGNED
- 32-BIT BARREL SHIFTER, 32-BIT ALU
- PROVISION FOR FLOATING POINT
- FOUR 32-BIT ACCUMULATORS, FOUR LEVEL 32-BIT FIFO
- IMMEDIATE AND COMPUTED BRANCH
- 8-LEVEL STACK
- 9 EXTERNAL AND 3 INTERNAL INTERRUPTS
- AUTOMATIC LOOP, UP TO 256 TIMES 32 INSTRUCTIONS
- 2 INDEPENDENT PARALLEL BUSES ; LOCAL AND SYSTEM
- FULL SPEED ACCESS TO EXTERNAL 64K x 16-BIT MEMORY ON THE LOCAL BUS
- HARDWARE AND/OR SOFTWARE WAIT STATES MODE TO ACCESS SLOWER EXTERNAL MEMORIES/PERIPHERALS, DMA CHANNEL
- 2 x 16 BYTES FIFO ON THE SYSTEM BUS
- SERIAL CHANNEL FOR DIRECT INTERFACE WITH CODEC, ISDN IC's...
- GENERAL PURPOSE PARALLEL PORT
- ON CHIP DATA RAM 2 x 256 x 16-bit
- FOUR INDEPENDENT ADDRESS CALCULATION UNITS
- ADDRESSING MODES : IMMEDIATE, DIRECT, INDIRECT WITH POST MODIFICATION, CIRCULAR, BIT REVERSED
- 2 VERSIONS : - ST18940 (PLCC/PGA 84) CLOSED VERSION WITH 3K x 32-BIT ON-CHIP PROGRAM ROM AND 512 x 16-BIT COEFFICIENT ROM
  - ST18941 (PGA 144) OPEN VERSION WITH 64K x 32-BIT OFF-CHIP PROGRAM ROM AND 128 x 16 BIT ON-CHIP COEFFICIENT RAM
- POWER DOWN MODE
- TYPICAL CONSUMPTION 0.5W

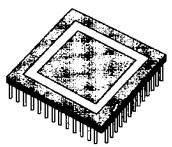
DEVELOPMENT SYSTEM

The ST18940-41 is supported by a complete set of hardware and software tools for system development. The software package includes an assembler/linker, a simulator, and a "C" compiler and optimizer which run under several VAX and PC operating systems. Hardware tools include a standalone emulator, an EPROM emulation module, a multiprocessor development station and an evaluation module (PC compatible).



ST18941 - PIN GRID ARRAY - 144-pin

ST18940 - PLASTIC LEADED CHIP CARRIER - 84-pin



ST18940 - PIN GRID ARRAY - 84-pin

DESCRIPTION

The ST18940/41 Digital Signal Processor is a member of SGS-THOMSON Microelectronics ST18 family.

The ST18 family comprises 3 products covering a wide spectrum of DSP applications. Complete development tools (hardware and software) are available as aids to efficient system designs.

The first processor in the ST18 family is the TS68930/31 (NMOS) with a 160ns machine cycle time. The second member of the family, the ST18930/31, is a CMOS version of the TS68930 with a faster instruction cycle time (80ns) and the inclusion of additional hardware and software features (The ST18930 is pin compatible with the TS68930).

The ST18940/41, which is described in this datasheet, is the third member in the family. It is upward compatible with the other members of the family, but provides enhanced arithmetic capabilities, addressing modes and additional I/O functions.

It is an advanced HCMOS single chip general purpose DSP designed for fast arithmetic intensive applications in the areas of telecommunications, modems, speech processing, graphic/image processing spectrum analysis, audio processing, digital filtering, high speed control, instrumentation, numeric processing...

The ST18940 structure is based on a triple 16-bit data bus, a 16 x 16 multiplier, a 32-bit ALU. The powerful parallel and serial Input/Output interfaces and the DMA channel contribute to the flexibility of the system interface with external environment.

Two versions are available :

- the ST18940 includes 3K x 32-bit program ROM and 512 x 16-bit coefficient ROM.
- the ST18941 microprocessor version can address up to 64K of program memory on a dedicated bus, thus providing true real-time emulation of the ST18940 ROM version. In addition to the two internal RAMs (X and Y), a 128 x 16-bit coefficient RAM is included for coefficient memory emulation.

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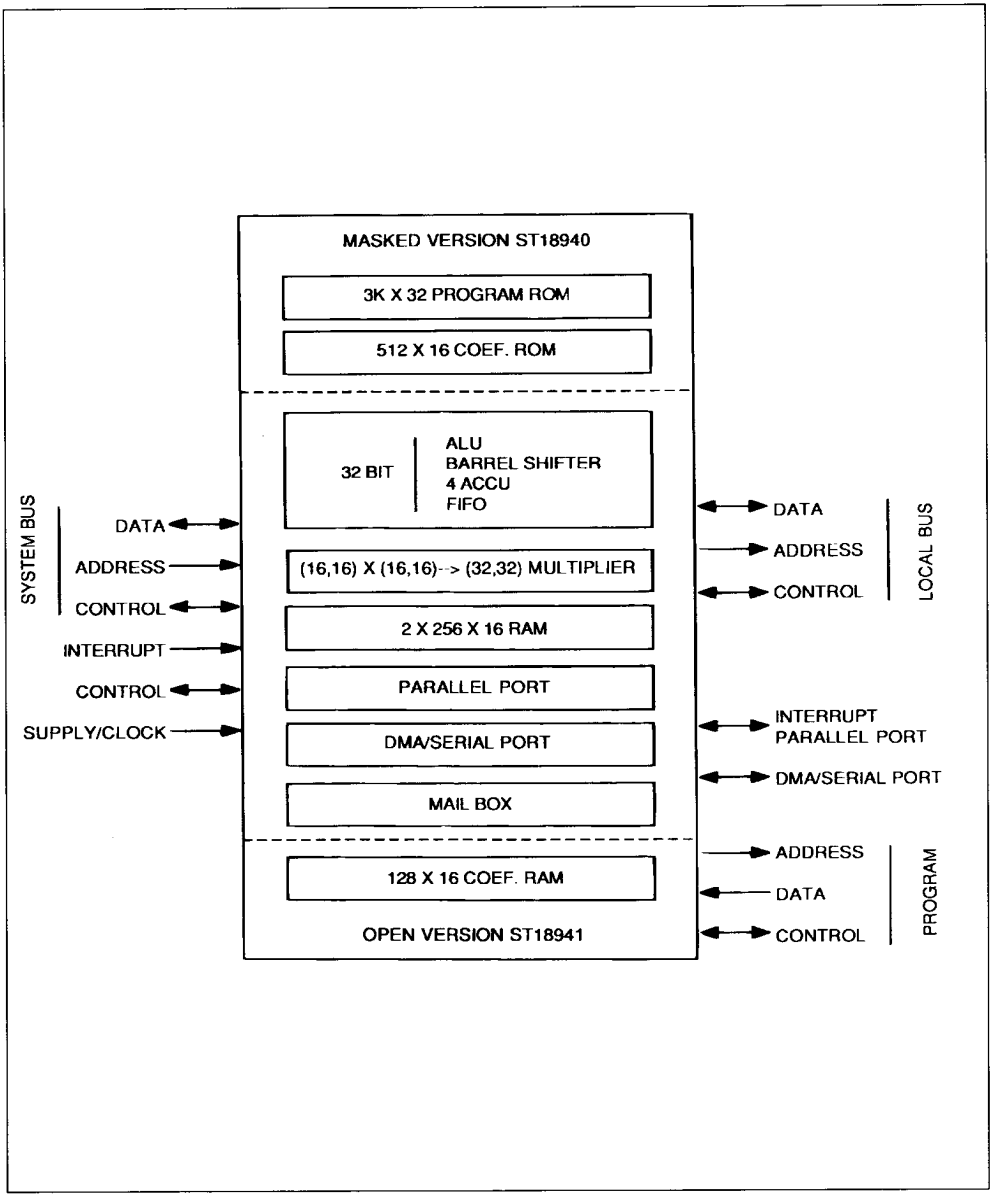
1. PIN DESCRIPTION

Figure 1 : Input/Output Pins.



1.1. LOCAL BUS

Name	Pins Type	Function	Description
D0-D15	I/O	Local Data Bus	16-Bit Data Bus. In high impedance when exchanges are not active or when RESET, HOLD, HALT or LP are active.
A0-A15	O	Local Address Bus	16-Bit Address Bus for Local Data. In high impedance when HOLD, HALT or LP are active.
DS/RD	O	Data Strobe/read	Synchronizes the transfer on local bus/read cycle.
R/W / WR	O	Read/write/write	Indicates the current bus cycle state/write cycle.
DTACK	I	Data Transfer Acknowledge	Indicates exchange acknowledgement.
BR	O	Bus Request	Active at each exchange on the local bus. In combination with DTACK, can be used to address resources shared by several processors.
HOLD	I	Hold Data	Used to free local bus in shared memory application. To HALT state if an access is attempted.
HOLDACK	O	Hold Acknowledge	Indicates that the processor is in hold state.

1.2. SYSTEM BUS

Name	Pins Type	Function	Description
SD0-SD7	I/O	System Data Bus	8-Bit data bus used for exchanges between the processor and a host via the mailbox.
CS	I	Chip Select	Selection of the system bus interface.
RS	I	Register Select	Address to select data FIFO or status register (MBS).
SDS/SRD	I	Data Strobe/read	Synchronizes the transfer on the system bus/read cycle.
SR/W/SWR	I	Read/write/write	Indicates the current system bus cycle/write cycle.
SDTACK	O	System Data Transfer Acknowledge	Indicates data exchange is acknowledged. Open drain.
IRQ	O	Interrupt Request	Signal sent to the host to signal readiness for mailbox data exchange.

1.3 DMA/SERIAL I/O INTERFACE : DUAL PURPOSE INTERFACE

Internally the DMA channel and serial I/O are implemented as fully independent separate blocks, although externally they are share 4 dual purpose I/O pins.

- DMA CHANNEL

Name	Pins Type	Function	Description
DMARQ	I	DMA Request	Activated by the device requesting the DMA. Can be a pulse ("single" mode) or a level ("burst" mode) (DPI0).
DMACK	O	DMA Acknowledge	Indicates that the request for DMA is acknowledged (DPI1).
DMAEND	O	DMA End	Indicates the end of the DMA exchange. Active as long as the channel is not reinitialized (DPI2).
DSDMA	O	Data Strobe DMA	Synchronizes the DMA exchange (DPI3).

- SERIAL INPUT/OUTPUT INTERFACE

Name	Pins Type	Function	Description
FSR	I/O	Frame Synchronization Receive	Synchronizes the receive. Can be generated or received by the processor (DPI0).
BCLKR	I/O	Bit Clock Receive	Receive bit clock. Can be generated or received by the processor (DPI1).
DA	I/O	Data A	Input or Output of Data A (DPI2).
DB	I/O	Data B	Input or Output of Data B (DPI3).
FSX	I/O	Frame Synchronization Transmit	Synchronizes the transmit. Can be generated or received by the processor (DPI4).
BCLKX	I/O	Bit Clock Transmit	Transmit bit clock. Can be generated or received by the processor (DPI5).

Note : $\overline{\text{DMARQ}}$/FSR, $\overline{\text{DMACK}}$/BCKLR, $\overline{\text{DMAEND}}$/DA, $\overline{\text{DSDMA}}$/DB are multiplexed.

1.4 PARRALLEL/INTERRUPT INTERFACE

This 8-bit port can be configured either as an interrupt controller or as a parallel input/output port.

- INTERRUPT CONTROLLER

Name	Pins Type	Function	Description
P0-P3	I	Maskable Interrupt Request	A negative transition on these input pins will initiate an interrupt sequence.
P4-P7	I	Maskable Interrupt Request	A low level on these input pins will initiate an interrupt sequence.

- PARALLEL INTERFACE

Name	Pins Type	Function	Description
P0-P7	I/O	Parallel Port	8-Bit parallel port with each bit programmable individually as input or output. Can be used as test conditions in branch instructions; four bits are edge sensitive, four are level sensitive.

1.5. POWER SUPPLY - CLOCK

Name	Pins Type	Function	Description
XTAL	O	Crystal Output	Internal oscillator output for crystal. Not connected if the internal oscillator is not used.
EXTAL/ CLKIN	I	Crystal Input	Internal oscillator input. External clock input, when the internal oscillator is not used. Oscillator frequency is twice the machine frequency.
CLKOUT	O	Clock Out	Internal clock output (oscillator frequency ÷ 2).
V_{CC}		5 Volts	Power Supply.
V_{SS}		Ground	Connected to Ground.

1.6. OTHER PINS

Name	Pins Type	Function	Description
$\overline{INT}$	I	Interrupt	Maskable interrupt request. Active Low
$\overline{RESET}$	I	Reset	Program counter is loaded with Hex. 0 and a NOP instruction is executed. Clock generator is resynchronized.
LP	I	Low Power	Stops the processor at the end of the current cycle, forces the NOP instruction and puts the processor in the powerdown mode. The internal processor state is conserved.
HT2	O	Clock	Reserved for test.

1.7. SPECIFIC PINS TO THE 18941 (open version)

Name	Pins Type	Function	Description
IA0-IA15	O	Instruction Address Bus	16-Bit address bus for external program memory. In high impedance if HALT is active or during a DMA exchange.
ID0-ID31	I	Instruction Data Bus	32-Bit data bus from external program memory.
$\overline{NMI}$	I	Non Maskable Interrupt	Interrupt input edge sensitive. Program counter is loaded with Hex. A.
$\overline{HALT}$	I	Halt	Stops the processor at the end of the current instruction. Local bus and instruction address buses are in high impedance.
$\overline{ECR}$	O	Enable CROM	Indicates that the A0-A8 addresses are used for the external emulation of the CROM.
INCYCLE	O	Instruction Clock	A falling edge indicates the start of a new instruction cycle.

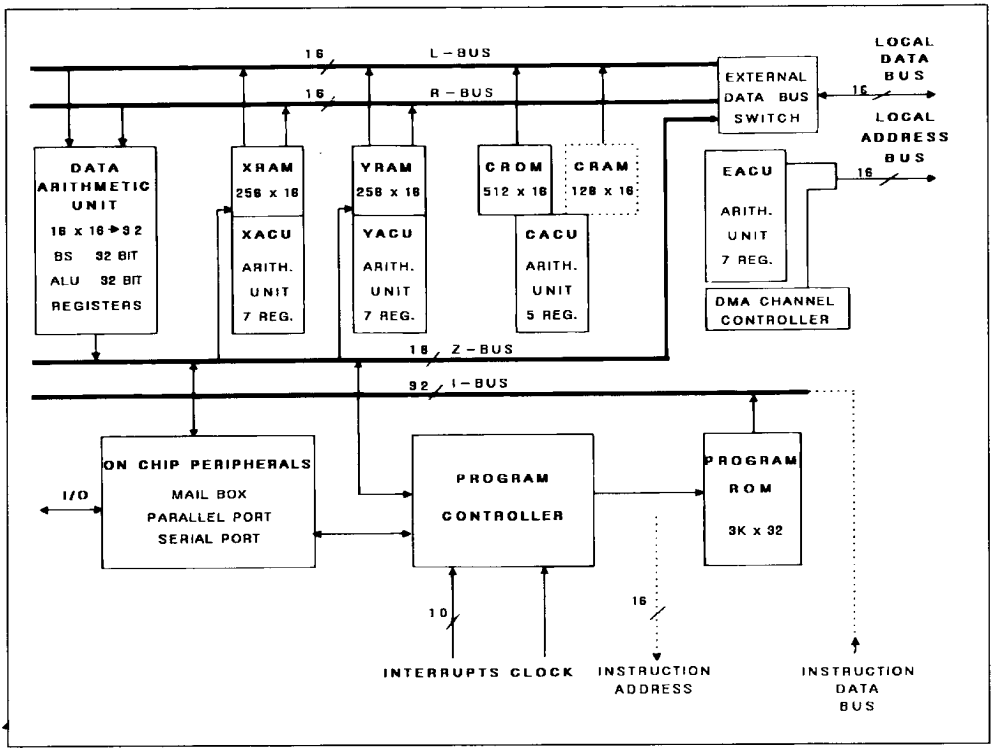
2. ARCHITECTURE

The architecture is HARVARD like with separate instruction bus and data buses. The block diagram shows four main blocks (see fig. 2) :
- the program controller
- the data arithmetic unit (ALU, multiplier and barrel shifter)
- the data storage unit
- the inputs/outputs

These four blocks can be considered as four independent processors working in parallel and communicating via three 16-bit data buses.
Within a single machine cycle the processor is able to execute all of the following operations :
- read two operands in internal or external memory
- execute a multiplication
- execute an ALU operation
- write a result to internal or external memory
- modify three address pointers
- in addition, I/O operations with on-chip peripherals may take place concurrently with internal operations.

3. BLOCK DIAGRAM

Figure 2 : ST18940/41 Block Diagram.



4. FUNCTIONAL DESCRIPTION

4.1. INTRODUCTION

One of the key features of the ST1840/41 is that all hardware resources have been designed to support the following three data types :

- simple precision : 16-bit data
- double precision : 32-bit data
- complex : 16-bit real and 16-bit imaginary

Any one of the above three arithmetic modes can be dynamically selected by means of a single program instruction. Once the mode has been selected, all resources (such as ALU, memories, registers, multiplier) are automatically configured for the appropriate operations. The same assembler instructions are used in all three modes. In double-precision and complex modes the data are stored in two contiguous memory locations, with an automatic adjustment of the address calculation unit. Two's complement representation is used throughout. In real mode, all instructions except branch are executed in one cycle time. In complex and double precision modes, all instructions are executed in two cycle times.

4.2. PROGRAM CONTROLLER

4.2.1. PROGRAM CONTROLLER (see figure 3). The purpose of the program controller is to generate the next instruction address to be executed, this instruction being in external memory for the ST18941 (64K word of 32-bit) or in the masked ROM for the ST18940 (3K word of 32-bit). The program controller takes into account the current mode to execute the instruction ; one cycle per instruction in

real mode, two cycles per instruction in double precision and complex mode. The HALT, HOLD, LP and the "WAIT STATES" suspend the sequencer cycle.

Exceptions in linear program address generation are the following :

- Execution of a branch instruction
- Call and return of a subroutine
- Execution of an interrupt routine : 2 types of hardware interrupt sources are possible : external interrupt [INT + P PORT + NMI (ST18941 only)], internal interrupt (Mailbox, serial port). The EI register enables or disables these interrupt sources.
- An 8-level stack is used to save and restore the PC in case of interrupts or subroutines.
- Loop execution : Automatic loop execution is possible by means of the loop register. This register defines the number of loops to be executed (max. 256), and the number of instructions in the loop (max. 32).

Programming model for loop execution

LOOP : Loop Register

It is used to automatically control the execution of a loop. This 16-bit register is divided in to 3 fields, LCI, LCR, LCD.

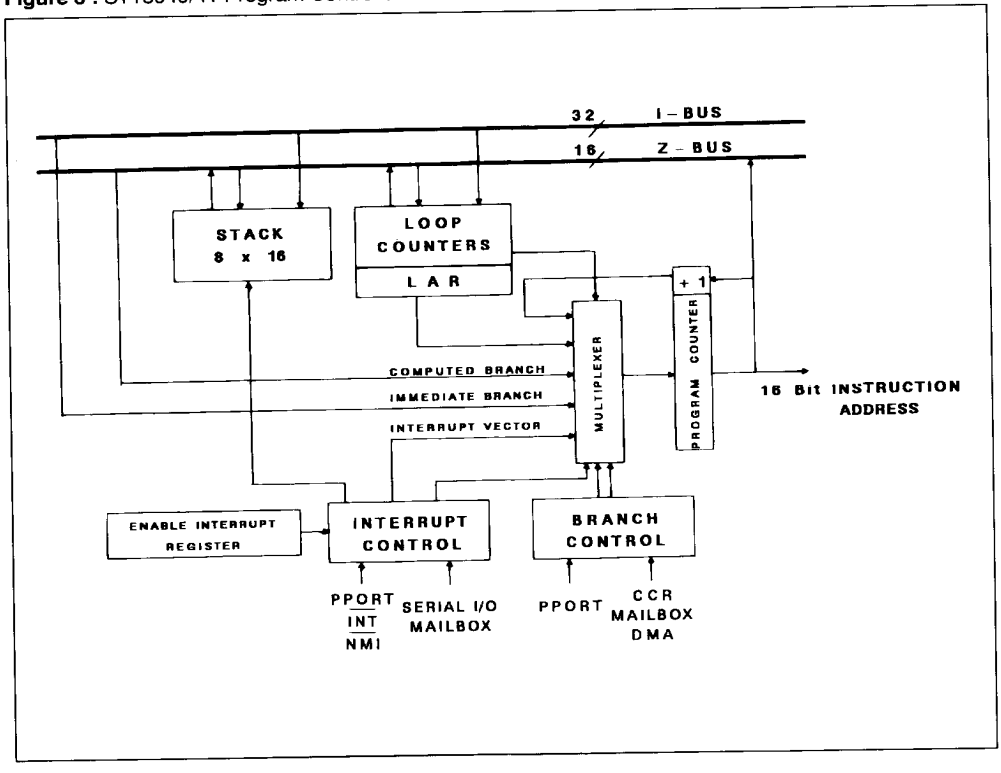
LCI (Loop Count Instruction) defines the number of instructions to be executed in a loop ; the maximum is 32 (5-bit).

LCR (Loop Count Register) defines the repeat count of the loop ; the maximum is 256 (8-bit).

LCD (Delay) defines, in terms of the number of instructions, the delay between the loop declaration and the beginning of the loop execution. The maximum is 7 (3-bit).

This "repeat of instruction blocks" feature provides code compaction and time efficient execution for vector and array processing frequently used in DSP algorithms. It is set at the macroassembler level by using a simple REPE-BEGIN-END construct.

Figure 3 : ST18940/41 Program Controller.



4.2.2. INTERRUPT CONTROL

* There are two types of hardware interrupt sources on the ST18940/41 : internal and external.

-The internal sources include chip peripheral devices : Mailbox (input/output)

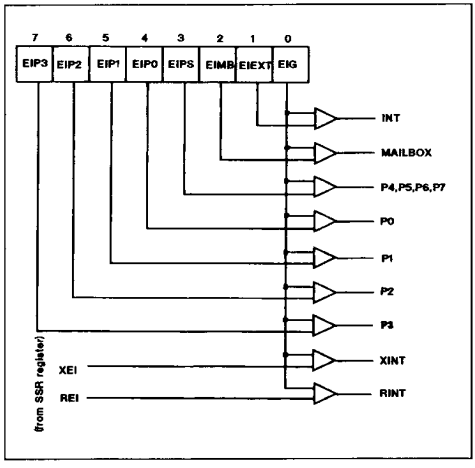
Serial port (1 for transmit, 1 for Receive)

-The external interrupts include $\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{NMI}}$ (ST18941 only) and the P Port (8 pins)

$\overline{\text{RESET}}$, $\overline{\text{INT}}$, $\overline{\text{P4}}$, P5, P6, P7 are low level sensitive interrupts and $\overline{\text{NMI}}$, P0, P1, P2, P3 are falling edge sensitive.

* The EI (enable interrupt) register is an 8-bit wide enable interrupt register. It controls the following interrupt sources : Mailbox, INT, P Port (see figure 4).

Figure 4 : ST18940/41 Enable Interrupt Register XEI, REI part of SSR Register (see page 21).



* Software interrupt can be implemented using P-Port.

* When an interrupt is acknowledged, the current program counter is pushed on the stack and the interrupt vector corresponding to the interrupt source (see table 1) is loaded into the program counter (PC). Upon completion of interrupt routine, a RTI (return from interrupt) instruction is processed. The content of the top location in the stack is popped into the PC.

Table 1 : Interrupt Vectors.

Address	Interrupt Sources
0	$\overline{\text{RESET}}$
1	$\overline{\text{INT}}$
2	R INT (serial I/O receive)
3	X INT (serial I/O Transmit)
4	B INT (mailbox)
5	P4, P5, P6, P7
6	P0
7	P1
8	P2
9	$\overline{\text{P3}}$
10	$\overline{\text{NMI}}$ (ST18941 only)

4.3. DATA ARITHMETIC UNIT (figure 5)

One of the most useful features of the ST18940-41 is to provide the user with three operating modes which can be dynamically set by software.

These three modes represent different data types :

-REAL 16-bit data

-Complex (CPLX) 16-bit real + 16-bit imaginary data

-Double-precision (DBPR) 32-bit data.

In double precision mode, data moves from and to memories are performed on 32 bits. This is especially useful in adaptive processing to keep track of L.S.B. updated coefficients.

Thus the DSP is seen by the user as a standard 16-bit real or complex machine or a 32-bit real machine. All operating units are automatically adjusted by the processor to the right length.

In all modes, the number representation used is signed 2's complement.

4.3.1. MULTIPLIER. In real and double-precision modes, the multiplier executes a 16x16-bit —> 32-bit signed or unsigned multiplication every instruction cycle.

-The operands are loaded into the M and N registers and the result of a previous multiplication is written in the P register during the same cycle.

-In complex mode the multiplier executes a complex multiplication every instruction cycle (2 x machine cycles) ie :

(a + jb) x (c + jd) = (ac - bd) + j(ad + bc).
In this case the registers M and N are 2 x 16-bit and the P register is 2 x 32-bit.

-The pipeline structure makes the multiplication result available 2 instruction cycles later in all 3 modes. The status bits relating to the multiplier are in STA (Status register) and the multiplier overflow (complex mode only) is updated in the Code Condition Register.

4.3.2. 32-Bit ALU/ACCUMULATOR. The 32-bit ALU is loaded on the right side by the R bus, by the RBD register or by the accumulators (A, B). On the left side, the operands always access the ALU through the barrel shifter, coming either from the L (left) bus or from the multiplier output register P.

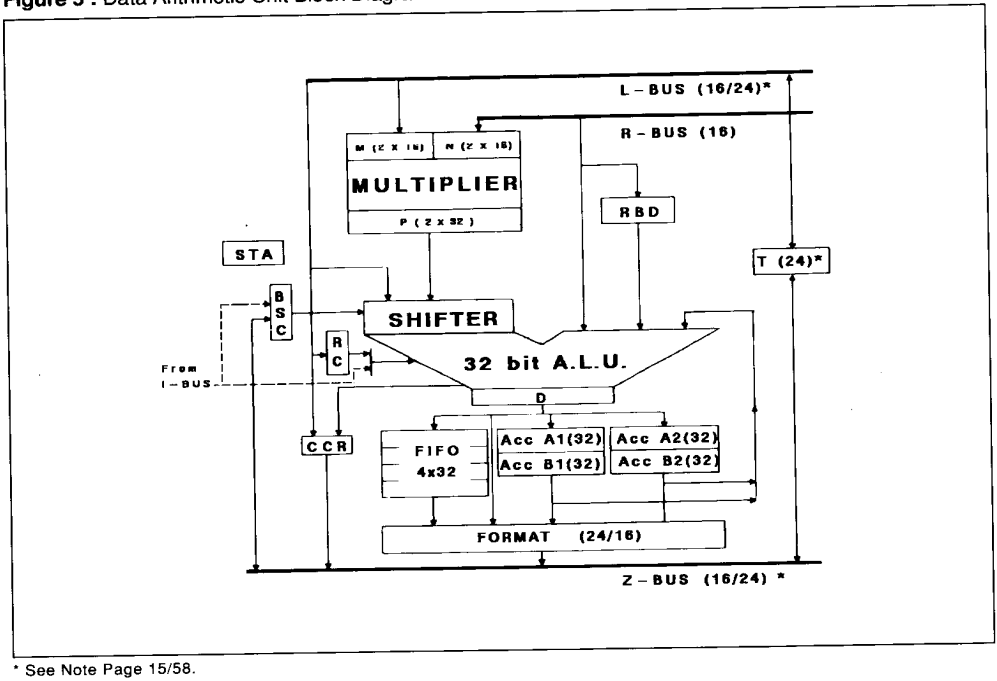
The result of an ALU operation is automatically written in the D register and, if required, into the accumulators or FIFO.

The ALU performs 32 different operations. These include the usual arithmetic, logical and shift operations e.g. ADD, SUB and AND. Additional special operations are also implemented. These include ADDS or SUBS (addition and subtraction with automatic prescaling of the left-side ALU input), and ABSolute value and EDGE operations (used for first significant bit detection and exponent adjustment).

The complete list of ALU codes and description is given in table 2 - p 27.

4.3.3. BARREL SHIFTER. The 32-bit barrel shifter located on the left side of the ALU performs all logic/arithmetic shifts and rotations. The shift value comes from the ALU code or from the BSC (Barrel Shift Control) register loaded by the Z bus. This feature combined with EDGE (Alu Code) allows easy, efficient and dynamic normalization used in floating point and dynamic scaling operations.

Figure 5 : Data Arithmetic Unit Block Diagram.



* See Note Page 15/58.

4.3.4. PROGRAMMING MODEL

Name	Function	Description
M	16 - Bit Register 2x16 - Bit (complex mode)	Left side operand of multiplier loaded via L bus.
N	16 - Bit Register 2x16 - Bit (complex mode)	Right side operand of multiplier loaded via R bus.
P	32 - Bit Register 2x32 - Bit Register (complex)	Multiplication Result
D	32 - Bit Register	ALU Result .
A1, A2	2x32 - Bit Registers	Accumulators A1 and A2 are selected by ACS bit 2 of STA register in real and double precision modes.
B1, B2	2x32 - Bit Registers	Accumulators B1 and B2 are selected by ACS bit 2 of STA register in real and double precision modes.
FIFO	4x32 - Bit Registers	FIFO loaded by ALU.
T	2x24 - Bit Registers	Bidirectional register between L bus and Z bus.
RBD	2x16 - Bit Registers	Right bus delay, this register is used as a buffer on the ALU right side.
STA	16 - Bit Register	Status register defining the state of the data arithmetic unit.
CCR	16 - Bit Register	Condition code register containing the flags generated by the data arithmetic unit. Every bit can be tested as a branch condition.
RC	7 - Bit Register	This register, directly connected to the ALU control unit, can be dynamically loaded by the L bus.
BSC	5 - Bit Register	Barrel shift control register is loaded by the Z bus and contains the shift value for the barrel shifter.

CONDITION CODE REGISTER (CCR)

Name	Bit #	Function	Description
SR	15	Sign Real	Set if the MSB of the ALU result is 1. Cleared Otherwise.
SI	14	Sign Imaginary	Set if the MSB of the ALU imaginary result is 1 (in complex mode). Cleared Otherwise.
CR	13	Carry Real	Set if carry is generated out of the MSB of the result for arithmetic and shift operations. Cleared Otherwise.
CI	12	Carry Imaginary	Set if a carry is generated out of the MSB of the imaginary part of the result for complex arithmetic and shift operations. Cleared Otherwise.
Z	11	Zero	Set if the ALU result equals zero. In complex mode it is set if both real and imaginary parts are equal to zero.
OVF	10	Overflow	Set if an arithmetic overflow occurs. This implies that the result cannot be represented in the operand size. In complex mode it is set for an overflow of either the real or imaginary part. Cleared Otherwise.
MOVF	09	Memorized Overflow	Set under the same conditions as overflow. Cleared when tested by a branch instruction.
AOVF	08	Advanced Overflow	Exclusive OR of bits 30 and 31 of the ALU. Set and memorized if arithmetic overflow occurs on half capacity. Cleared when tested by a branch instruction.
OVFM	07	Overflow Multiplier	Set and memorized if the multiplier has overflowed in complex mode. Cleared by LCCR ALU instruction.
EF	06	Empty FIFO	Set if FIFO is empty. Cleared Otherwise.
	05→00		Reserved

STATUS REGISTER (STA)

Name	Bit #	Function	Description
EPI	15	Enable Imaginary Product	Imaginary product enable under interrupt.
EPR	14	Enable Real Product	Real product enable under interrupt.
SE	13	Smallest Exponent	Conditional Load of BSC
	12	Reserved	
	11	Reserved	
	10	Reserved	
MODE	09/08		Real /CPLX/DBPR
EMI	07	Enable Multiplier Input	Multiplier enable under interrupt.
TCM	06	Two's Complement M	M signed/unsigned.
TCN	05	Two's Complement N	N signed/unsigned.
CPR	04	Conjugate Product Result	M x N conjugate.
SAT	03	SATuration	ALU Saturation
ACS	02	ACcumultator Selection	A1 or A2 and B1 or B2
FORM	01	FORMat * see note 1.	24 MSB/16 LSB Selection
RBDS	00	Right Bus Delay Selection	RBD Register Selection

Note : The data buses and the T register are 24 bits wide enabling 24-bit wide ALU results to be fed back to the left ALU input.

4.4. DATA STORAGE UNIT (figure 6)

The ST18940/41 provides four different data memories within two categories : the data memories and the coefficient memory. The coefficient memory in the ST18940 is a 512 x 16-bit masked ROM (CROM). For emulation of the ST18940 CROM, a 128x16 internal CRAM is provided in addition to the external 512x16 CRAM. Internal CRAM is usefull when coefficients are to be used in conjunction with external data in the same instruction. For both versions the internal data memories consist of two 256x16 bit RAM's denoted XRAM and YRAM. The external addressing space is of size 64k x 16-bit (ERAM) and is accessible via the local bus using a single instruction as for the internal memories.

Each memory is controlled by a dedicated Address Calculation Unit called XACU for the XRAM, YACU for the YRAM, CACU for the CRAM or CROM and EACU for the ERAM.

4.4.1. ADDRESSING MODES. The addresses are generated by each ACU according to the four addressing modes :

- Immediate addressing :
the data is in the instruction
- Direct addressing :
the address is in the instruction
- Indirect addressing :
the address is in one of the ACU registers
- Circular addressing :
also called virtual shift mode
Bit reversed mode

4.4.2. ADDRESS CALCULATION UNITS (ACU). The dedicated ACU's are independent and contain 7 registers : two banks of dual pointers selected by a bit in the ASTA register, one current pointer used in the circular addressing mode, and, two post-incrementing/decrementing registers. The register structure of XACU is given below :

X0A, X1A : dual pointer bank A

X0B, X1B : dual pointer bank B

X2 : current pointer in circular addressing

K, L : two post-incrementing/decrementing registers

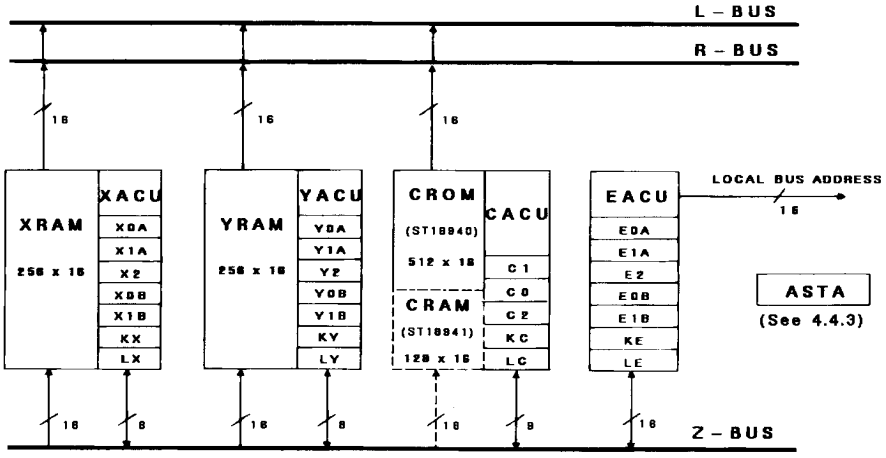
The CACU is the only ACU with a single pointer bank.

The circular addressing mode uses the A bank pointer for the minimum and maximum limits and the current pointer for the current address.

Each ACU (with the exception of CACU) supports bit reversed addressing as required for the FFT algorithms.

For the external data memory in direct addressing mode, the 16-bit address is obtained by concatenating the 13 bits contained in the instruction (LSB) to the 3 bits of the page register (MSB).

Figure 6 : ST18940/41 - Data Memories Block Diagram.



---: ST18941 ONLY

4.4.3. ASTA REGISTER - ADDRESS STATUS REGISTER

Name	Bit #	Function	Description
RBX	15	Register Bank Selection RAMX	Select Bank A or B for X, Y or ERAM
RBY	14	Register Bank Selection RAMY	
RBE	13	Register Bank Selection ERAM	
	12		Reserved.
EC	11	External Coefficient	ST18941 only, Internal or External CRAM Selection
BRX	10	Bit reversed RAMX.	Set bit reversed mode.
BRY	09	Bit reversed RAMY.	
BRE	08	Bit reversed ERAM.	
X_C	07	Circular RAMX	Set circular addressing mode.
Y_C	06	Circular RAMY	
E_C	05	Circular ERAM	
C_C	04	Circular CROM	
ADOFX	03	ADOF RAMX	Force the 1st address in complex or double. Precision mode to be odd or even.
ADOFY	02	ADOF RAMY	
ADOFE	01	ADOF ERAM	
ADOFC	00	ADOF CROM	

4.5. INPUT/OUTPUT

The ST18940/41 provides four I/O interfaces :

-the system bus
-the local bus
-the parallel port
-the serial interface

4.5.1. THE SYSTEM BUS. For asynchronous exchanges between the ST18940/41 and a host (general purpose MCU and/or other ST18940/41 processors), the ST18940/41 is provided with a "mailbox mechanism" comprising a double 16-byte FIFO, one for input (RIN), one for output (ROUT).

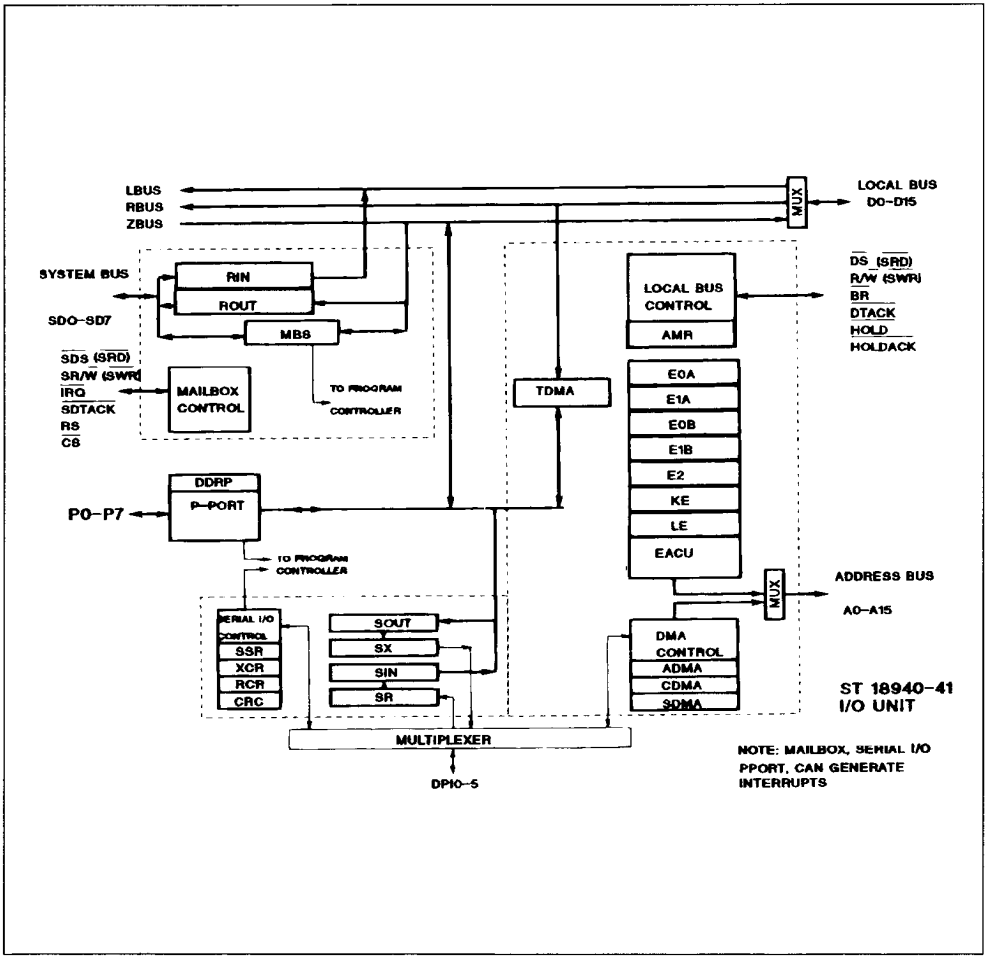
A 6-bit status register MBS is accessible to both the ST18940/41 and the host. Internally RIN is connected to the L bus and ROUT to the Z bus. Externally SD0-SD7 gives access to RIN and ROUT.

The $\overline{CS}$ input selects the mail box (RIN, ROUT, MBS) in the host system addressing space while the RS input selects RIN-ROUT or MBS. The (SR/W, SWR) and ($\overline{SDS}$, $\overline{SRD}$) inputs synchronize and control the exchanges on the system bus. These signals are programmable (AMR bit 7) in order to be directly compatible with MOTOROLA or INTEL hosts.

MBS REGISTER : MAILBOX STATUS REGISTER (6-BIT - R/W)

Name	Bit #	Function	Description
RIE	5	Register Input Empty	Input FIFO Empty
RIF	4	Register Input Full	Input FIFO Full
RISH	3	Register Input DSP/host	Input to processor/host indicates to which input mailbox belongs to.
ROE	2	Register Output Empty	Output FIFO Empty
ROF	1	Register Output Full	Output FIFO Full
ROSH	0	Register Output DSP/host	Output to processor/host indicates to which mailbox belongs to.

Figure 7 : Input/output Functions.



4.5.2. LOCAL BUS. On this 16-bit bus (16-bit data, 16-bit address) the ST18940/41 can access external memories or peripherals. To access slow devices, the DSP can stretch its external memory cycle by the insertion of wait states. This can be achieved using either of the two following methods :

-Hardware mechanism : the external memory or peripherals generates a DTACK pulse to signal the end of the exchange

-Programmable multicycle exchanges : the exchange lasts for the number of cycles programmed by the ES0 and ES1 bits of the Access Mode Register. Easy implementation of multiprocessor application using the local bus is allowed by mean of the HOLD function. External devices can take control of the local bus by using the HOLD and HOLDA pins.

-AMR REGISTER : ACCESS MODE REGISTER (8 - BIT, R/W)

Name	Bit #	Functions	Description
I/M	7	Intel/MOTOROLA Format System Bus	Must be set according to the host control : ($\overline{RD}$, $\overline{WR}$) or (SDS, SW/R)
MASK	6		When this bit is set, an interrupt will reset the AMR bits : ES0, ES1, DTACKEN, CSS0, CSS1 (at the end of the interrupt routine, previous AMR state is automatically restored).
DPIF	5	Dual Purpose Interface	DPI Function Selection (serial I/O or DMA)
CSS1 CSS0	4 3	Control Signal Selection	Select one of the three possible sets of control signals on the local bus.
DTACKEN	2	DTACK Enable	DTACK Validation
ES1 ES0	1 0		Exchange speed (1 to 4 cycles)

4.5.3. PARALLEL INTERFACE. The P port is a general purpose 8-bit port, where each bit is programmable as input or as output by means of the DDR 8-bit register. In addition each bit can be used as an external test condition in a branch instruction or as an interrupt source. Four bits (P0-P3) are edge sensitive and four bits (P4-P7) are level sensitive.

4.5.4. DMA CHANNEL. The DMA channel controls transparent exchanges on the local bus between internal XRAM, YRAM or ERAM and an external device.

Single and burst modes are provided. In single mode, the exchange is processed word by word and synchronized by the DMARQ signal (edge sensitive). In burst mode, the exchange is carried out on a block basis with the number of words to be transferred stored in CDMA (13-bit register). In this case the DMARQ is level sensitive and the end of the exchange is indicated by the assertion of the DMAEND signal. The DMA channel is accessed through four pins of DPI port (Dual Purpose interface) and is programmed by the three following registers :

-SDMA REGISTER : STATUS DMA (6 - BIT-R/W)

Name	Bit #	Functions	Description
DMEND	5		End of DMA
O/I	4		DMA as Input or Output
E	3		DMA with ERAM
Y	2		DMA with YRAM
X	1		DMA with XRAM
B/S	0		Burst/single Mode

ADMA Register (13-bit-R/W) : contains the DMA address

TDMA Register (16-bit-R/W) : DMA data buffer

4.5.5. SERIAL I/O. This serial port provides 2 bidirectional lines DA and DB programmable as input or output to give access to the receive or to the transmit part of the port.

Four pins are dedicated to clock and synchronization :

-BCLKX and BCLKR : Transmit and Receive Clocks Frequency equals to single or double the data rate.

-FSX and FSR : Frame synchro pulse.

These four signals can be internally or externally generated.

-Transmitted and received words can be programmed to 8 or to 16 bits (XWL-RWL).

-In one frame several words can be transmitted or received. XS0-XS5 (resp. RS0-RS5) indicate the starting time slot for the transmit (resp. receive) part, XE0-XE5 (resp. RE0-RE5) indicate the ending time slot for the transmit (resp. receive) part.

-The serial port shares 4 pins with the DMA channel controller.

-Direct interfacing with serial devices (such as CODEC, ISDN...) is provided.

-SIN - Serial Input Register (8 - 16-bit - Read)

-SOUT - Serial output Register (8 - 16-bit - Write).

SSR - SERIAL STATUS REGISTER (16-bit - R/W)

Name	Bit #	Functions
XEI	15	Transmit - Interrupt Enable
XRE	14	Transmit - Interrupt (SOUT empty)
XER	13	Transmit - Underspeed Error
XEN	12	Transmit - Enable
XWL	11	Transmit - Word Length (8 or 16)
XF	10	Transmit - Frequency
XDL	09	Transmit - Delay Synchro
XCS	08	Transmit - Internal Clock
REI	07	Receive - Interrupt Enable
RRF	06	Receive - Interrupt (SIN full)
RER	05	Receive - Overspeed Error
REN	04	Receive - Enable
RWL	03	Receive - World Length (8 or 16)
RF	02	Receive - Frequency
RDL	01	Receive - Delay Synchro
RCS	00	Receive - External Clock

XCR - TRANSMIT CONTROL REGISTER (15-bit - R/W)

Name	Bit #	Functions
XZ	14	Level 1 High Impedance
XV	13	Output Buffer Enable
X A/B	12	Transmit on DA or DB
XEO-XE5	06-11	Time Slot # End of Transmit
XSO-XS5	00-05	Time Slot # Start of Transmit

RCR - RECEIVE CONTROL REGISTER (13-bit - R/W)

Name	Bit #	Functions
R A/B	12	Receive on DA or DB
REO-RE5	06-11	Time Slot # End of Receive
RSO-RS5	00-05	Time Slot # Start of Receive

CRC - CLOCK CONTROL REGISTER(16-bit - R/W)

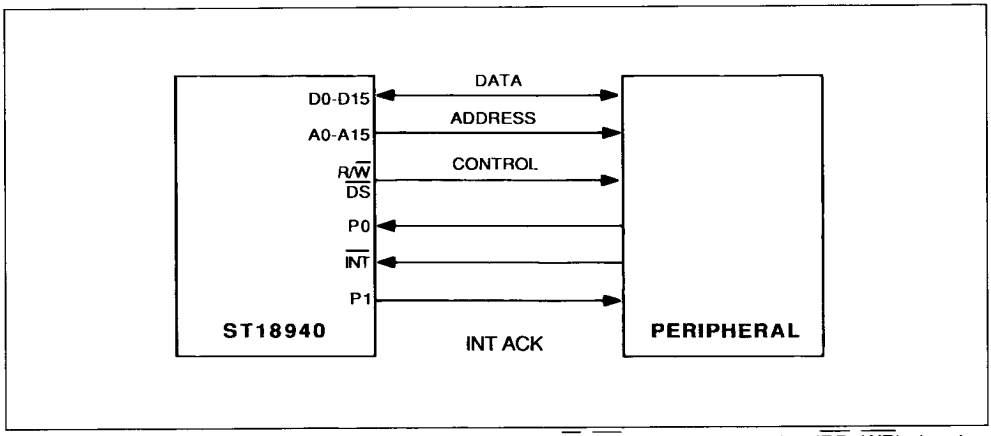
Name	Bit #	Functions
Reserved	15	Reserved
T0-T5	09-14	Frame Synchro Frequency
PSC	08	Prescaler 1/8
CDO-CD7	00-07	Internal Clock Division Range

5. SYSTEM CONFIGURATIONS

5.1. MINIMUM APPLICATION (ST18940 + peripherals)
The ST18940/41 input/output architecture has been designed to support a wide variety of peripherals types, speeds, and organizations without the use of additional circuit chips (glue chip). A minimum application consists of one processor connected to one peripheral.

The following examples show the method to interface several types of peripherals with the ST18940.

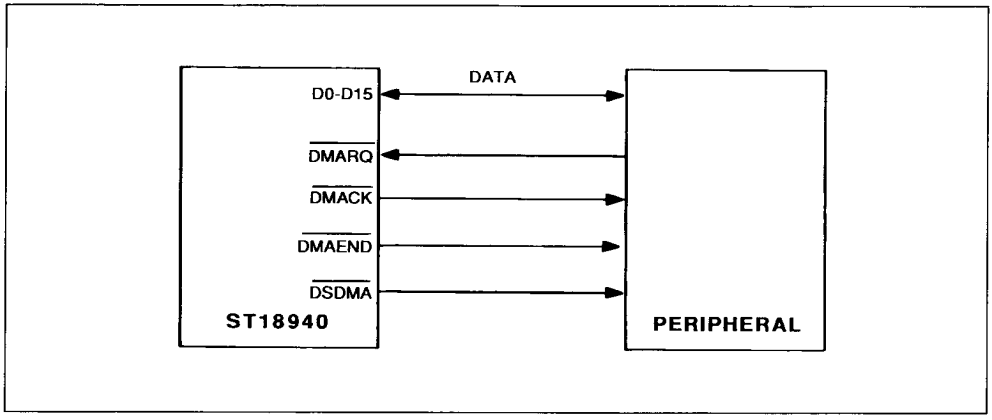
5.1.1. PERIPHERAL ON LOCAL BUS.



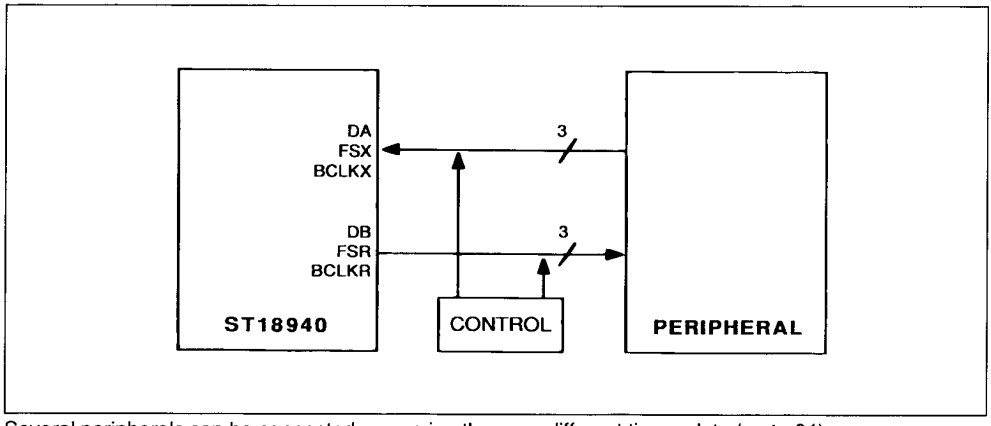
The peripheral can be A/D converter, parallel CODEC...
Exchange can be initialized by interrupt or polling (branch condition).

* (R/W, DS) can be changed to (RD, WR) signals.

5.1.2. PERIPHERAL ON DMA CHANNEL, DPI PORT.

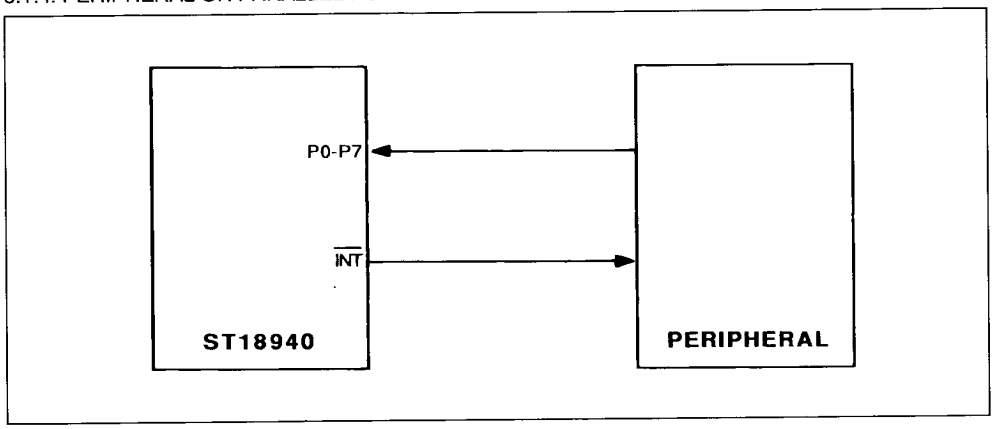


5.1.3. PERIPHERAL ON SERIAL PORT (TYPICAL APPLICATION - SERIAL CODEC)



Several peripherals can be connected, assuming they use different time - slots (up to 64)

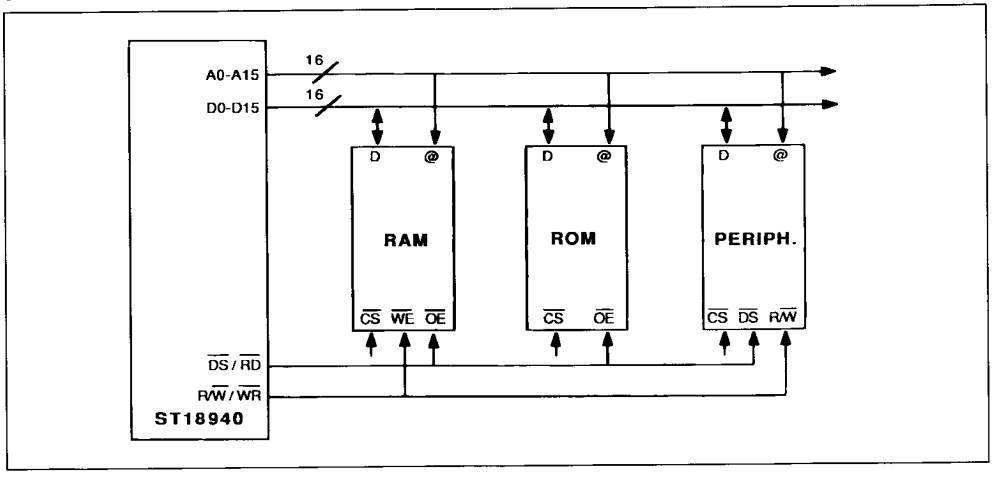
5.1.4. PERIPHERAL ON PARALLEL PORT.



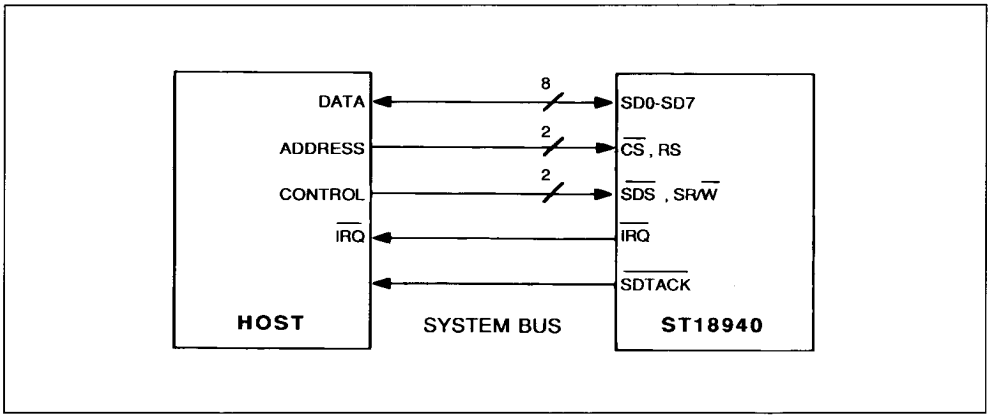
5.2. BUS EXTENSION

The external double-bus architecture is well suited for connections to memory extensions or to a host computer. The system bus/mailbox is intended for communication with other procesors while the local bus is designed for flexible straightforward memory extension interfacing.

5.2.1. EXTENSION ON LOCAL BUS.



5.2.2. HOST PROCESSOR INTERFACE ON SYSTEM BUS.

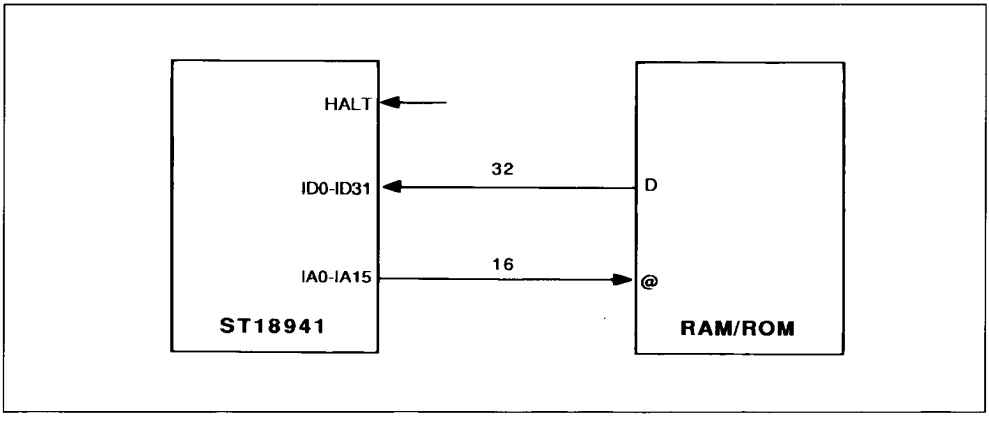


* (SDS, SR/W) can be changed to (SRS, SWR) signals.

5.3. SPECIFIC APPLICATION WITH ST18941 (ROMLESS VERSION)

The ST18941 (open version) provides a dedicated bus to access 64K x 32-bit of external program memory without any additional logical glue.

PROGRAM MEMORY INTERFACE



6. SOFTWARE

6.1. INSTRUCTION FORMAT

The instruction set is divided into 5 instruction types :

* calculation instruction	:	OPIM	with immediate addressing
		OPIN	with indirect addressing
		OPDI	with direct addressing
* shift instruction	:	SHIFT	with direct addressing
* transfer instruction	:	TFR	with direct addressing
* branch instruction	:	BRI	Immediate branch
		BRC	Computed branch
* Initialization instruction	:	PINI	Pointer initialization
		RINI	Register initialization

By virtue of the parallel architecture, each instruction controls a number of concurrent operations. The instruction format is divided into a number of fields, which can be used to specify source and destination and operation type for the 4 resources : Zbus, Lbus, Rbus and ALU.

Typical instruction format :

<instr. mnemonioc>, <Z bus field>, < bus field>, <bus field>, <ALU field>

Typical field :

<mnemonic>, and < sources>, and <destinations>

All instructions (except control instructions) are executed in 1 machine cycle (100ns) in REAL mode. All instructions are executed in 2 machine cycles (200ns) in complex and double-precision modes.

In all three modes, every instruction occupies 1 single word (32-bit) of program memory.

6.2. INSTRUCTION SET

6.2.1. ALU CODES. The ALU code is used with calculation instructions (section 6.3.2). Enhanced shift operations are available with the shift instruction (section 6.3.3).

Table 2 : List of Alu Codes.

Type	Mnemonic	Function
ADD	ADD	Addition
	ADDC	Addition with Carry
	ADDS	Addition with L side operand shifted by N bits.
	ADDX	Add the complex conjugate of L-side.
SUB	SBC	Substract with Carry
	SBCR	Reversed substract with carry (Rside - Lside).
	SUB	Substract Lside - Rside
	SUBR	Substract R side - L side
	SUBS	Substract with L side operand shifted by N bits.
LOGIC	AND	Logical AND
	COM L or R	Complement R side or L side
	XOR	Exclusive OR
	OR	Inclusive OR
SHIFT	ASL	Arithmetic Shift Left
	ASR	Arithmetic Shift Right
	LSL	Logical Shift Left
	LSLB	Logical Shift Left of 8 Positions
	LSR	Logical Shift Right
	LSRB	Logical Shift Right of 8 Positions
	ROR	Rotate
RC	RCE	Execute RC
	RCER	Execute and replace RC.
	RCR	Load RC
MISCELLANEOUS	ABS	Absolute Value
	CLR	Clear
	NOP	no Operation
	SET	Set to One
	LCCR	Load L Bus into CCR Register
	TRA L or R	Transfer operation from L side or R side.
	EDGE	Edge Transition for Binary Point Detection

6.2.2. CALCULATION INSTRUCTION. The three instruction types OPIM, OPDI, OPIN have the same structure but differ in terms of addressing mode. OPIM is for use with immediate addressing on R source operands. OPDI is for use with direct addressing on L source operands. OPIN is for use with indirect addressing on all operands. With the exception of some shift operations, the calculation instructions are the only instructions providing access to the ALU codes.

Instruction structures are given below for each class.

Detailed information is provided in the user's manual and in the programming reference card.

OPIN	Z Field		L Field		R Field		ALU Code Source Dest.
	Source	Dest.	Source	Dest.	Source	Dest.	
	(1)	Indirect	Indirect	(2)	Indirect	(2)	

Most of the typical DSP algorithms are implemented on the ST18940-41 system using OPIN class instructions.

OPDI	Z Field		L Field		R Field		ALU Code Source Dest.
	Source	Dest.	Source	Dest.	Source	Dest.	
	(1)	Indirect	Direct	(2)	Indirect	(2)	

OPIM	Z Field	L Field		R Field		ALU Code Source Dest.
	NOT AVAILABLE	Source	Dest.	Source	Dest.	
		Indirect	(2)	Value	(2)	

(1) Sources of the Z field are typically selected from the set of options : ALU output (D register), accumulators A1, B1, A2, B2 and FIFO.
(2) Destinations of the Lbus and Rbus are typically the multiplier input registers and the ALU inputs (which are not latched).

6.2.3. SHIFT INSTRUCTIONS. The shift instruction allows access to barrel shifter operations with programmable shift values.

SHIFT CODE	SHIFT VALUE	L Bus		Z Bus	
		Source	DEST.	Source	DEST.
		Direct	(2)	(1)	Indirect

6.2.4. TRANSFER INSTRUCTION. The transfer instruction TFR is used to move data through the Z bus. All internal registers can be accessed in read and write through the Z bus.

TFR	Z Bus		
	Source	DESTINATION 1	DESTINATION 2
	Register	Register	Direct

6.2.5. BRANCH INSTRUCTION. The branch address for conditional branch operations may be immediate or computed. In the latter case the new PC value may be loaded from accumulators A, B, FIFO or the T register. Twenty three conditions can be tested (Condition Code Register, mailbox and DMA flags, and PPORT).

BRANCH	Branch Conditions	Branch Address Immediate or Computed	PC Save Operations Z Bus	
			Source	DESTINATION
			PC	Indirect

The "PC save" field allows stack extension in data memory (either internal or external) with a minimum execution time overhead.

6.2.6. INITIALIZATION INSTRUCTIONS. The PINI instruction is used for pointer initialization. In addition to mode setting, PINI instruction provides initialization of 2 address pointers in one cycle.

PINI	Mode	Field 1		Field 2	
		Immediate Value	Register or Resource	Immediate Value	Register or Resource

The RINI instruction is used to initialize index address registers, DMA registers, loop counters as well as the bits of the status (STA register).

RINI	Value	Register	Register
		Dest. 1	Dest. 2

Note : Two registers cannot be initialized in the same RINI instruction. Only one register of class 1 or 2 can be initialized within a single instruction.

6.3. PROGRAMMING EXAMPLE

OPIN ST B [E0] + K ; LDL [X0] + L M ; LDR [Y0] - K N ; ADDS P A, A\

OPIN	Instruction type
ST B [E0] + K	Z field : B is stored into ERAM location addressed by E0. The next E0 value will be E0 + KE
LDL [X0] + L M	L field : XRAM location addressed by X0 is transferred via the LBUS and stored in the MULTIPLIER input M. The next X0 value will be X0 + LX
LDR [Y0] - K N	R field : YRAM location addressed by Y0 is transferred via the RBUS and stored in the MULTIPLIER input N. The next Y0 value will be Y0 - KY
ADDS PA, A	ALU field : product scaled by BARREL SHIFTER (shift value given by BSC) is added to previous value of A, result is stored into A.

7. ELECTRICAL SPECIFICATIONS

7.1. DC ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	– 0.3 to 7.0	V
V_{in}*	Input Voltage	– 0.3 to 7.0	V
T_A	Operating Temperature Range	0 to 70	°C
T_{stg}	Storage Temperature Range	– 55 to 150	°C
P_{Dmax}	Maximum Power Dissipation	0.8	W

* With respect to Vss.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

7.2. DC ELECTRICAL CHARACTERISTICS

Conditions : V_{CC} ± 10%, Ambient Temperatures = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	4.5	5	5.5	V
V_{IL}	Input Low Level	– 0.3		0.8	V
V_{IH}	Input High Level	2.4		V_{CC}+0.3	V
I_{in}	Input Leakage Current	– 10		10	µA
V_{OH}	Output High Level (I_{OH} = 300µA)	2.7			V
V_{OL}	Output Low Level (I_{OL} = 2mA)			0.5	V
P_D	Power Dissipation		0.5		W

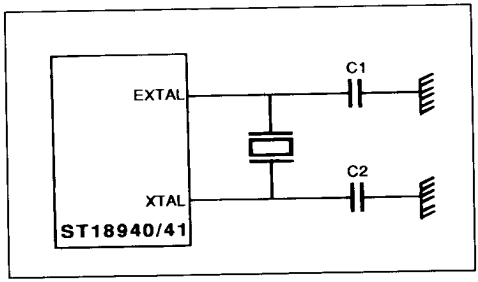
7.3. CLOCK CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_X	Frequency	5		20	Mhz
	C1, C2		10		pF

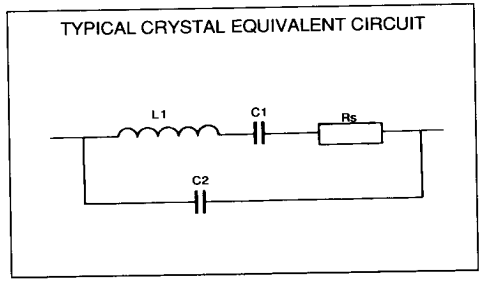
The CKLOUT frequency is half the crystal operating frequency.

INTERNAL CLOCK OPTION

A crystal can be connected across XTAL and EXTAL functioning in the parallel resonant fundamental mode, AT – cut.



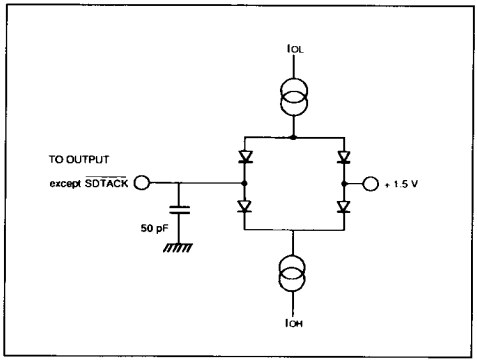
C1, C2 TYPICAL VALUE = 10 PF

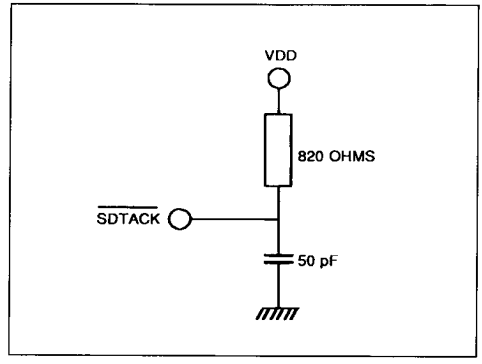


TYPICAL VALUES :
RS = 10 OHMS C2 = 4 PF
C1 = 0.02 PF Q > 30 K

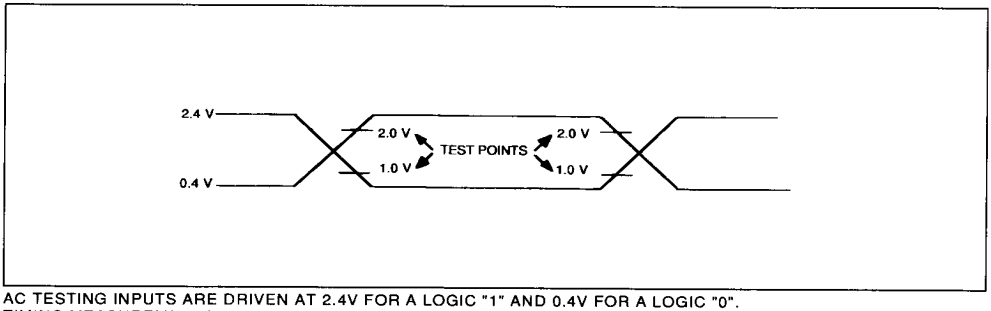
7.4. AC MEASUREMENT CONDITIONS

OUTPUT LOAD





AC TESTING INPUT, OUTPUT WAVEFORM

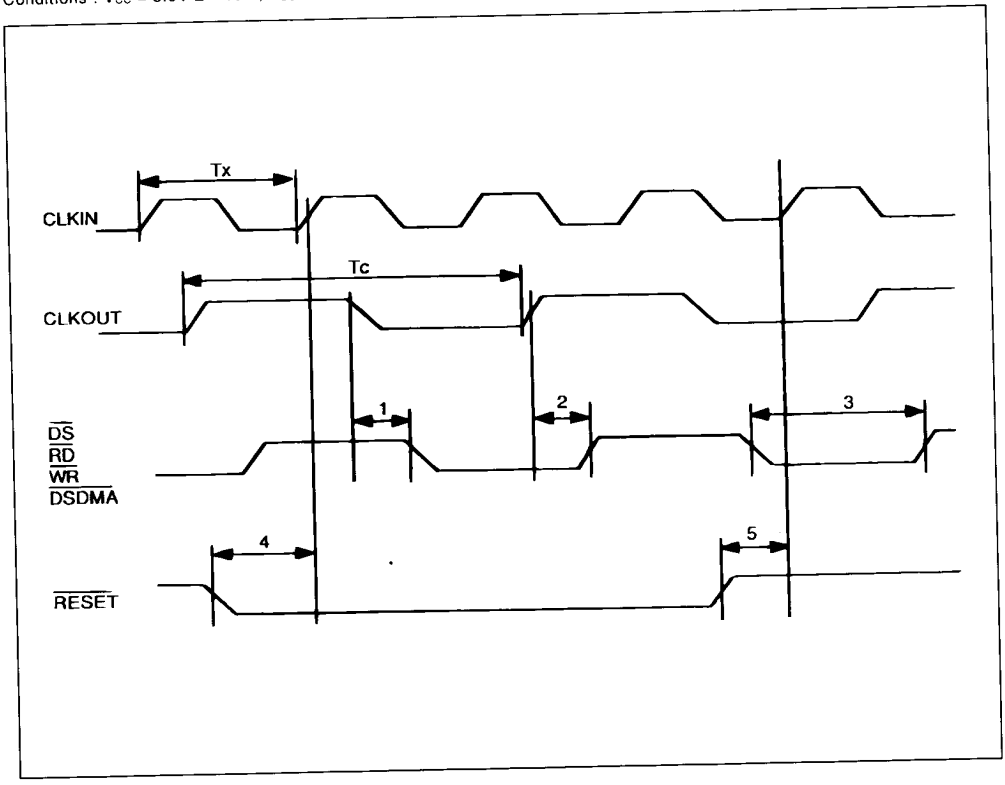


AC TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.4V FOR A LOGIC "0".
TIMING MEASUREMENTS ARE MADE AT 2V FOR A LOGIC "1" AND AT 1.0V FOR A LOGIC "0".

7.5. EXTERNAL CLOCK OPTION

Num.	Parameter	Min.	Typ.	Max.	Unit
TX	Period	50		200	ns
	Duty Cycle	40		60	%
	Rise Time			5	ns
	Fall Time			5	ns
T_C	CLKOUT Period		$2xT_X$		ns
1	$\overline{DS}$ Low to CLKOUT Delay	− 5		+ 5	ns
2	$\overline{DS}$ High to CLKOUT Delay	− 5		+ 5	ns
3	$\overline{DS}$, $\overline{RD}$, $\overline{WR}$, $\overline{DSDMA}$ Low Level		$T_C/2$		ns
4, 5	$\overline{RESET}$ Set up	15			ns

Conditions : V_{CC} = 5.0V ± − 10%, V_{SS} = 0V, T_A = 0 to 70°C.

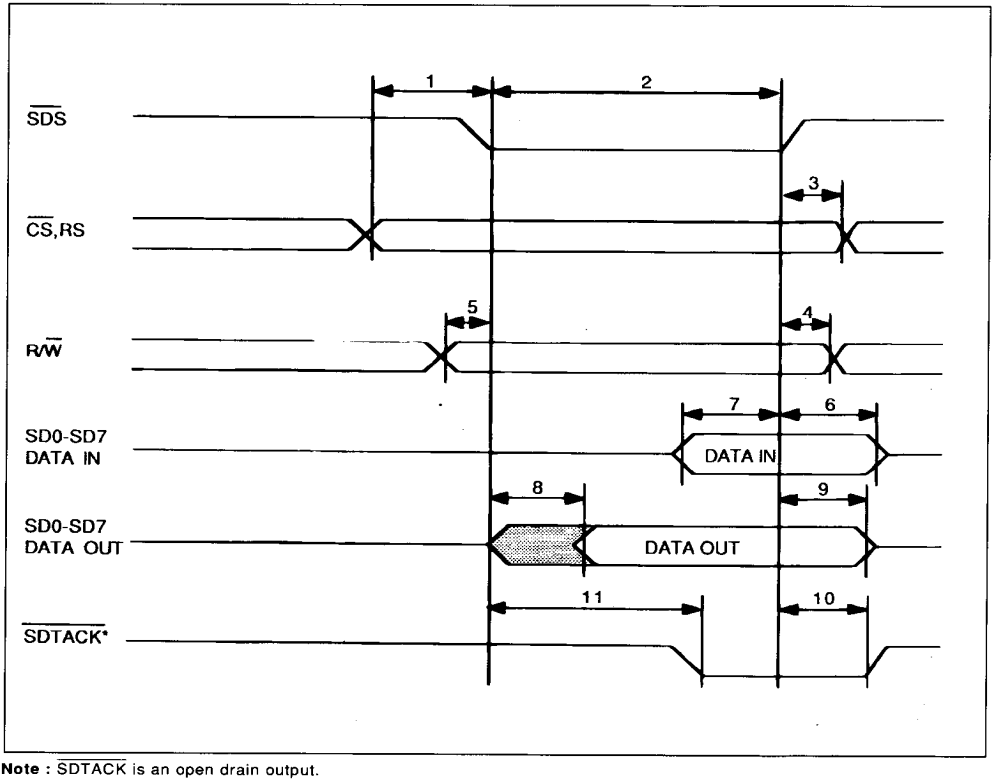


7.6. SYSTEM BUS TIMING

Num.	Parameter	Min.	Max.	Unit
2	$\overline{SDS}$, $\overline{SRD}$, $\overline{SWR}$ Pulse Width	40		ns
1	Address to $\overline{SDS}$ Setup	15		ns
3	Address to $\overline{SDS}$ Hold	5		ns
5	R/$\overline{W}$ to $\overline{SDS}$ Setup	15		ns
4	SR/$\overline{W}$ to $\overline{SDS}$ Hold	5		ns
7	Data in to $\overline{SWR}$, $\overline{SDS}$ Setup	15		ns
6	Data in to $\overline{SWR}$, $\overline{SDS}$ Hold	5		ns
8	Data out to $\overline{SRD}$, $\overline{SDS}$ Delay		25	ns
9	Data out to $\overline{SRD}$, $\overline{SDS}$ Hold	5	25	ns
11	$\overline{SDTACK}$ to $\overline{SRD}$, $\overline{SWR}$, $\overline{SDS}$ Delay		25	ns
10	$\overline{SDTACK}$ to $\overline{SRD}$, $\overline{SWR}$, $\overline{SDS}$ Hold	5	50	ns

Conditions : V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_A = 0 to 70°C.

SYSTEM BUS TIMINGS

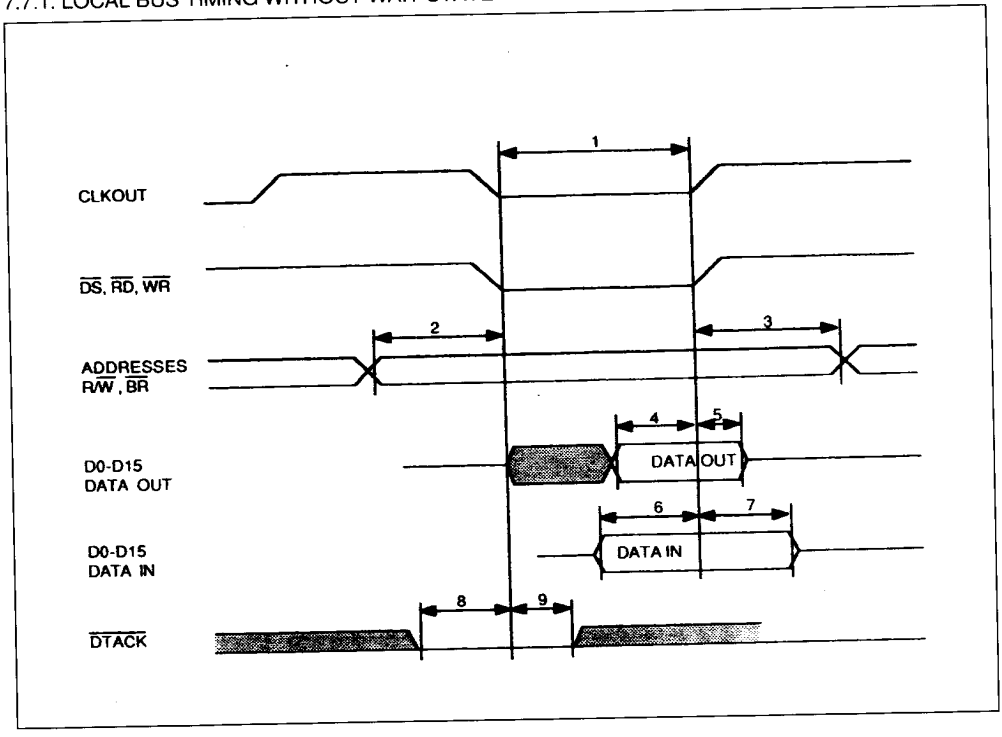


Note : $\overline{SDTACK}$ is an open drain output.

7.7. LOCAL BUS TIMING

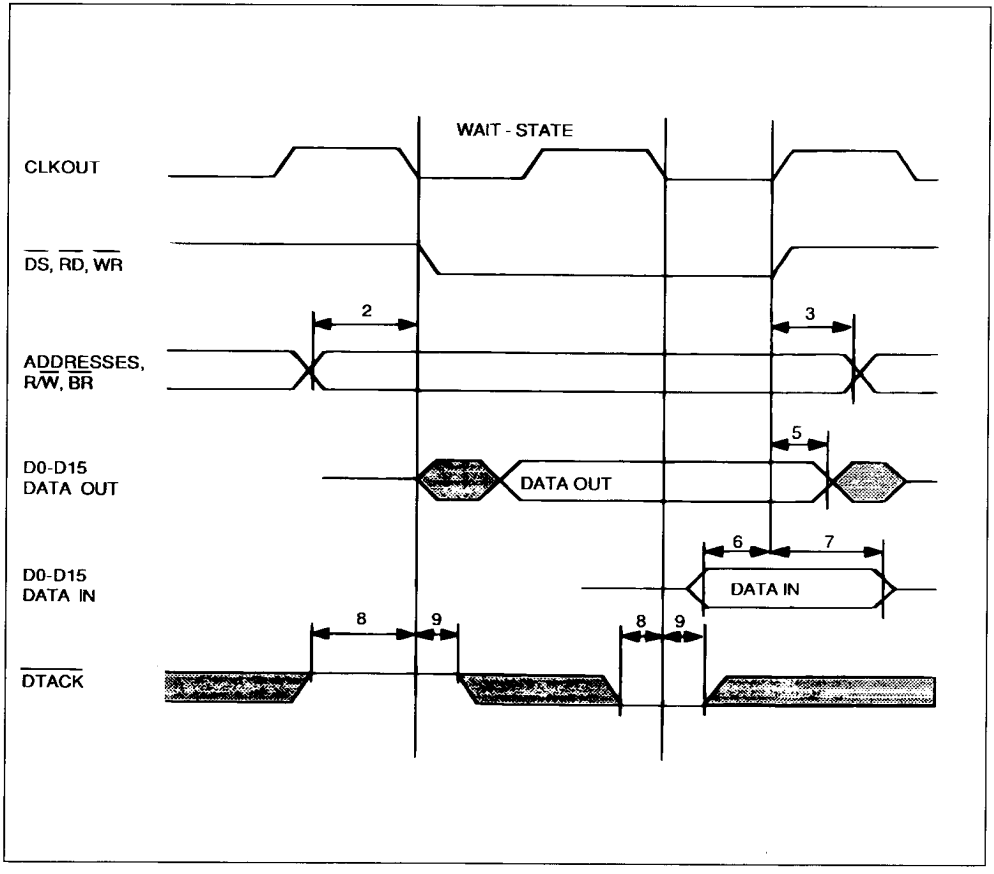
Num.	Parameter	Min.	Max.	Unit
1	$\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Pulse Width	$T_C/2$-10	$T_C/2$	ns
2	Address to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Delay	$T_C/2$-25		ns
3	Address to $\overline{DS}$, $\overline{RD}$, $\overline{WR}$ Hold	5		ns
4	DATA to $\overline{DS}$, $\overline{WR}$ Delay Write	$T_C/2$-25		ns
5	DATA to $\overline{DS}$, $\overline{WR}$ Hold Write	5	25	ns
6	DATA to $\overline{DS}$, $\overline{RD}$ Setup Read	15		ns
7	DATA to $\overline{DS}$, $\overline{RD}$ Hold Read	5		ns
8	$\overline{DTACK}$ to CLKOUT Delay	15		ns
9	$\overline{DTACK}$ to CLKOUT Hold	15		ns

7.7.1. LOCAL BUS TIMING WITHOUT WAIT STATE



SGS-THOMSON MICROELECTRONICS

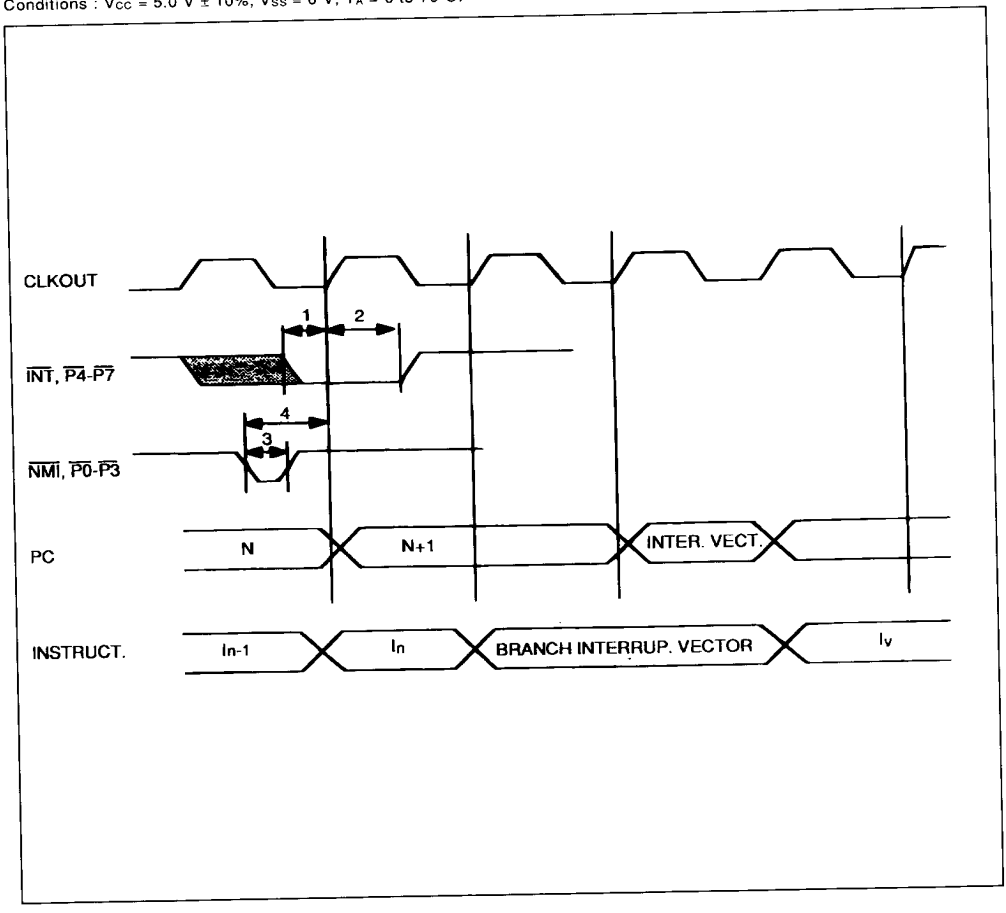
7.7.2. LOCAL BUS TIMING WITH WAIT - STATE



7.8. INTERRUPT TIMING

Num.	Parameter	Min.	Max.	Unit
1	$\overline{INT}$, $\overline{P4}$-$\overline{P7}$ to CLKOUT Setup	20		ns
2	$\overline{INT}$, $\overline{P4}$-$\overline{P7}$ to CLKOUT Hold	5		ns
4	$\overline{NMI}$, $\overline{P0}$-$\overline{P3}$ to CLKOUT Setup	15		ns
3	$\overline{NMI}$, $\overline{P0}$-$\overline{P3}$ to CLKOUT Hold	10		ns

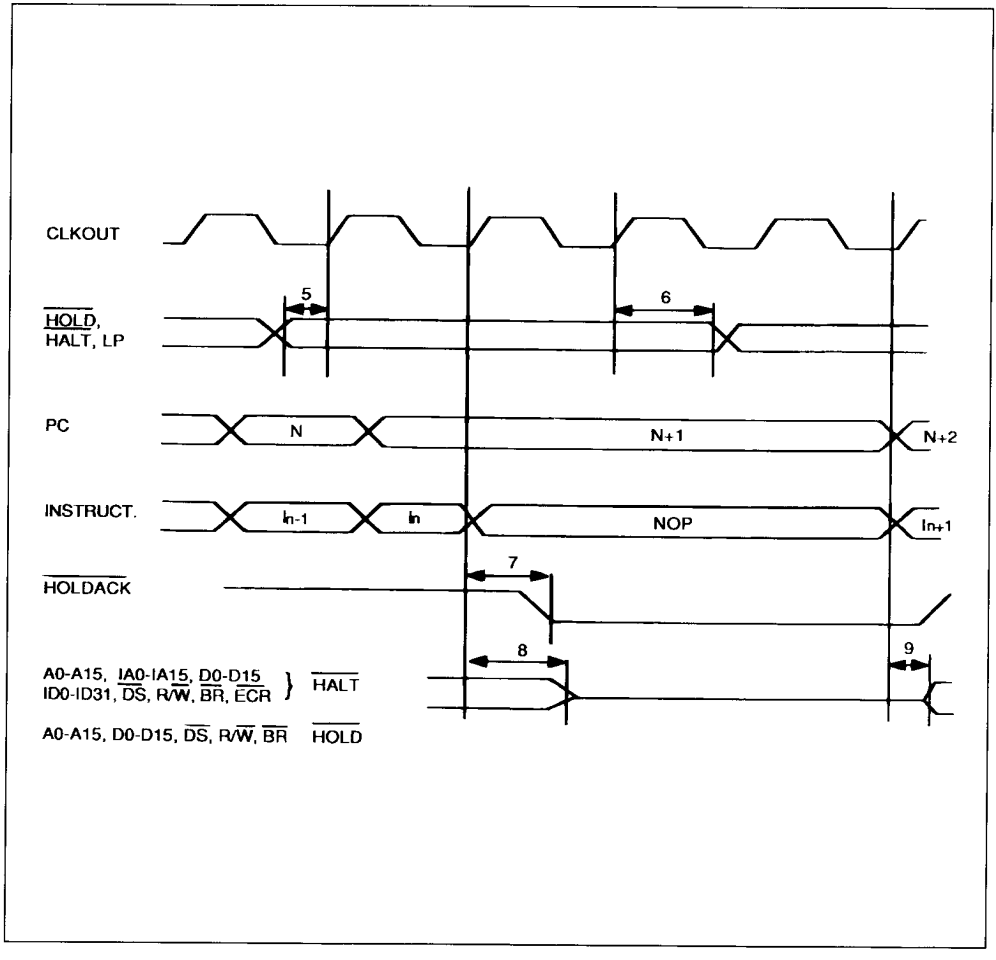
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.9. $\overline{HOLD}$, LP, $\overline{HALT}$ TIMING

Num.	Parameter	Min.	Max.	Unit
5	$\overline{HOLD}$ to CLKOUT Setup	20		ns
6	$\overline{HOLD}$ to CLKOUT Hold	5		ns
7	CLKOUT High to $\overline{HOLDACK}$ Low		30	ns
8	CLKOUT High to HI-Z	5	30	ns
9	CLKOUT High to Valid	0	5	ns

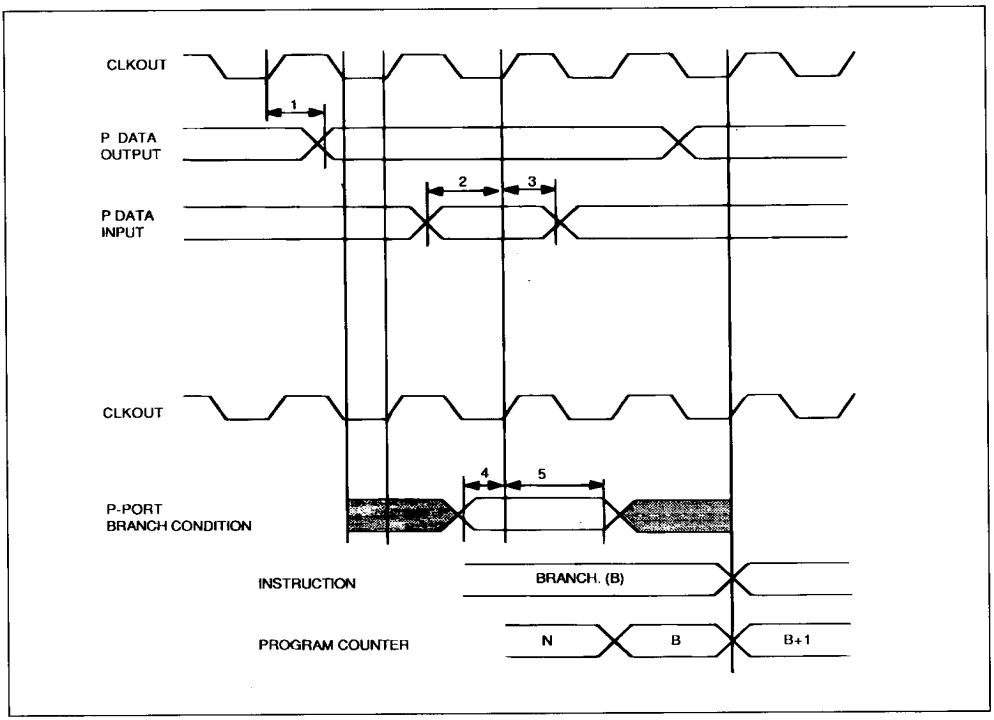
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.10. P-PORT TIMING

Num.	Parameter	Min.	Max.	Unit
1	CLKOUT to High to P0:7 Valid		30	ns
2, 4	P0:P7 to CKLOUT Setup	20		ns
3, 5	P0:P7 to CKLOUT Hold	5		ns

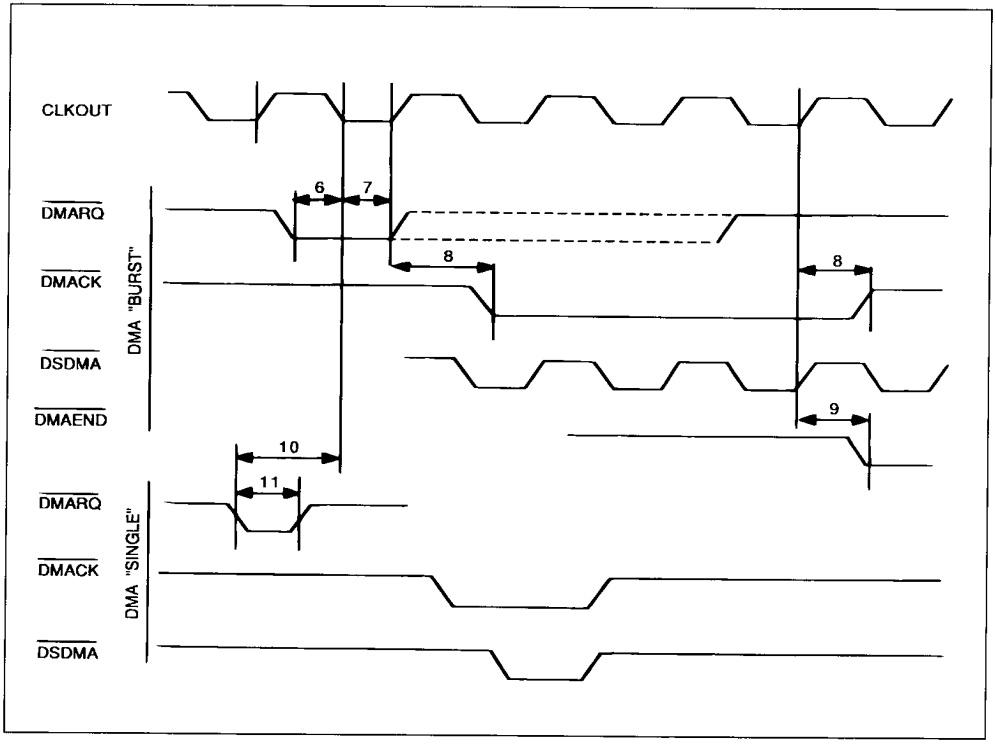
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.



7.11. DMA TIMING

Num.	Parameter	Min.	Max.	Unit
6	$\overline{\text{DMARQ}}$ to CLKOUT Setup	20		ns
7	$\overline{\text{DMARQ}}$ to CLKOUT Hold	5		ns
8	$\overline{\text{DMACK}}$ to CLKOUT Delay		30	ns
9	CLKOUT High to $\overline{\text{DMAEND}}$ Valid		30	ns
10	$\overline{\text{DMARQ}}$ to CLKOUT Setup	40		ns
11	$\overline{\text{DMARQ}}$ Pulse Width	10		ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

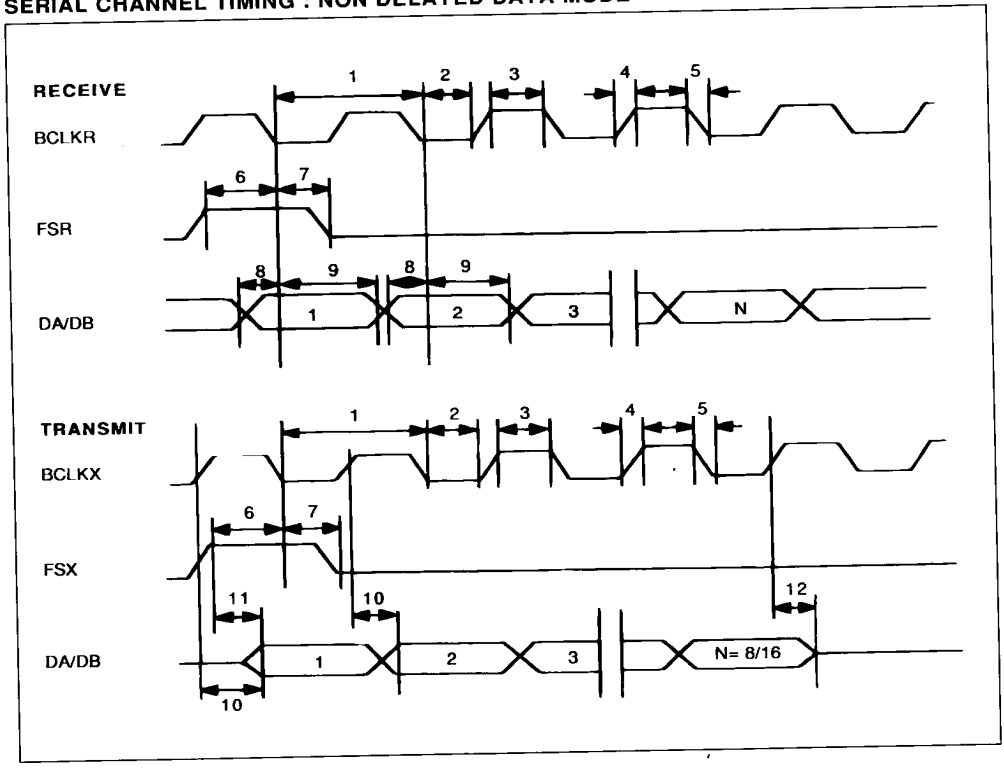


7.12. SERIAL CHANNEL TIMING

Num.	Parameter	Min.	Max.	Unit
1	BCLKR, BCLKX Period	200		ns
2	BCLKR, BCLKX Width Low	80		ns
3	BCLKR, BCLKX Width High	80		ns
4	BCLKR, BCLKX Rise Time		30	ns
5	BCLKR, BCLKX Fall Time		30	ns
6	FSR, FSX to BCLKX, BCLKR Setup	30		ns
7	FSR, FSX to BCLKX, BCLKR Hold	0		ns
8	DA, DB to BCLKR Setup	20		ns
9	DA, DB to BCLKR Hold	0		ns
10	BCLKX High to DA, DB Valid		30	ns
11	FSX High to DA, DB Valid		30	ns
12	BCLKX High to DA, DB-Z	0	30	ns

Serial Channel Timing : Non Delayed Data Mode.
Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

SERIAL CHANNEL TIMING : NON DELAYED DATA MODE

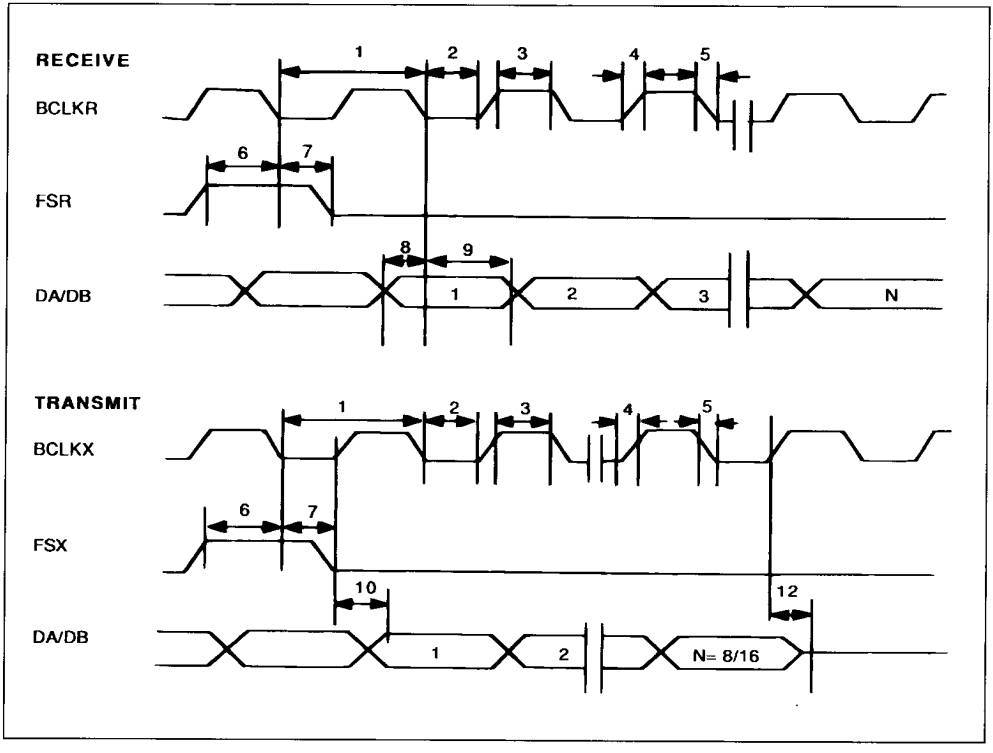


SGS-THOMSON MICROELECTRONICS

Num.	Parameter	Internal Clock		External Clock		Unit
		Min.	Max.	Min.	Max.	
1	BCLKR, BCLKX Period	200		125		ns
2	BCLKR, BCLKX Width Low	80		50		ns
3	BCLKR, BCLKX Width High	80		50		ns
4	BCLKR, BCLKX Rise Time		30		10	ns
5	BCLKR, BCLKX Fall Time		30		10	ns
6	FSR, FSX to BCLKR, BCLKX Setup	30		30		ns
7	FSR, FSX to BCLKR, BCLKX Hold	0		0		ns
8	DA, DB to BCLKR Setup	20		20		ns
9	DA, DB to BCLKR Hold	0			30	ns
10	BCLKX High to DA, DB Valid		30		30	ns
12	BCLKX High to DA, DB-Z		30		30	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

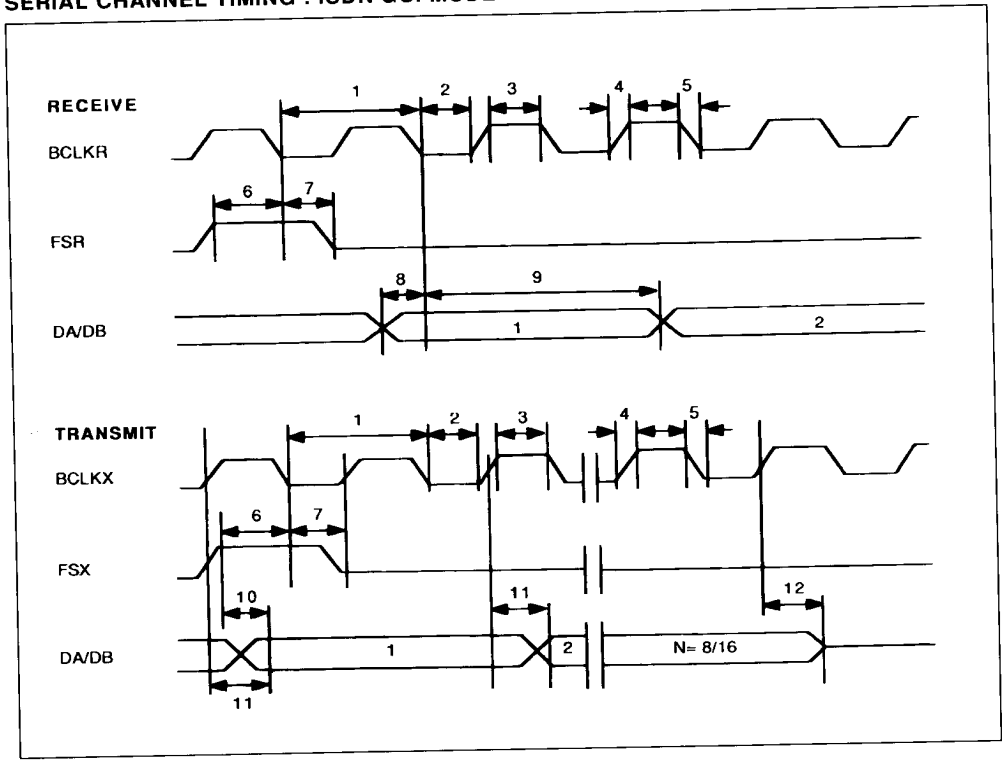
SERIAL CHANNEL TIMING : DELAYED DATA MODE



Num.	Parameter	Internal Clock		External Clock		Unit
		Min.	Max.	Min.	Max.	
1	BCLKR, BCLKX Period	200		125		ns
2	BCLKR, BCLKX Width Low	80		50		ns
3	BCLKR, BCLKX Width High	80		50		ns
4	BCLKR, BCLKX Rise Time		30		10	ns
5	BCLKR, BCLKX Fall Time		30		10	ns
6	FSR, FSX to BCLKR, BCLKX Setup	30		30		ns
7	FSR, FSX to BCLKR, BCLKX Hold	0		0		ns
8	DA, DB to BCLKR Setup	20		20		ns
9	DA, DB to BCLKR Hold	0			30	ns
10	BCLKX High to DA, DB Valid		30		30	ns
11	FSX High to DA, DB Valid		30		30	ns
12	BCLKX High to DA, DB-Z		30		30	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

SERIAL CHANNEL TIMING : ISDN GCI MODE



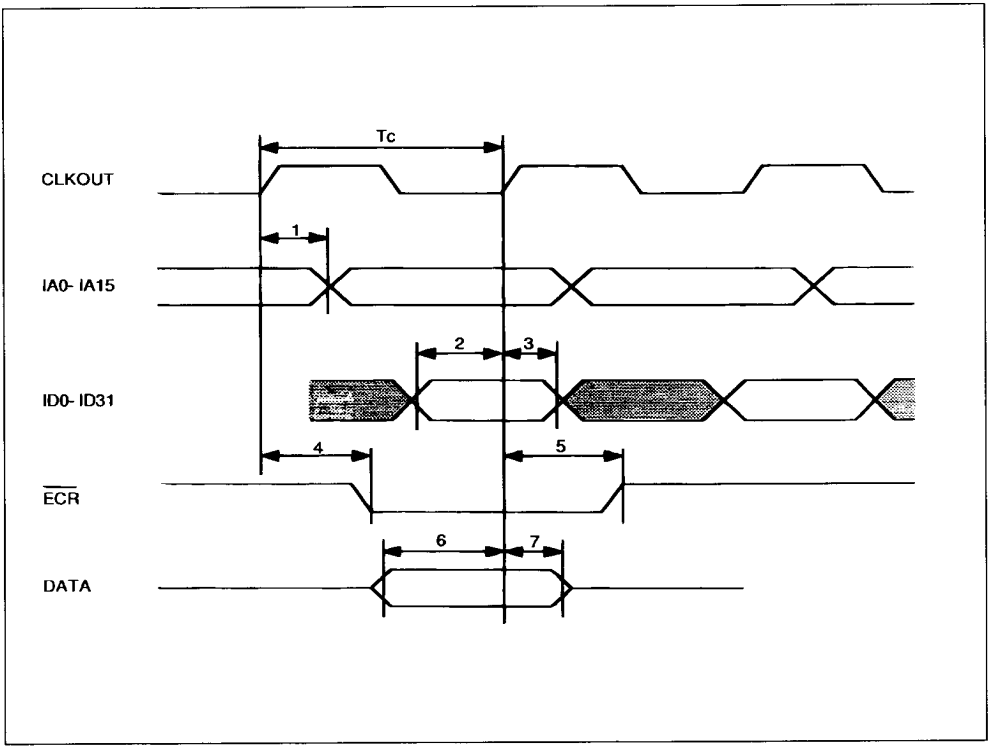
SGS-THOMSON MICROELECTRONICS

7.13. INSTRUCTION BUS TIMING ST 18941

Num.	Parameter	Min.	Max.	Unit
1	CLKOUT High to Address Valid		25	ns
2	Data to CLKOUT Setup	40		ns
3	Data to CLKOUT Hold	5		ns
4	CLKOUT High to ECR Valid		30	ns
5	$\overline{ECR}$ to CLKOUT Hold	5		ns
6	Data to CLKOUT Setup	15		ns
7	Data to CKLOUT Hold	5		ns
8	CLKOUT High to HI Low Delay	− 5	+ 5	ns
9	CLKOUT Low to HI High Delay	− 5	+ 5	ns

Conditions : V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.

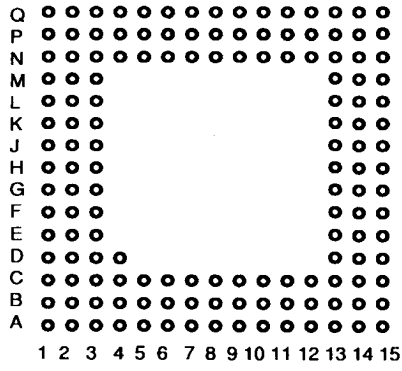
INSTRUCTION BUS TIMING



8. PIN CONNECTIONS

8.1 ST18941 : OPEN VERSION

144-pin Pin Grid Array Ceramic Package



BOTTOM VIEW

ST18941 PIN GRID ARRAY 144-PIN

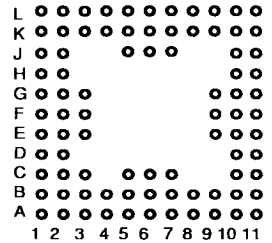
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	SD7	C7	VDD	H13	VSS	N10	ID11
A2	SD3	C8	VSS	H14	DPI1	N11	ID5
A3	CS	C9	D12	H15	DPI0	N12	ID2
A4	SB/W / SWR	C10	D8	J1	IA8	N13	ID1
A5	SDS / SRD	C11	D4	J2	IA10	N14	HT2
A6	VDD	C12	VDD	J3	VDD	N15	HOLDA
A7	VDD	C13	A14	J13	DPI4	P1	INT
A8	VSS	C14	A11	J14	DPI5	P2	RESET
A9	D14	C15	A8	J15	DPI2	P3	ID31
A10	D13	D1	P1	K1	IA9	P4	ID29
A11	D10	D2	P5	K2	IA11	P5	ID26
A12	D7	D3	VSS	K3	VSS	P6	ID23
A13	D5	D13	A13	K13	CLKOUT	P7	ID21
A14	D2	D14	A9	K14	DTACK	P8	ID17
A15	D0	D15	A7	K15	DPI3	P9	ID13
B1	P6	E1	IA1	L1	VSS	P10	ID12
B2	SD6	E2	P2	L2	VSS	P11	ID9
B3	SD2	E3	P4	L3	IA15	P12	ID6
B4	SD0	E13	A10	L13	DS / RD	P13	ID4
B5	RS	E14	A6	L14	XTAL	P14	ID0
B6	IRQ	E15	A5	L15	BR	P15	ECR
B7	VDD	F1	IA4	M1	IA12	Q1	LP
B8	D15	F2	IA0	M2	IA14	Q2	ID30
B9	D11	F3	P0	M3	NMI	Q3	ID27
B10	D9	F13	A4	M13	VSS	Q4	ID25
B11	D6	F14	A3	M14	R/W / WR	Q5	ID22
B12	D3	F15	A1	M15	EXTAL	Q6	ID19
B13	D1	G1	IA5	N1	IA13	Q7	ID18
B14	A15	G2	IA2	N2	HALT	Q8	ID16
B15	A12	G3	IA3	N3	INCYCLE	Q9	ID15
C1	P3	G13	VDD	N4	VSS	Q10	ID14
C2	P7	G14	A2	N5	ID28	Q11	ID10
C3	SD5	G15	A0	N6	ID24	Q12	ID8
C4	SD4	H1	IA7	N7	ID20	Q13	ID7
C5	SD1	H2	IA6	N8	VDD	Q14	ID3
C6	SDTACK	H3	VSS	N9	VSS	Q15	HOLD

8.2. ST18940 : MASKED VERSION

84-pin Pin Grid Array Ceramic Package

ST18940 PLCC 84-PIN

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	A9	B11	LP	F9	VSS	L11	SD2
A2	A7	C1	A13	F10	VDD	K2	VSS
A3	A6	C2	A11	F11	P3	K3	D13
A4	A4	C5	A3	G1	D4	K4	IRQ
A5	A1	C6	VDD	G2	D5	K5	RS
A6	A0	C7	XTAL	G3	D6	K6	VSS
A7	CLKOUT	C10	HOLD	G9	P0	K7	DPI1
A8	BR	C11	RESET	G10	P1	K8	DPI4
A9	HOLDA	D1	A15	G11	P2	K9	SD1
A10	DS / RD	D2	A14	H1	D7	K10	VSS
A11	HT2	D10	INT	H2	D8	K11	SD4
B1	A12	D11	P7	H10	SD6	L1	D12
B2	A10	E1	D2	H11	SD7	L2	D14
B3	A8	E2	D1	J1	D9	L3	D15
B4	A5	E3	D0	J2	D11	L4	SDTACK
B5	A2	E9	P6	J5	SDS	L5	SR/W / SWR
B6	VSS	E10	P5	J6	VDD	L6	CS
B7	EXTAL	E11	P4	J7	DPI2	L7	DPI0
B8	DTACK	F1	D3	J10	SD3	L8	DPI3
B9	R/W / WR	F2	VDD	J11	SD5	L9	DPI5
B10	VDD	F3	VSS	K1	D10	L10	SD0

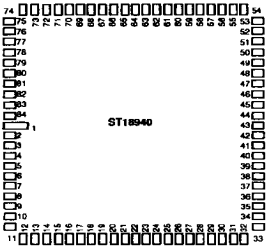


BOTTOM VIEW

84-pin Plastic Leaded Chip Carrier

ST18940 PLCC 84-PIN

PAD	NAME	PAD	NAME	PAD	NAME	PAD	NAME
1	VDD	22	VSS	43	VDD	64	VSS
2	A0	23	D3	44	CS	65	P3
3	A1	24	D4	45	DPI0	66	P4
4	A2	25	D5	46	DPI1	67	P5
5	A3	26	D6	47	DPI2	68	P6
6	A4	27	D7	48	DPI3	69	P7
7	A5	28	D8	49	DPI4	70	INT
8	A6	29	D9	50	DPI5	71	RESET
9	A7	30	D10	51	SD0	72	LP
10	A8	31	D11	52	SD1	73	HOLD
11	A9	32	D12	53	SD2	74	HT2
12	A10	33	VSS	54	VSS	75	VDD
13	A11	34	D13	55	SD3	76	R/W / WR
14	A12	35	D14	56	SD4	77	DS / RD
15	A13	36	D15	57	SD5	78	HOLDA
16	A14	37	IRQ	58	SD6	79	DTACK
17	A15	38	SDTACK	59	SD7	80	BR
18	D0	39	SDS / SRD	60	P0	81	XTAL
19	D1	40	RS	61	P1	82	EXTAL
20	D2	41	SR/W / SWR	62	P2	83	CLKOUT
21	VDD	42	VSS	63	VDD	84	VSS



TOP VIEW

9. ORDERING INFORMATION

9.1. DEVICE TYPE

Part Number	Operating Temperature Range*	Package Type
ST 18940 CR/PXXX**	0 to + 70°C	84 - pin Ceramic Pin Grid Array
ST 18940 CFN/PXXX	0 to + 70°C	84 - pin Plastic Leaded Chip Carrier
ST 18941 CR	0 to + 70°C	144 - pin Ceramic Pin Grid Array

** XXX is the specific number associated to the customer code.
* for extended temperature range, please consult ST sales offices.

9.2. SOFTWARE TOOLS

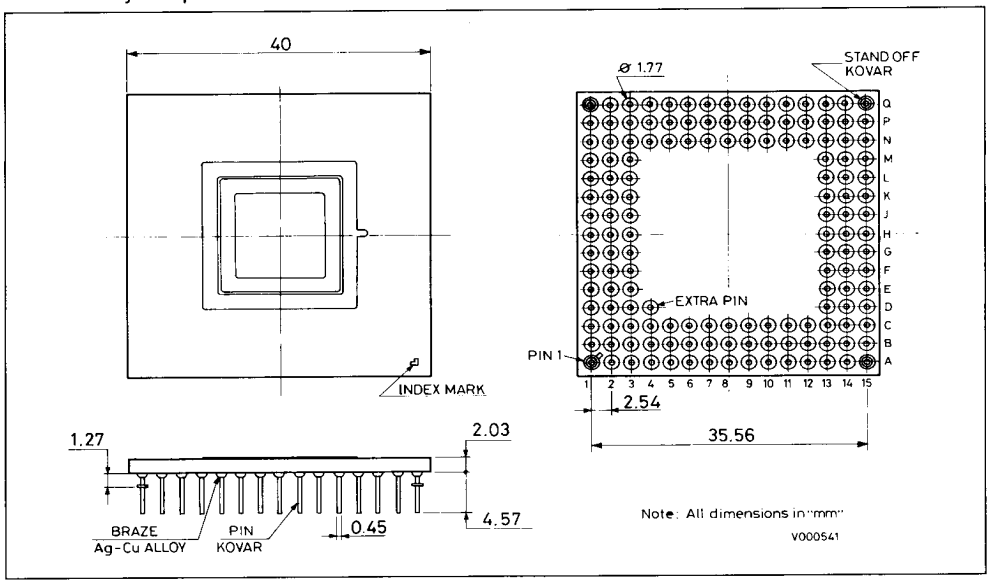
ST 18940 SP-PC	Software Package Including Macroassembler Functionnal Stimulator Linker for PC
ST 18940 SP-VM	Same Software Package for VAX Machines
ST 18940 SPC-PC	Same Software with C-compiler for PC
ST 18940 SPC-VM	Same Software Package with C - Compiler for VAX

9.3. HARDWARE TOOLS

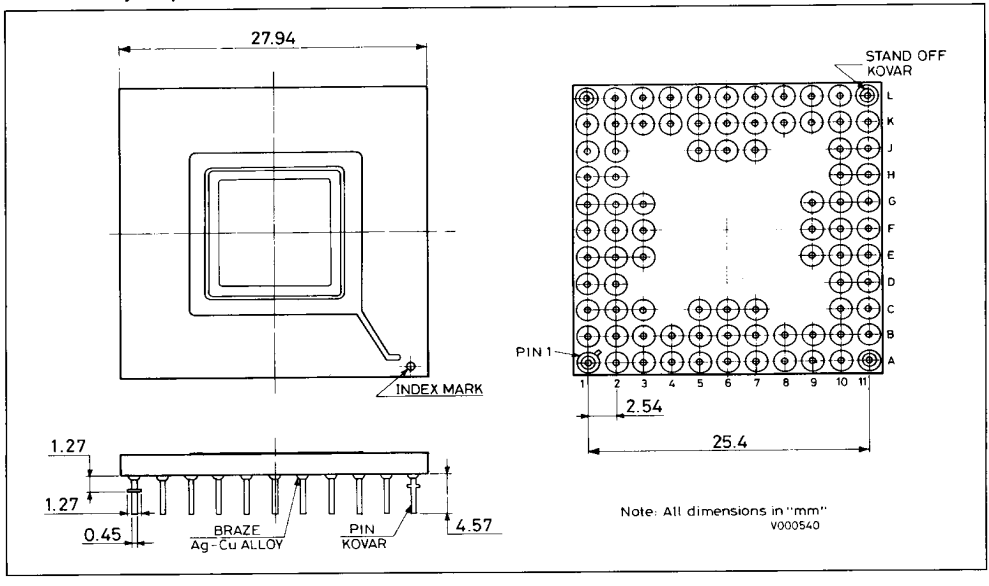
ST 18940 EMU	Stand - Alone Emulator
ST 18940 HDS-110	Hardware Development System 110V Power Supply
ST 18940 HDS-220	Hardware Development System 220V Power Supply
ST 18940 EPROM	EPROM Simulation Module for ST 18940
ST 18940-PC	PC Compatible Emulation Board

10. MECHANICAL DATA

Pin Grid Array 144-pin - ST18941



Pin Grid Array 84-pin - ST18940



11. DEVELOPMENT TOOLS

11.1. DESIGN PROCEDURE

The design of a digital signal processing application using the ST18940/41 is supported by a complete range of dedicated software and hardware tools including macroassembler, linker, high-level simulator and a C compiler and optimizer.

Additional hardware design tools include :

1 - stand alone emulation card ST18940-EMU
2 - multiprocessor hardware development system ST18940-HDS
3 - EPROM emulation module ST18940-EPROM
4 - PC compatible card ST18940-PC.

11.2. SOFTWARE TOOLS

All the development softwares run on the most common computers, such as IBM-PC XT, AT, under MS-DOS, VAXR under VMS, UNIXR or ULTRIX operating systems.

The macroassembler supports conditional assembly, high level language facilities for loop definition and generates all the files for simulation, emulation and PROM programming.

The functional simulator provides step by step execution, break on address and data values, access to all internal registers and interface to I/O files (ADC, DAC, test inputs).

The linker provides modular programming facilities.

The library consists of macros, basic DSP routines etc... and provides additional help to user's for their applications.

The C language compiler offers high-level language facilities which meets the advanced requirements (parallelism, pipe-line, three computation modes, 32-bit instruction set) to the ST18940.

11.3. HARDWARE TOOLS

All the hardware tools are designed to provide ease of use and minimum learning time by means of a menu driven interface and DSP specific emulation features.

ST18940 EMU and ST18940 HDS have in common :

- Full speed emulation of ST18940 and ST18941
- Use of internal or external clock
- 28 breakpoints (stops at defined addresses)
- 8 conditional breakpoints (stop after N address X and M address Y)
- Realtime trace of internal resources
- Emulation probes (for ST18940 - 41)
- Menu driven operation (about 100 commands)
- Resident Assembler/Disassembler with full screen editor
- Symbolic debugging
- Direct link with PROM programmers
- Direct link with host (KERMIT protocol)

Emulator specific features :

The ST18940 EMU is a low cost, stand-alone emulator providing advanced emulation features such as real-time trace. It can be driven via a RS232C link by a terminal or an IBM-PC^{R} and offers :

- 3K program memory
- 4K x 16-bit data RAM
- A wire-wrapping area
- Full speed 100 ns cycle emulation
- 2 RS232C serial ports
- Complex conditions break-points

Hardware development station features :

The ST18941 HDS is a hardware development station, aimed at the development of multiprocessor applications. Up to four pairs of emulator board/logic analyzer board can be combined to match exactly the user's needs :

- CMOS memory for backup of configuration
- 64K x 32 program memory
- 64K x 16 data RAM (mapping on a word basis)
- A logic analyser with :

*2K x 119 bits for trace of ST18940-41 bus and 15 external inputs

*Synchronous analyser on program and local buses

*Asynchronous analyser on system bus or external inputs

*Triggering conditions (Address bus with count, data bus external branch inputs, mailbox exchanges, external inputs).

EPROM module :

The ST18940 EPROM is a small-sized module which uses the perfect compatibility between ST18940 and ST18941. The module uses a ST18941 and fast EPROM memories to emulate in real time a ROM masked ST18940 during prototyping or field tests to minimize hardware developments. The module is plug - and function-compatible with ST18940.

APPENDIX A - BENCHMARKS

	Execution Time 100ns Instruction Cycle	**Memory Size** (words) **Prgm + coef.**
20 Tap FIR Filter	2.4µs	6 + 20
64 Tap FIR Filter	6.8µs	6 + 64
67 Tap FIR Filter	7.1µs	6 + 67
20 Tap Double Precision FIR Filter	7.6µs	26 + 40
3x3 Bidimentional FIR Filter	8.5µs	8 + 9
20 Tap Adaptive FIR Filter	4.6µs	12
8 Pôle Cascaded Canonic Biqual IIR Filter (4x)	2.4µs	13 + 20
8 Pôle Cascaded Canonic Biqual IIR Filter (5x)	2.8µs	13 + 20
8 Pôle Cascaded Transpose Biqual IIR Filter	3.3µs	15 + 20
Dot Product 2 x 2	0.6µs	6
Matrix Mult (2x2) Times (2x2)	1.4µs	14
Matrix Mult (3x3) Times (3x1)	1.5µs	15
FFT 64 pts	90.3µs	45 + 64
FFT 256 pts	500.1µs	177 + 256
FFT 1024 pts	3.15ms	234 + 512
8x8 Discrete Cosine Transform	4.75ms	650 + 12

APPENDIX B

MASKING INFORMATION

The information required by SGS-THOMSON Microelectronics to realize a customer masked version of the ST18940 must include program ROM content and coefficient ROM content. They can be transferred on EPROMS, 5" 1/4 floppy disks, magnetic tapes (VAX/VMS format) or by link to SGS-THOMSON Microelectronics. This must be done in conjunction with your local sales office or representative indications.

VERIFICATION MEDIA

All original pattern media are filled for contractual purpose and are not returned. A computer listing of the ROM content code will be generated and returned to the customer with a listing verification form. The listing should be carefully checked and the approval form completed, signed and returned to SGS-THOMSON. The returned verification form is the contractual agreement for generation of the customer masks and batch manufacturing.

VERIFICATION UNITS

Ten engineering samples containing the customer ROM patterns will be sent for program verification.

These samples will be engineering samples and must be kept by user as reference parts.