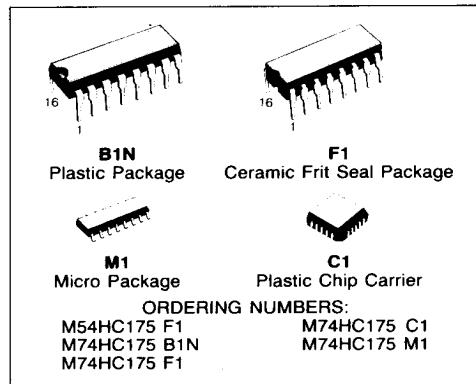


QUAD D-TYPE FLIP-FLOP WITH CLEAR

- HIGH SPEED
 $t_{PD} = 18 \text{ ns (TYP.)}$ at $V_{CC} = 5V$
- LOW POWER DISSIPATION
 $I_{CC} = 4 \mu\text{A (MAX.)}$ at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- OUTPUT DRIVE CAPABILITY
 10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
 $|I_{OH}| = |I_{OL}| = 4 \text{ mA (MIN.)}$
- BALANCED PROPAGATION DELAYS
 $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
 V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
 WITH 54/74LS175


DESCRIPTION

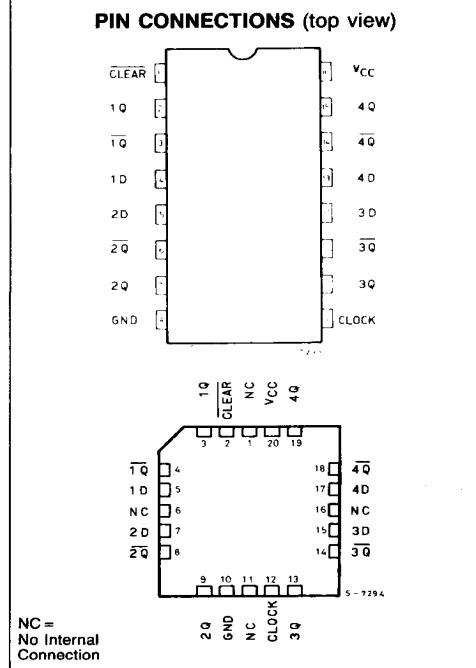
The M54/74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP WITH CLEAR fabricated in silicon gate CMOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

These four flip-flops are controlled by a clock input (CLOCK) and a clear input (CLEAR). The information data applied to the D inputs (1D to 4D) are transferred to the outputs (1Q to 4Q and $\bar{1}Q$ to $\bar{4}Q$) on the positive-going edge of the clock pulse. The reset function is accomplished when the clear input is taken low and all Q outputs are kept low regardless of other input conditions. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

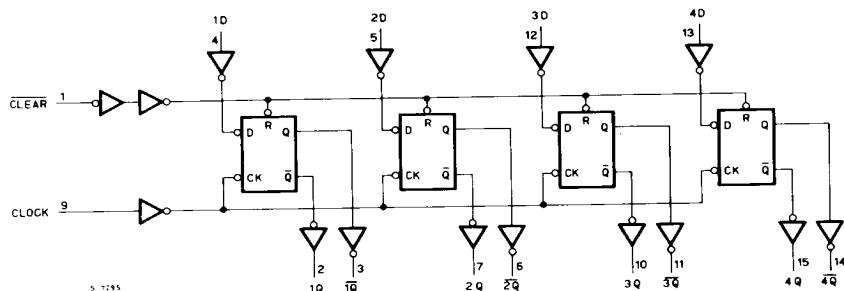
TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
CLEAR	D	CLOCK	Q	\bar{Q}	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Qn	$\bar{Q}n$	NO CHANGE

X: DON'T CARE



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) 500 mW: $\approx 65^\circ\text{C}$ derate to 300 mW by 10 mW/°C: 65°C to 85°C .

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	-40 to 85 -55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} { 2 V 4.5V 6 V } 0 to 1000 0 to 500 0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition	T _A =25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — 4.2	1.5 3.15 —	— — 4.2	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — 1.8	0.5 1.35 —	— — 1.8	0.5 1.35 —	— — 1.8	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0 4.5 6.0 4.5 6.0	V _I	I _O	1.9 4.4 5.9 — —	2.0 4.5 6.0 4.18 5.68	— — — 4.31 5.8	1.9 4.4 5.9 4.13 5.63	— — — 4.10 5.60	1.9 4.4 5.9 — —	V
		V _{IH} or V _{IL}	-20 μA	— — — — —	— — — — —	— — — — —	— — — — —	— — — — —	— — — — —	V	
		V _I	20 μA	— — — —	0.0 0.0 0.0 0.17	0.1 0.1 0.1 0.26	— — — —	0.1 0.1 0.1 0.33	— — — —	0.1 0.1 0.1 0.40	V
		V _{IH} or V _{IL}	4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _I	Input Leakage Current	6.0	V _I =V _{CC} or GND	—	—	±0.1	—	±1.0	—	±1.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I =V _{CC} or GND	—	—	4	—	40	—	80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V, T_A=25°C, C_L=15pF, Input t_r=t_f=6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PPLH} t _{PHL}	Propagation Delay Time (CLOCK-Q, \bar{Q})		18	28	ns
t _{PHL}	Propagation Delay Time (CLEAR-Q, \bar{Q})		20	32	ns
f _{MAX}	Maximum Clock Frequency	33	53		MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Q, \bar{Q})	2.0 4.5 6.0		— — —	105 21 18	165 33 28	— — —	205 41 35	— — —	250 50 43	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLEAR-Q, \bar{Q})	2.0 4.5 6.0		— — —	115 23 20	185 37 31	— — —	230 46 39	— — —	280 56 48	ns
f _{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	12 48 56	— — —	4.8 24 28	— — —	4 20 24	— — —	MHz
t _{W(H)} t _{W(L)}	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _{W(L)}	Minimum Pulse Width CLEAR	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t _s	Minimum Set-up Time	2.0 4.5 6.0		— — —	10 3 3	50 10 9	— — —	65 13 11	— — —	75 15 13	ns
t _h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t _{REM}	Minimum Removal Time (CLEAR)	2.0 4.5 6.0		— — —	0 0 0	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
C _{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C _{PD} (*)	Power Dissipation Capacitance			—	71	—	—	—	—	—	pF

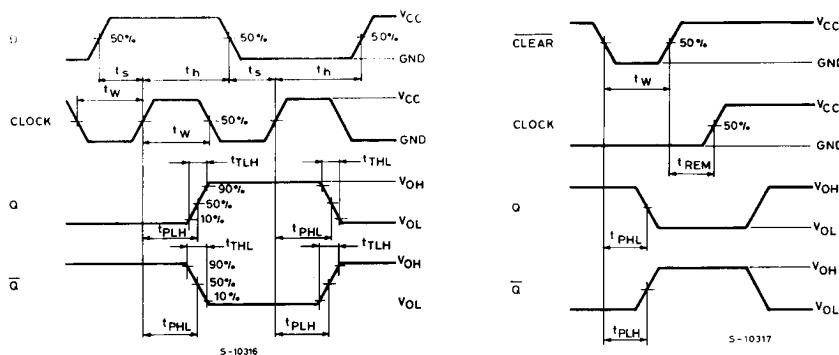
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (for Flip/Flop).}$$

And the total C_{PD} at the time when n pcs of Flip-Flop operate can be gained C_{PD} (total) = 43 + 28 × n

SWITCHING CHARACTERISTICS TEST WAVEFORM

TEST CIRCUIT I_{CC} (Opr.)