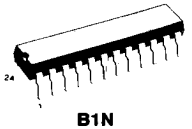
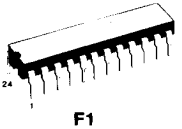
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- HIGH NOISE IMMUNITY
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS181



B1N
Plastic Package



F1
Ceramic Frit Seal Package

M1
Micro Package

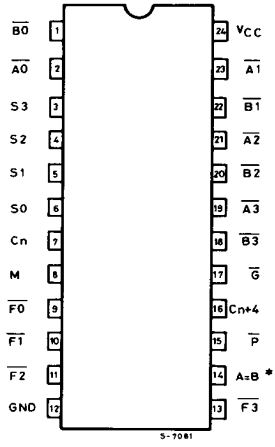
ORDERING NUMBERS:

M54HC181 F1	M74HC181 M1
M74HC181 B1N	M74HC181 F1

DESCRIPTION

The M54/74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR fabricated with silicon gate C²MOS technology. It has the same high speed performance of SLTTL combined with true CMOS low power consumption. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (SO, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing aritmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the M54HC182 or M74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. These circuits will accomodate active-high or active-low data, if the pin designations are interpreted as shown below. Subtraction is accomplished by 1,s complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is 1—B—1, which requires an end-around or forced carry to produce A—B. The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicated equality (A = B).

PIN CONNECTIONS (top view)



*: Open drain Output Structure

DESCRIPTION (Continued)

The ALU should be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-drain so that it can be wire-AND connected to give a comparison for more that four bits. The carry output ($Cn + 4$) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively. These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry.

All inputs are equipped with portection circuits against static discharge and transient excess voltage.

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A = B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn + 4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
ACTIVE-LOW DATA (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn + 4	$\overline{P}$	$\overline{G}$
ACTIVE-HIGH DATA (Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	Cn	Cn + 4	X	Y

Input Cn	Output Cn + 4	Active-Low data (Figure 1)	Active-High data (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

Figure 1

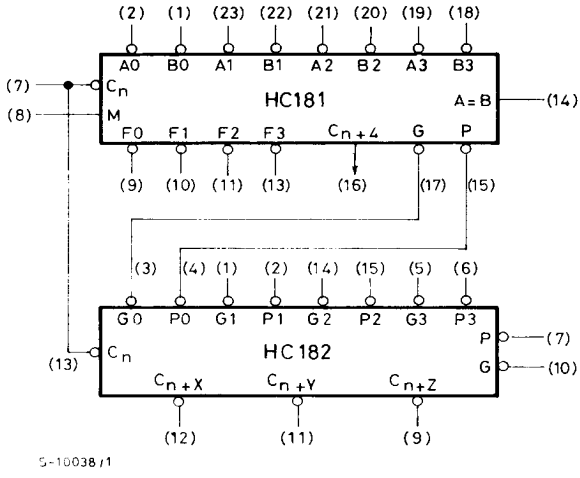


TABLE 1

Selection				Active Low Data		
				M = H Logic Functions	M = L: Arithmetic Operations	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ Minus 1	$F = (A\overline{B})$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus $(A + \overline{B})$	F = A Plus $(A + \overline{B})$ Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus (A + B)	F = AB Plus $(A + \overline{B})$ Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	$F = (A + \overline{B})$ Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = A\overline{B}$ Plus (A + B)	$F = A\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	$F = A\overline{B}$ Plus A	$F = A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.

Figure 2

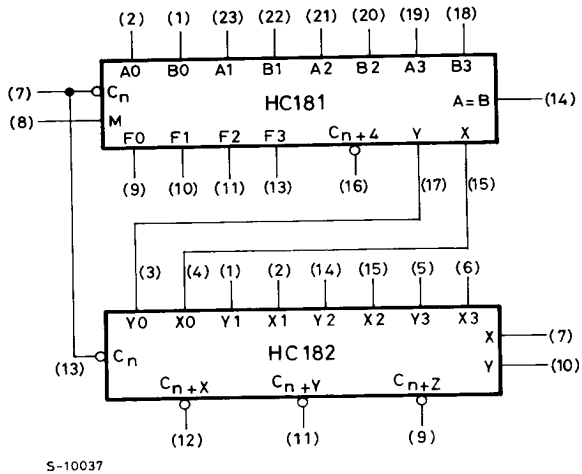
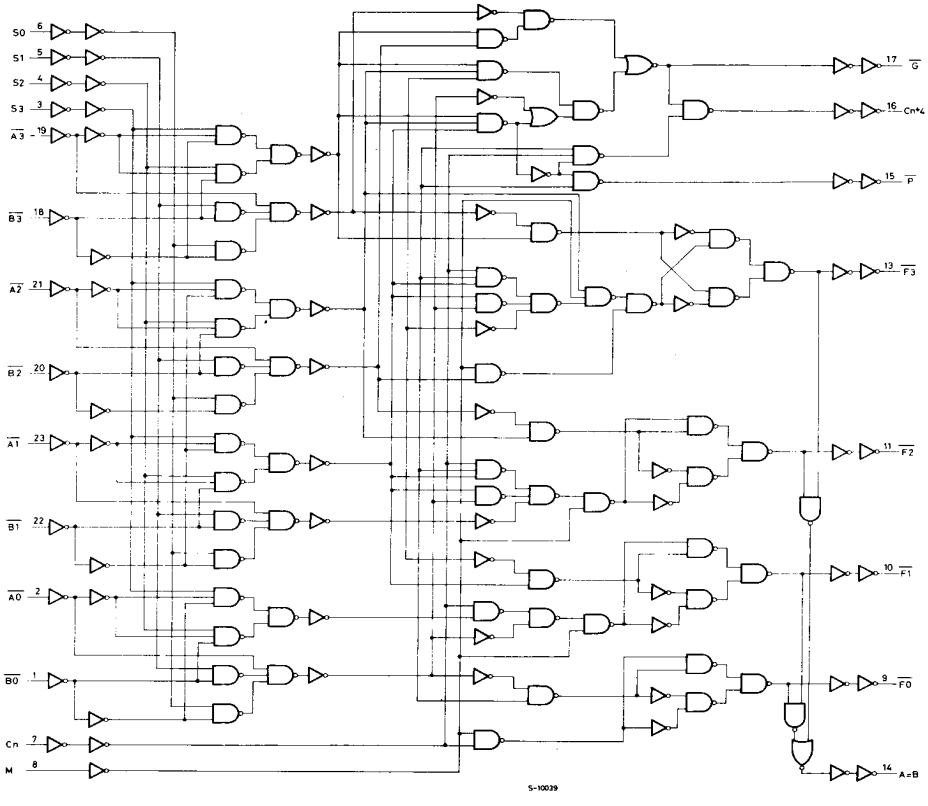


TABLE 2

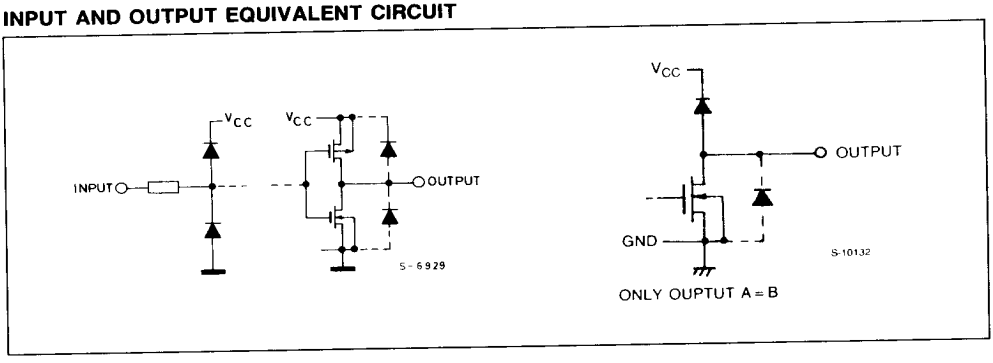
Selection				Active High Data		
				M = H	M = L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F=\overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F=\overline{A+B}$	$F=A+B$	$F=(A+B)$ Plus 1
L	L	H	L	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Comp1)	F = Zero
L	H	L	L	$F=\overline{AB}$	$F=A$ Plus $A\overline{B}$	$F=A$ Plus $A\overline{B}$ Plus 1
L	H	L	H	$F=\overline{B}$	$F=(A+B)$ Plus $A\overline{B}$	$F=(A+B)$ Plus $A\overline{B}$ Plus 1
L	H	H	L	$F=A\oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F=A\overline{B}$	$F=A\overline{B}$ Minus 1	$F=A\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F=\overline{A\oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F=(A+\overline{B})$ Plus AB	$F=(A+\overline{B})$ Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F=A+\overline{B}$	$F=(A+B)$ Plus A	$F=(A+B)$ Plus A Plus 1
H	H	H	L	$F=A+B$	$F=(A+\overline{B})$ Plus A	$F=(A+\overline{B})$ Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



INPUT AND OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	−40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} 2 V	0 to 1000	ns
			V_{CC} 4.5V	0 to 500	
			V_{CC} 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage		V_{IN}	I_{OH}								
		2.0	$V_{IH} = V_{IL}$ Any output except A = B	$-20\ \mu A$	1.9	2.0	—	1.9	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		-4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		-5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage			I_{OL}								
		2.0	V_{IN} or V_{IH}	$20\ \mu A$	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_{IN}	Input Leakage Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	± 0.1	—	± 1	—	± 1	μA
I_{OZ}	3-State Output Off state Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$		—	—	± 0.5	—	± 5.0	—	± 10	
I_{CC}	Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND		—	—	4	—	40	—	80	

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (1)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time (2)		27	42	ns
t_{PLH} t_{PHL}	Propagation Delay Time (3)		26	41	ns
t_{PLH} t_{PHL}	Propagation Delay Time (4)		24	37	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (5)		25	39	ns
t_{PLH} t_{PHL}	Propagation Delay Time (6)		24	38	ns
t_{PLH} t_{PHL}	Propagation Delay Time (7)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (8)		23	37	ns
t_{PLH} t_{PHL}	Propagation Delay Time (9)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (10)		30	46	ns
t_{PLH} t_{PHL}	Propagation Delay Time (11)		24	37	ns
t_{PZL}	3-State Output•Enable Time (12)		27	42	ns
t_{PLZ}	3-State Output•Disable Time (12)		29	46	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	95	—	110	ns
		4.5		—	8	15	—	19	—	22	
		6.0		—	7	13	—	16	—	19	
t_{PLH} t_{PHL}	Propagation Delay Time (1)	2.0		—	68	135	—	170	—	205	ns
		4.5		—	17	27	—	34	—	41	
		6.0		—	14	23	—	29	—	35	
t_{PLH} t_{PHL}	Propagation Delay Time (2)	2.0		—	124	240	—	300	—	360	ns
		4.5		—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLH} t_{PHL}	Propagation Delay Time (3)	2.0		—	120	235	—	295	—	355	ns
		4.5		—	30	47	—	59	—	71	
		6.0		—	26	40	—	50	—	60	
t_{PLH} t_{PHL}	Propagation Delay Time (4)	2.0		—	112	215	—	270	—	325	ns
		4.5		—	28	43	—	54	—	65	
		6.0		—	24	37	—	46	—	55	

AC ELECTRICAL CHARACTERISTICS (Continued)

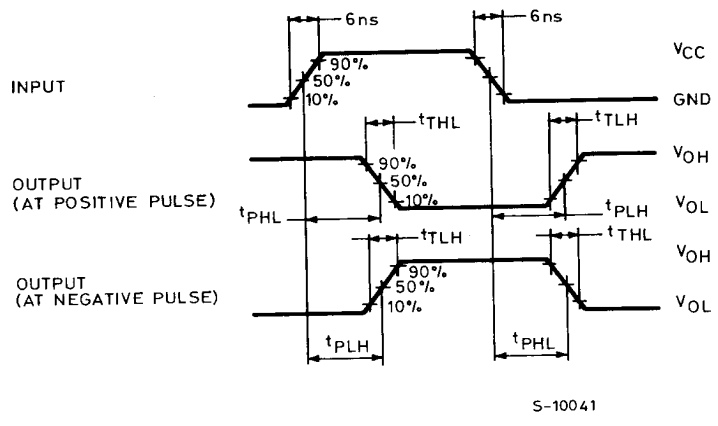
Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			-40 to $85°C$ 74HC		-55 to $125°C$ 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (5)	2.0		—	116	225	—	280	—	340	ns
		4.5		—	29	45	—	56	—	68	
		6.0		—	25	38	—	48	—	58	
t_{PLH} t_{PHL}	Propagation Delay Time (6)	2.0		—	116	220	—	275	—	330	ns
		4.5		—	29	44	—	55	—	66	
		6.0		—	25	37	—	47	—	56	
t_{PLH} t_{PHL}	Propagation Delay Time (7)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (8)	2.0		—	108	210	—	265	—	315	ns
		4.5		—	27	42	—	53	—	63	
		6.0		—	23	36	—	45	—	54	
t_{PLH} t_{PHL}	Propagation Delay Time (9)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	
t_{PLH} t_{PHL}	Propagation Delay Time (10)	2.0		—	136	265	—	335	—	400	ns
		4.5		—	34	53	—	66	—	80	
		6.0		—	29	45	—	56	—	68	
t_{PLH} t_{PHL}	Propagation Delay Time (11)	2.0		—	112	215	—	270	—	325	ns
		4.5		—	28	43	—	54	—	65	
		6.0		—	24	37	—	46	—	55	
t_{PZL}	3-State Output Enable Time (12)	2.0		—	124	240	—	300	—	360	ns
		4.5	$R_L = 1k\Omega$	—	31	48	—	60	—	72	
		6.0		—	26	41	—	51	—	61	
t_{PLZ}	3-State Output Disable Time (12)	2.0		—	140	260	—	325	—	390	ns
		4.5	$R_L = 1k\Omega$	—	35	52	—	65	—	78	
		6.0		—	30	44	—	55	—	66	
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{PD} (*)	Power Dissipation Capacitance			—	216	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average operating current can be obtained by the following equation:
$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

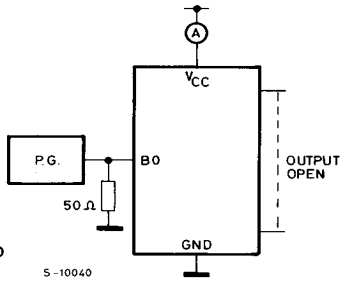
PROPAGATION DELAY TIME TEST CONDITIONS

Test No.	From (Input)	To (Output)	Test Conditions
(1)	Cn	Cn + 4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn + 4	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M = GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = GND, S0 = S3 = V_{CC}, S1 = S2 = GND ($\overline{SUM}$ mode)
(10)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{A1}$ or $\overline{B1}$	$\overline{Fi}$	M = V_{CC} (Logic Mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A = B	M = GND, S0 = S3 = GND, S1 = S2 = V_{CC} ($\overline{DIFF}$ mode)

SWITCHING CHARACTERISTICS TEST WAVEFORM



TEST CIRCUIT I_{CC} (Opr.)



Input Condition:
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$, S0, S3, Cn = V_{DD}
$\overline{B1}$, $\overline{B2}$, $\overline{B3}$, S1, S2, M = GND

INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST