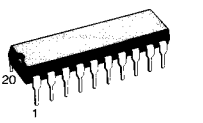
SGS-THOMSON MICROELECTRONICS

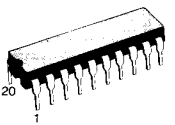
M54HCT374
M74HCT374

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

- LOW POWER DISSIPATION
  I_{CC} = 4 μA (MAX.) at T_A = 25°C
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2 V (MIN) V_{IL} = 0.8 V (MAX.)
- OUTPUT DRIVE CAPABILITY
  15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}| = I_{OL}$ = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS374



B1N
Plastic Package



F1
Ceramic Frit Seal Package

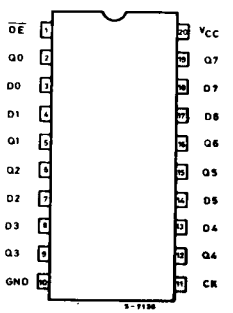
M1
Micro Package

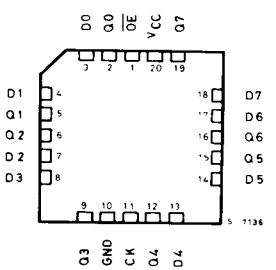
C1
Plastic Chip Carrier

ORDERING NUMBERS:

M54HCT374 F1
M74HCT374 B1N
M74HCT374 F1
M74HCT374 C1
M74HCT374 M1

PIN CONNECTIONS (top view)





NC = No Internal Connection

DESCRIPTION

The M54/74HCT374 is a high speed CMOS OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set precisely to the logic state that was setup at the D inputs.

While the $\overline{OE}$ input is low, the eight outputs will be in a normal logic state (high or low logic level), and while high, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

The three-state output configuration and the wide choice of outline will make its application in bus-organized system simple. All inputs are equipped with protection circuits against static discharge and transient excess voltage. This integrated circuit has totally compatibility, input and output characteristic is with standard 54/74 LSTTL logic families.

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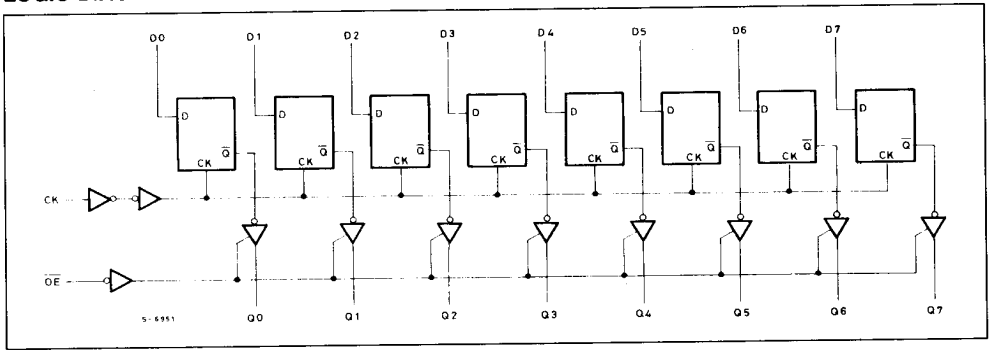
TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X: DON'T CARE — Z: HIGH IMPEDANCE

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		4.5 to 5.5	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 − 55 to 125	°C
t_r, t_f	Input Rise and Fall Time		0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0	—	—	2.0	—	2.0	—	V
V_{IL}	Low Level Input Voltage	4.5 to 5.5			—	—	0.8	—	0.8	—	0.8	V
V_{OH}	High Level Output Voltage	4.5	V_{IN}	I_{OH}								V
			V_{IH} or V_{IL}	− 20 μA	4.4	4.5	—	4.4	—	4.4	—	
				− 6.0 mA	4.18	4.31	—	4.13	—	4.10	—	
V_{OL}	Low Level Output Voltage	4.5	V_{IN}	I_{OL}								V
			V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	
				6.0 mA	—	0.17	0.26	—	0.33	—	0.40	
I_{OZ}	3-State Output Off-State Current	5.5	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		—	—	±0.5	—	±5.0	—	±10.0	μA
I_{IN}	Input Leakage Current	5.5	V_{IN} = V_{CC} or GND		—	—	±0.1	—	±1	—	±1	μA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND		—	—	4	—	40	—	80	μA
I_{CC}			Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		—	—	2.0	—	2.9	—	3.0	mA

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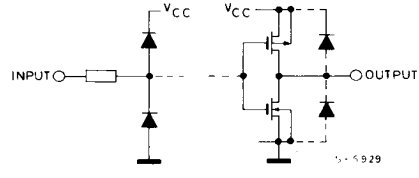
AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25°C$ 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5		—	7	12	—	15	—	18	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q)	4.5		—	26	40	—	50	—	60	ns
f_{MAX}	Maximum Clock Frequency	4.5		25	38	—	20	—	17	—	MHz
t_W	Minimum Pulse Width	4.5		—	13	25	—	32	—	38	ns
t_s	Minimum Set-up Time	4.5		—	6	15	—	19	—	23	ns
t_h	Minimum hold Time	4.5		—	—	0	—	0	—	0	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	4.5	$R_L = 1k\Omega$	—	27	42	—	53	—	63	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	4.5	$R_L = 1k\Omega$	—	22	32	—	40	—	48	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
C_{OUT}	Output Capacitance			—	10	—	—	—	—	—	pF
C_{PD} (*)	Power Dissipation Capacitance			—	60	—	—	—	—	—	pF

Note (*) C_{PD} is defined as the value of IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)
Average opeating current is: $I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per FLIP/FLOP)
And the C_{PD} when n circuits of FLIP/FLOP operate, can be gained by the following equation. C_{PD} (TOTAL) = 42 + 18•n (pF)

INPUT AND OUTPUT EQUIVALENT CIRCUIT



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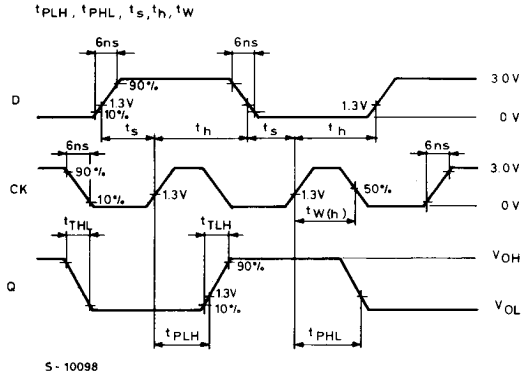
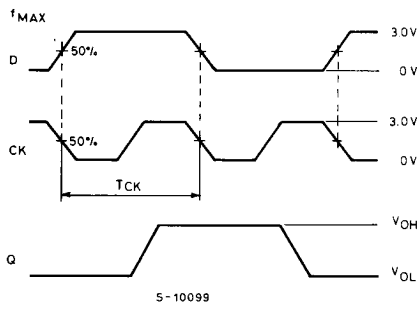
SWITCHING CHARACTERISTICS TEST WAVEFORM





Duty cycle of CK: 50%

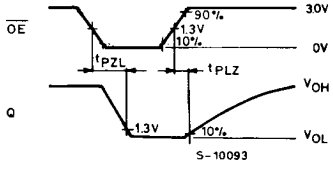
$$f_{MAX} = \frac{1}{T_{CK}}$$

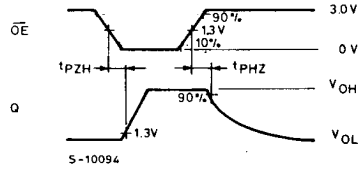
t_{PLZ}, t_{PZL}

The 1KΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line. All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{PHZ}, t_{PZH}

The 1KΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ inputs is held low.





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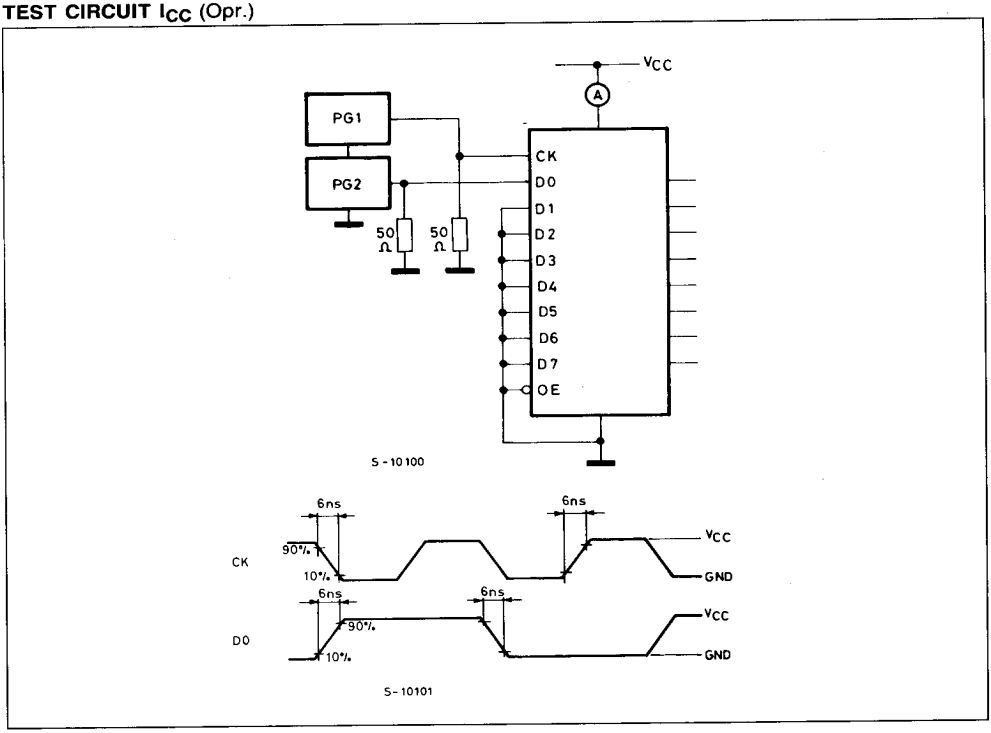
TEST CIRCUIT I_{CC} (Opr.)



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