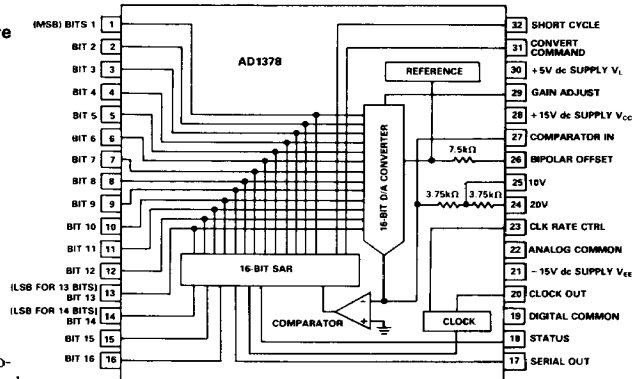


### FEATURES

**Complete 16-Bit Converter with Reference and Clock**  
 **$\pm 0.003\%$  Maximum Nonlinearity Over Temperature Available with MIL-STD-883 Screening**  
**Fast Conversion – 17  $\mu\text{s}$  Maximum (16 Bit)**  
**Short Cycle Capability**  
**Parallel and Serial Outputs**  
**Low Power: 800 mW Maximum**  
**Industry Standard Pin Out**  
**Specified Over Military Temperature Range**

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION

The AD1378 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock and laser-trimmed thin-film components. It is packaged in a compact 32-pin, ceramic DIP. The thin-film scaling resistors allow analog input ranges of  $\pm 2.5\text{ V}$ ,  $\pm 5\text{ V}$ ,  $\pm 10\text{ V}$ , 0 to  $+5\text{ V}$ , 0 to  $+10\text{ V}$ , and 0 to  $+20\text{ V}$ .

Important performance characteristics of the devices are maximum linearity error of  $\pm 0.003\%$  of FSR, and maximum 14-bit conversion time of 15  $\mu\text{s}$ . This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD1378 provides data in parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

### APPLICATIONS

The AD1378 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required. The device may be short cycled to achieve 14-bit conversions in 15  $\mu\text{s}$ .

### PRODUCT HIGHLIGHTS

1. The AD1378 provides 16-bit resolution with maximum linearity error less than  $\pm 0.003\%$  ( $\pm 0.006\%$  for S grade) at  $+25^\circ\text{C}$ .
2. Conversion time is 14  $\mu\text{s}$  typical to 14 bits with short cycle capability, and 16  $\mu\text{s}$  to 16 bits.
3. Two binary codes are available on the AD1378 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary twos complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary ICs used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.
5. The AD1378 includes an internal reference and clock, with external clock adjust pin, and a serial output.

# AD1378—SPECIFICATIONS (typical at $T_A = +25^\circ\text{C}$ , $V_S = \pm 15$ , $+5\text{ V}$ unless otherwise noted)

Model	AD1378SD	AD1378TD	Units
RESOLUTION	16 (max)	*	Bits
ANALOG INPUTS			
Voltage Ranges			
Bipolar	$\pm 2.5, \pm 5, \pm 10$	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	Volts
Impedance (Direct Input)			
0 to +5 V, $\pm 2.5\text{ V}$	1.88	*	k $\Omega$
0 to +10 V, $\pm 5.0\text{ V}$	3.75	*	k $\Omega$
0 to +20 V, $\pm 10\text{ V}$	7.50	*	k $\Omega$
DIGITAL INPUTS <sup>1</sup>			
Convert Command	Positive Pulse 50 ns Wide (min) Trailing Edge Initiates Conversion		
Logic Loading	1	*	LS TTL Load
TRANSFER CHARACTERISTICS <sup>2</sup>			
ACCURACY			
Gain Error	$\pm 0.05^3$ ( $\pm 0.1$ max)	*	%
Offset Error			
Unipolar	$\pm 0.05^3$ ( $\pm 0.1$ max)	*	% of FSR <sup>4</sup>
Bipolar	$\pm 0.05^3$ ( $\pm 0.2$ max)	*	% of FSR
Linearity Error (max)	$\pm 0.006$	$\pm 0.003$	% of FSR
Inherent Quantization Error	$\pm 1/2$	*	LSB
Differential Linearity Error	$\pm 0.003$	*	% of FSR
POWER SUPPLY SENSITIVITY			
$\pm 15\text{ V dc}$ ( $\pm 0.75\text{ V}$ )	0.001 (0.003 max)	*	% of FSR/% $\Delta V_S$
$+5\text{ V dc}$ ( $\pm 0.25\text{ V}$ )	0.001 (0.005 max)	*	% of FSR/% $\Delta V_S$
CONVERSION TIME <sup>3</sup>			
14 Bits	14 (15 max)	*	$\mu\text{s}$
16 Bits	16 (17 max)	*	$\mu\text{s}$
WARM-UP TIME	1	*	Minutes
DRIFT			
Gain	$\pm 15$ (max)	$\pm 5$ ( $\pm 15$ max)	ppm/ $^\circ\text{C}$
Offset			
Unipolar	$\pm 2$ ( $\pm 4$ max)	$\pm 2$ ( $\pm 4$ max)	ppm of FSR/ $^\circ\text{C}$
Bipolar	$\pm 10$ (max)	$\pm 3$ ( $\pm 10$ max)	ppm of FSR/ $^\circ\text{C}$
Linearity	$\pm 2$ (3 max)	$\pm 0.3$ (2 max)	ppm of FSR/ $^\circ\text{C}$
Guaranteed No Missing Code Temperature Range	$-55$ to $+125$ (13 Bits)	$-55$ to $+125$ (14 Bits)	$^\circ\text{C}$
DIGITAL OUTPUT <sup>1</sup>			
(All Codes Complementary)			
Parallel & Serial Output Codes <sup>6</sup>			
Unipolar	CSB	*	
Bipolar	COB, CTC <sup>7</sup>	*	LSTTL Loads
Output Drive	5	*	
Status	Logic "1" During Conversion	*	LSTTL Loads
Status Output Drive	5 (max)	*	
Internal Clock <sup>8</sup>			
Clock Output Drive	5 (max)	*	LSTTL Loads
Frequency	1040	*	kHz
POWER SUPPLY REQUIREMENTS			
Power Consumption	645 (800 max)	*	mW
Rated Voltage, Analog	$\pm 15 \pm 0.75$ (max)	*	V dc
Rated Voltage, Digital	$+5 \pm 0.25$ (max)	*	V dc
Supply Drain +15 V dc	+25 (max)	*	mA
Supply Drain -15 V dc	-40 (max)	*	mA
Supply Drain +5 V dc	+25 (max)	*	mA
TEMPERATURE RANGE			
Specification	$-55$ to $+125$	*	$^\circ\text{C}$
Storage	$-65$ to $+150$	*	$^\circ\text{C}$

## NOTES

<sup>1</sup>Logic "0" = 0.8 V, max. Logic "1" = 2.0 V, min for inputs. For digital outputs Logic "0" = +0.4 V max. Logic "1" = 2.7 V min.

<sup>2</sup>Tested on  $\pm 10\text{ V}$  and 0 to  $+10\text{ V}$  ranges.

<sup>3</sup>Adjustable to zero.

<sup>4</sup>Full-Scale Range.

<sup>5</sup>Conversion time may be shortened with "Short Cycle" set for lower resolution.

<sup>6</sup>CSB - Complementary Straight Binary. COB - Complementary Offset Binary. CTC - Complementary Twos Complement.

<sup>7</sup>CTC coding obtained by inverting MSB (Pin 1).

<sup>8</sup>With Pin 23, clock rate controls tied to digital ground.

\*Specifications same as AD1378SD.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS\***

Supply Voltage	±18 V
Logic Supply Voltage	+7 V
Analog Inputs (Pins 24 & 25)	±25 V
Digital Inputs	+5.5 V
Junction Temperature	+175°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

**THEORY OF OPERATION**

A 16-bit conversion A/D converter partitions the range of analog inputs into  $2^{16}$  discrete ranges or quanta. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of  $\pm 1/2$  LSB, associated with the resolution, in addition to the actual conversion errors.

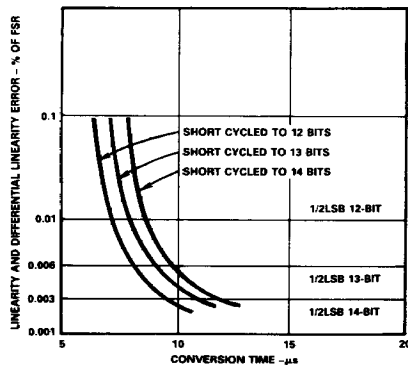


Figure 1. AD1378 Nonlinearity vs. Conversion Time

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at  $\pm 0.2\%$  FSR for gain and  $\pm 0.1\%$  FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 3 and 4. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The

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**ORDERING GUIDE**

Model	Max Linearity Error	Temperature Range	Package Option*
AD1378SD	0.006% FSR	-55°C to +125°C	Ceramic DH-32E
AD1378TD	0.003% FSR	-55°C to +125°C	Ceramic DH-32E

\*DH-32E = Bottom Brazed Ceramic DIP. For outline information see Package Information section.



linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 2).

Monotonic behavior requires that the differential linearity error be less than 1 LSB, however a monotonic converter can have missing codes; the AD1378 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

$\epsilon_G$  = Gain Drift Error (ppm/°C)

$\epsilon_O$  = Offset Drift Error (ppm of FSR/°C)

$\epsilon_L$  = Linearity Error (ppm of FSR/°C)

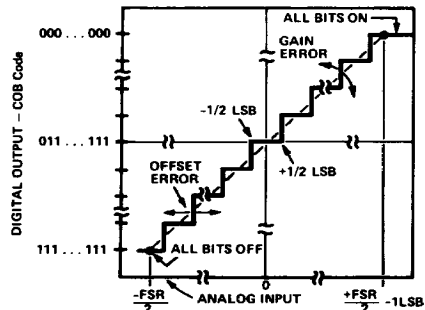


Figure 2. Transfer Characteristics for an Ideal Bipolar A/D

# AD1378

## DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD1378 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

## GAIN ADJUSTMENT

The gain adjust circuit consists of a 100-ppm/°C potentiometer connected across  $\pm V_S$  with its slider connected through a 300-k $\Omega$  resistor to the gain adjust Pin 29 as shown in Figure 3. If no external trim adjustment is desired, Pin 27 (offset adj) and Pin 29 (gain adj) may be left open.

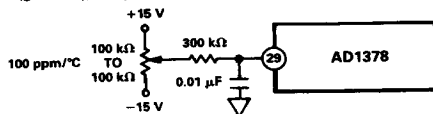


Figure 3. Gain Adjustment Circuit ( $\pm 0.15\%$  FSR)

## OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100-ppm/°C potentiometer connected across  $\pm V_S$  with its slider connected through a 1.8-M $\Omega$  resistor to Comparator Input Pin 27 for all ranges. As shown in Figure 4, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a  $-1200$ -ppm/°C tempco contributes a worst-case offset tempco of  $32 \text{ LSB}_{14} \times 61 \text{ ppm/LSB}_{14} \times 1200 \text{ ppm/°C} = 2.3 \text{ ppm/°C}$  of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than  $\pm 16 \text{ LSB}_{14}$ , use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

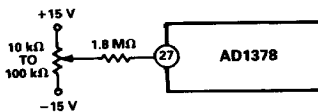


Figure 4. Offset Adjustment Circuit ( $\pm 0.3\%$  FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco  $< 100$  ppm/°C) are used, is shown in Figure 5.

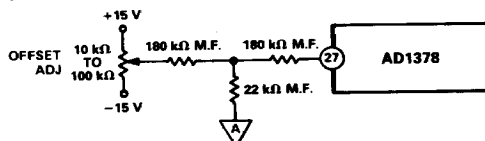


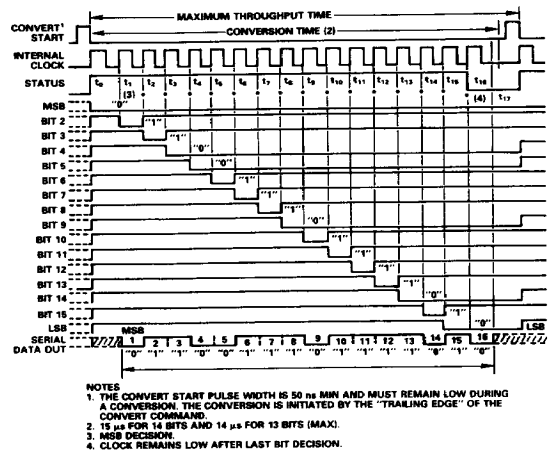
Figure 5. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to Pin 27 should be located close to this pin to keep the pin connection runs short. Comparator Input Pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common.

## TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time  $t_0$ ,  $B_1$  is reset and  $B_2 - B_{16}$  are set unconditionally. At  $t_1$  the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at  $t_{16}$ . The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.



- NOTES
1. THE CONVERT START PULSE WIDTH IS 50 ns MIN AND MUST REMAIN LOW DURING A CONVERSION; THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
  2. 15  $\mu$ s FOR 14 BITS AND 14  $\mu$ s FOR 13 BITS (MAX).
  3. MSB DECISION.
  4. CLOCK REMAINS LOW AFTER LAST BIT DECISION.

Figure 6. Timing Diagram (Binary Code 011001110111010)

**DIGITAL OUTPUT DATA**

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0 V and Logic "0" = 2.4 V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20 ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 7).

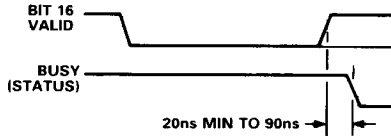


Figure 7. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120 ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 8. There are 17 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

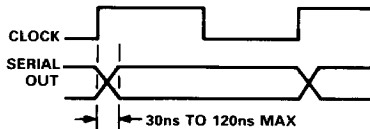


Figure 8. Clock High to Serial Out Valid

**Short Cycle Input:** A Short Cycle Input, Pin 32, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, Pin 32 is connected to Bit 11 output Pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 5). Short cycle connections and associated 8-, 10-, 12-, 13-, 14- and 15-bit conversion times are summarized in Table I, for a 933 kHz clock.

Resolution Bit	(%FSR)	Maximum Conversion Time (μs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	17.1	t <sub>16</sub>	N/C (Open)
15	0.003	16.1	t <sub>15</sub>	16
14	0.006	15.0	t <sub>14</sub>	15
13	0.012	13.9	t <sub>13</sub>	14
12	0.024	12.9	t <sub>12</sub>	13
10	0.100	10.7	t <sub>10</sub>	11
8	0.390	8.6	t <sub>8</sub>	9

Table I. Short Cycle Connections

**INPUT SCALING**

The AD1378 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

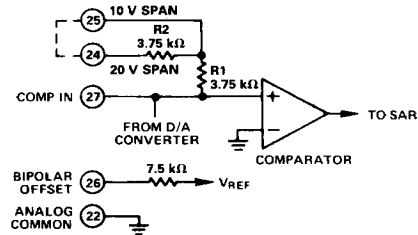


Figure 9. AD1378 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
± 10 V	COB	27	Input Signal	24
± 5 V	COB	27	Open	25
± 2.5 V	COB	27	Pin 27	25
0 V to +5 V	CSB	22	Pin 27	25
0 V to +10 V	CSB	22	Open	25
0 V to +20 V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table II. AD1378 Input Scaling Connections

Code Under Test			Low Side Transition Values				
MSB	LSB	Range	$\pm 10$ V	$\pm 5$ V	$\pm 2.5$ V	0 to +10 V	0 to +5 V
000 . . . 000*		+ Full Scale	+10 V -3/2 LSB	+ 5 V -3/2 LSB	+2.5 V -3/2 LSB	+10 V - 3/2 LSB	+5 V -3/2 LSB
011 . . . 111		Midscale	0-1/2 LSB	0-1/2 LSB	0-1/2 LSB	+5 V-1/2 LSB	+2.5 V-1/2 LSB
111 . . . 110		- Full Scale	-10 V +1/2 LSB	-5 V +1/2 LSB	-2.5 V +1/2 LSB	0 V +1/2 LSB	0 V +1/2 LSB

\*Voltages given are the nominal value for transition to the code specified.  
 Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		$\pm 10$ V	$\pm 5$ V	$\pm 2.5$ V	0 V to +10 V	0 V to +5 V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least FSR Significant (Bit LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV
	n = 13	2.44 mV	1.22 mV	0.61 mV	1.22 mV	0.61 mV
	n = 14	1.22 mV	0.61 mV	0.31 mV	0.61 mV	0.31 mV
	n = 15	0.61 mV	0.31 mV	0.15 mV	0.31 mV	0.15 mV

NOTES

- \*COB = Complementary Offset Binary.
- \*\*CTC = Complementary Twos Complement - achieved by using an inverter to complement the most significant bit to produce (MSB).
- \*\*\*CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

**0 to +10 V Range:** Set analog input to +1 LSB<sub>14</sub> = 0.00061 V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR - 2 LSB = + 9.99878 V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000 V; digital output code should be 01111111111111.

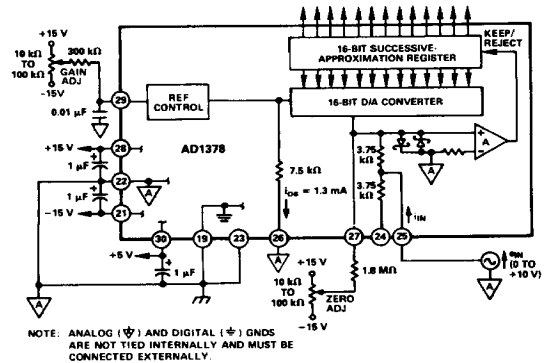


Figure 10. Analog and Power Connections for Unipolar 0 to +10 V Input Range

**-10 V to +10 V Range:** Set analog input to  $-9.99878$  V; adjust zero for 111111111110 digital output (complementary offset binary) code. Set analog input to  $9.99756$  V; adjust Gain for 0000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to  $0.00000$  V; digital output (complementary offset binary) code should be 011111111111.

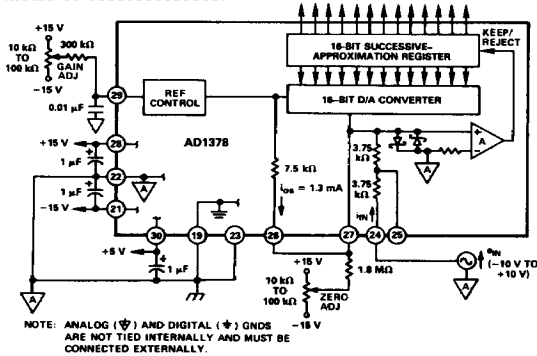


Figure 11. Analog and Power Connections for Bipolar  $-10$  V to  $+10$  V Input Range

**Other Ranges:** Representative digital coding for 0 to  $+10$ -V and  $-10$ -V to  $+10$ -V ranges is given above. Coding relationships and calibration points for 0 to  $+5$ -V,  $-2.5$ -V to  $+2.5$ -V and  $-5$ -V to  $+5$ -V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to  $+10$ -V and  $-10$ -V to  $+10$ -V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately  $\pm 1/2$  LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *Analog-Digital Conversion Handbook*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

### GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (Pins 19 and 22) must be tied together at one point for the AD1378 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD1378. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD1378 sup-

ply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD1378 supply terminals should be capacitively decoupled as close to the AD1378 as possible. A large value capacitor such as  $1 \mu\text{F}$  in parallel with a  $0.1 \mu\text{F}$  capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

### CLOCK RATE CONTROL

The AD1378 may be operated at faster conversion times by connecting the Clock Rate Control (Pin 23) to an external multitrans trim potentiometer (TCR  $< 100$  ppm/ $^{\circ}\text{C}$ ) as shown in Figures 12 and 13. The integral linearity and differential linearity errors will vary with speed as shown in Figure 1.

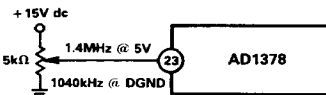


Figure 12. Clock Rate Control Circuit

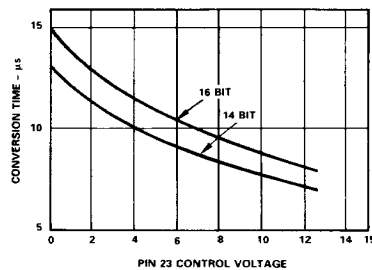


Figure 13. Conversion Time vs. Control Voltage

### HIGH RESOLUTION DATA ACQUISITION SYSTEM

The essential details of a high resolution data acquisition system using the AD386 and AD1378 are shown in Figure 14. Conversion is initiated by the falling edge of the CONVERT START pulse. This edge drives the AD1378's STATUS line high. The inverter then drives the AD386 into hold mode. STATUS remains high throughout the conversion and returns low once the conversion is completed. This allows the AD386 to reenter track mode.

This circuit can exhibit nonlinearities arising from transients produced at the A/D's input by the falling edge of CONVERT-START. This edge resets the A/D's internal DAC; the resulting transient depends on the SHA's present output voltage and the A/D's prior conversion result. In the circuit of Figure 14 the falling edge of CONVERT-START also places the SHA into hold mode (via the A/D's STATUS output), causing the reset transient to occur at the same moment as the SHA's track-and-

# AD1378

hold transition. Timing skews and capacitive coupling can cause some of the transient signal to add to the signal being acquired by the SHA, introducing nonlinearity.

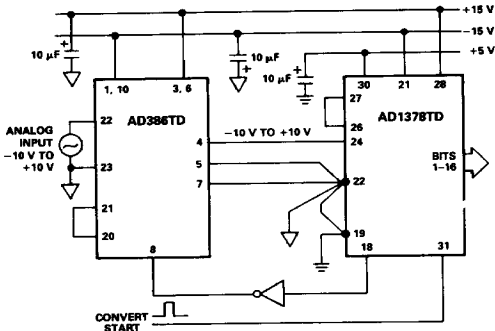


Figure 14. Basic Data Acquisition System Interconnections

A much safer approach is to add a flip flop as shown in Figure 15. The rising edge of CONVERT START places the T/H into

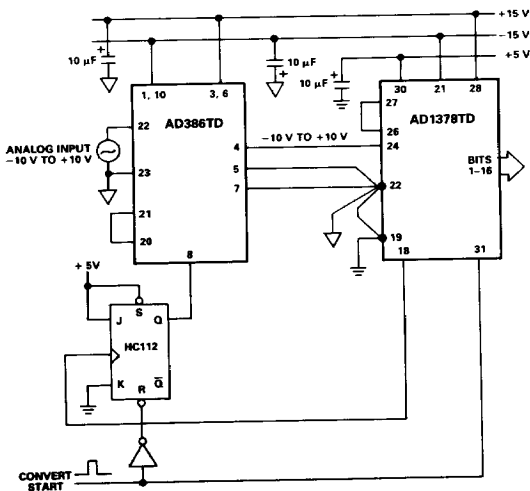


Figure 15. Improved Data Acquisition System

hold mode before the A/D reset transients begin. The falling edge of STATUS places the AD386 back into track mode. System throughput will be reduced if a long CONVERT START pulse is used. Throughput can be calculated from

$$\text{Throughput} = \frac{1}{T_{ACQ} + T_{CONV} + T_{CS}}$$

where  $T_{ACQ}$  is the T/H acquisition time,  $T_{CONV}$  is the time required for the A/D conversion, and  $T_{CS}$  is the duration of CONVERT START. The combination of the AD1378 and AD386 will provide greater than 50 kHz throughput over the full military temperature range. No significant T/H droop error will be introduced provided the width of CONVERT START is small compared with the A/D's conversion time.

### Using the AD1378 at Slower Conversion Times

The user may wish to run the AD1378 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock must consist of narrow negative-going clock pulses, as seen in Figure 16. The pulse must be a minimum of 100 ns wide but not greater than 700 ns. Having a rising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD1378 to function normally and complete a conversion after 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD1378 at slower conversion times.

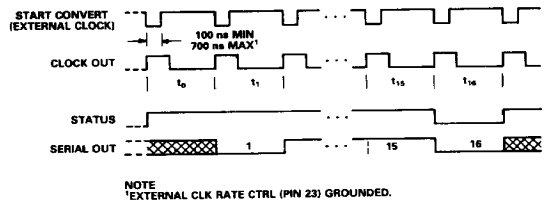


Figure 16. Timing Diagram for Use with an External Clock