

**AD7672**
**FEATURES**

**12-Bit Resolution and Accuracy**  
**Fast Conversion Time**  
 AD7672XX03 – 3 $\mu$ s  
 AD7672XX05 – 5 $\mu$ s  
 AD7672XX10 – 10 $\mu$ s  
**Unipolar or Bipolar Input Ranges**  
**Low Power: 110mW**  
**Fast Bus Access Times: 90ns**  
**Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages**

**GENERAL DESCRIPTION**

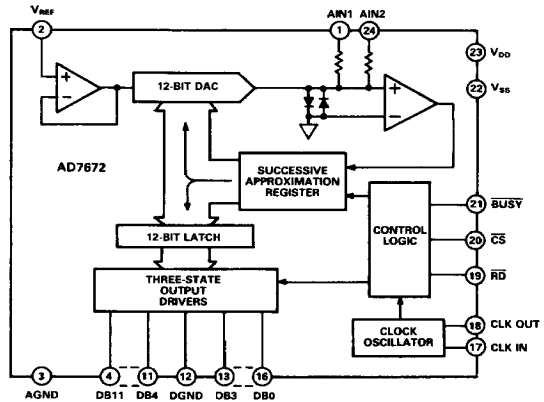
The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC<sup>2</sup>MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3 $\mu$ s while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and  $\pm$ 5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and -12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally -12V.

**FUNCTIONAL BLOCK DIAGRAM**


The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.

**PRODUCT HIGHLIGHTS**

1. Fast, 3 $\mu$ s, 5 $\mu$ s and 10 $\mu$ s conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC<sup>2</sup>MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or  $\pm$ 5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.

( $V_{DD} = 5V \pm 5\%$ ,  $V_{SS} = -12V \pm 10\%$ ,  $V_{REF} = -5V$  unless otherwise noted.  
 $f_{CLK}$ : 4MHz for AD7672XX03, 2.5MHz for AD7672XX05, 1.25MHz for AD7672XX10.  
 All Specifications  $T_{min}$  to  $T_{max}$  unless otherwise noted. Specifications apply to Slow Memory Mode.)

# AD7672—SPECIFICATIONS

Parameter	K Version <sup>1</sup>	L Version <sup>1</sup>	B Version <sup>1</sup>	C Version <sup>1</sup>	Units	Test Conditions/Comments
<b>ACCURACY<sup>2</sup></b>						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	±1/2	LSB max	Tested Range ±5V
$T_{min}$ to $T_{max}$	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
$T_{min}$ to $T_{max}$	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
$T_{min}$ to $T_{max}$	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: ±5V
$T_{min}$ to $T_{max}$	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: ±5V
$T_{min}$ to $T_{max}$	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
<b>ANALOG INPUT</b>						
Unipolar Input Current	3.5	3.5	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	±1.75	±1.75	mA max	Input Range: ±5V
<b>REFERENCE INPUT</b>						
$V_{REF}$ (For Specified Performance)	-5	-5	-5	-5	Volts	±1%
Input Reference Current	-3	-3	-3	-3	µA max	
<b>POWER SUPPLY REJECTION</b>						
$V_{DD}$ Only, (FS Change)	±1	±1	±1	±1	LSB typ	$V_{SS} = -12V$ , $V_{DD} = +4.75V$ to $+5.25V$
$V_{SS}$ Only, (FS Change)	±1	±1	±1	±1	LSB typ	$V_{DD} = +5V$ , $V_{SS} = -10.8V$ to $-13.2V$
<b>LOGIC INPUTS</b>						
$\overline{CS}$ , $\overline{RD}$ , CLK IN						
$V_{IN(L)}$ , Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	$V_{DD} = 5V \pm 5\%$
$V_{IN(H)}$ , Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
$C_{IN}^3$ , Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$ , $\overline{RD}$						
$I_{IN}$ , Input Current	±10	±10	±10	±10	µA max	$V_{IN} = 0$ to $V_{DD}$
CLK IN						
$I_{IN}$ , Input Current	±20	±20	±20	±20	µA max	$V_{IN} = 0$ to $V_{DD}$
<b>LOGIC OUTPUTS</b>						
DB11-DB0, $\overline{BUSY}$ , CLK OUT						
$V_{OL}$ , Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	$I_{SINK} = 1.6mA$
$V_{OH}$ , Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	$I_{SOURCE} = 200\mu A$
Floating-State Leakage Current						
DB11-DB0	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance <sup>3</sup>	15	15	15	15	pF max	
<b>CONVERSION TIME</b>						
AD7672XX03						Applies to K and B Grades Only
Synchronous Clock	3.125	-	3.125	-	µs max	$f_{CLK} = 4MHz$ . See Under
Asynchronous Clock	3/3.25	-	3/3.25	-	µs min/max	Control Inputs Synchronization
AD7672XX05						
Synchronous Clock	5	5	5	5	µs max	$f_{CLK} = 2.5MHz$
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	µs min/max	
AD7672XX10						
Synchronous Clock	10	10	10	10	µs max	$f_{CLK} = 1.25MHz$
Asynchronous Clock	9.6/10.4	9.6/10.4	9.6/10.4	9.6/10.4	µs min/max	
<b>POWER REQUIREMENTS</b>						
$V_{DD}$	+5	+5	+5	+5	VNOM	±5% for Specified Performance
$V_{SS}$	-12	-12	-12	-12	VNOM	±10% for Specified Performance
$I_{DD}^4$	7	7	7	7	mA max	$\overline{CS} = \overline{RD} = V_{DD}$ , $A_{IN1} = A_{IN2} = 5V$
$I_{SS}^4$	-12	-12	-12	-12	mA max	$\overline{CS} = \overline{RD} = V_{DD}$ , $A_{IN1} = A_{IN2} = 5V$
Power Dissipation	110	110	110	110	mW typ	
	179	179	179	179	mW max	

## NOTES

<sup>1</sup>Temperature range as follows: K, L Versions; 0 to +70°C.

B, C Versions; -25°C to +85°C.

<sup>2</sup> $V_{DD} = 5V$ ,  $V_{SS} = -12V$ , 1LSB - FS/4096

<sup>3</sup>Sample tested to ensure compliance.

<sup>4</sup>Power supply current is measured when AD7672 is inactive, i.e.,  $\overline{CS} = \overline{RD} = \overline{BUSY} = HIGH$ .

Specifications subject to change without notice.

Parameter	T Version <sup>1</sup>	U Version <sup>1</sup>	Units	Test Conditions/Comments
<b>ACCURACY<sup>2</sup></b>				
Resolution	12	12	Bits	
Integral Nonlinearity ( $\alpha$ + 25°C)	±1	±1/2	LSB max	Tested Range ±5V
$T_{min}$ to $T_{max}$	±1	±3/4	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error ( $\alpha$ + 25°C)	±5	±3	LSB max	
$T_{min}$ to $T_{max}$	±6	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
Unipolar Gain Error ( $\alpha$ + 25°C)	±5	±4	LSB max	Typical TC is 2ppm/°C
$T_{min}$ to $T_{max}$	±7	±6	LSB max	Input Range: 0 to 5V or 0 to 10V
Bipolar Zero Error ( $\alpha$ + 25°C)	±5	±3	LSB max	Typical TC is 2ppm/°C
$T_{min}$ to $T_{max}$	±6	±4	LSB max	Input Range: ±5V
Bipolar Gain Error ( $\alpha$ + 25°C)	±5	±4	LSB max	Typical TC is 2ppm/°C
$T_{min}$ to $T_{max}$	±7	±6	LSB max	Input Range: ±5V
				Typical TC is 2ppm/°C
<b>ANALOG INPUT</b>				
Unipolar Input Current	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	mA max	Input Range: ±5V
<b>REFERENCE INPUT</b>				
$V_{REF}$ (For Specified Performance)	-5	-5	Volts	±1%
Input Reference Current	-3	-3	μA max	
<b>POWER SUPPLY REJECTION</b>				
$V_{DD}$ Only, (FS Change)	±1	±1	LSB typ	$V_{SS} = -12V$ , $V_{DD} = +4.75V$ to $+5.25V$ $V_{DD} = +5V$ , $V_{SS} = -10.8V$ to $-13.2V$
$V_{SS}$ Only, (FS Change)	±1	±1	LSB typ	
<b>LOGIC INPUTS</b>				
$\overline{CS}$ , $\overline{RD}$ , CLK IN				
$V_{IN(L)}$ , Input Low Voltage	+0.8	+0.8	V max	$V_{DD} = 5V \pm 5\%$
$V_{IN(H)}$ , Input High Voltage	+2.4	+2.4	V min	
$C_{IN}^3$ , Input Capacitance	10	10	pF max	
$\overline{CS}$ , $\overline{RD}$				
$I_{IN}$ , Input Current	±10	±10	μA max	$V_{IN} = 0$ to $V_{DD}$
CLK IN				
$I_{IN}$ , Input Current	±20	±20	μA max	$V_{IN} = 0$ to $V_{DD}$
<b>LOGIC OUTPUTS</b>				
DB11-DB0, $\overline{BUSY}$ , CLK OUT				
$V_{OL}$ , Output Low Voltage	+0.4	+0.4	V max	$I_{SINK} = 1.6mA$ $I_{SOURCE} = 200\mu A$
$V_{OH}$ , Output High Voltage	+4.0	+4.0	V min	
Floating-State Leakage Current				
DB11-DB0	±10	±10	μA max	
Floating-State Output Capacitance <sup>3</sup>	15	15	pF max	
<b>CONVERSION TIME</b>				
<b>AD7672XX05</b>				
Synchronous Clock	5	5	μs max	$f_{CLK} = 2.5MHz$ . See Under Control Inputs Synchronization
Asynchronous Clock	4.8/5.2	4.8/5.2	μs min/max	
<b>AD7672XX10</b>				
Synchronous Clock	10	10	μs max	$f_{CLK} = 1.25MHz$
Asynchronous Clock	9.6/10.4	9.6/10.4	μs min/max	
<b>POWER REQUIREMENTS</b>				
$V_{DD}$	+5	+5	VNOM	±5% for Specified Performance ±10% for Specified Performance
$V_{SS}$	-12	-12	VNOM	
$I_{DD}^4$	7	7	mA max	$\overline{CS} = \overline{RD} = V_{DD}$ , $A_{IN1} = A_{IN2} = 5V$ $\overline{CS} = \overline{RD} = V_{DD}$ , $A_{IN1} = A_{IN2} = 5V$
$I_{SS}^4$	-12	-12	mA max	
Power Dissipation	110	110	mW typ	
	179	179	mW max	

## NOTES

<sup>1</sup>Temperature range as follows: T, U Versions; -55°C to +125°C.<sup>2</sup> $V_{DD} = 5V$ ,  $V_{SS} = -12V$ , 1LSB = FS/4096<sup>3</sup>Sample tested to ensure compliance.<sup>4</sup>Power supply current is measured when AD7672 is inactive, i.e.,  $\overline{CS} = \overline{RD} = \overline{BUSY} = HIGH$ .

Specifications subject to change without notice.

# AD7672

## TIMING CHARACTERISTICS<sup>1</sup> ( $V_{DD}=5V, V_{SS}=-12V$ )

Parameter	Limit at +25°C (All Grades)	Limit at $T_{min}, T_{max}$ (K, L, B, C Grades)	Limit at $T_{min}, T_{max}$ (T, U Grades)	Units	Conditions/Comments
$t_1$	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
$t_2$	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
$t_3^2$	90	110	120	ns max	Data Access Time after $\overline{RD}$ , $C_L = 20pF$
	125	150	170	ns max	Data Access Time after $\overline{RD}$ , $C_L = 100pF$
$t_4$	$t_3$	$t_3$	$t_3$	ns min	$\overline{RD}$ Pulse Width
$t_5$	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
$t_6^2$	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
$t_7^3$	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
$t_8$	200	200	200	ns min	Delay Between Successive Read Operations

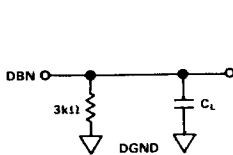
### NOTES

<sup>1</sup>Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with  $t_r = t_f = 5ns$  (10% to 90% of +5V) and timed from a voltage level of 1.6V.

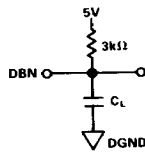
<sup>2</sup> $t_3$  and  $t_6$  are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

<sup>3</sup> $t_7$  is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

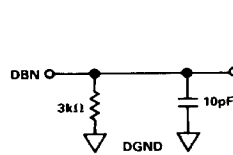


a. High-Z to  $V_{OH}$  ( $t_3$ ) and  $V_{OL}$  to  $V_{OH}$  ( $t_6$ )

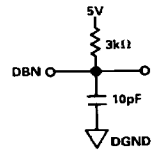


b. High-Z to  $V_{OL}$  ( $t_3$ ) and  $V_{OH}$  to  $V_{OL}$  ( $t_6$ )

Figure 1. Load Circuits for Access Time



a.  $V_{OH}$  to High-Z



b.  $V_{OL}$  to High-Z

Figure 2. Load Circuits for Output Float Delay

### ABSOLUTE MAXIMUM RATINGS\*

( $T_A = +25^\circ C$  unless otherwise noted)

$V_{DD}$ to DGND	-0.3V to +7V
$V_{SS}$ to DGND	+0.3V to -17V
AGND to DGND	-0.3V to $V_{DD} + 0.3V$
AIN1, AIN2 to AGND	-15V to +15V
$V_{REF}$ to AGND	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Digital Input Voltage to DGND (CLK IN, $\overline{CS}$ , $\overline{RD}$ )	-0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to DGND (DB11-DB0, $\overline{BUSY}$ , CLK OUT)	-0.3V to $V_{DD} + 0.3V$

### Operating Temperature Range

K, L	0 to +70°C
B, C	-25°C to +85°C
T, U	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

\*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



## TERMINOLOGY

**UNIPOLAR OFFSET ERROR**

The ideal first code transition should occur when the analog input is 1/2LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

**BIPOLAR ZERO ERROR**

The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000) for the  $\pm 5V$  range should occur when the analog input is 1/2LSB below AGND. Bipolar zero error is the deviation

of the actual transition from that point.

**GAIN ERROR**

The ideal difference between the first code transition and last code transition is FS - 2LSBs. The Gain error is defined as the deviation between this ideal difference and the measured difference. Ideal FS corresponds to 5V for the unipolar 0 to 5V range and 10V for both the unipolar 0 to 10V and bipolar  $\pm 5V$  ranges.

## ORDERING GUIDE

Model <sup>1,2</sup>	Conversion Time	Temperature Range	Accuracy Grade	Package Option <sup>3</sup>
AD7672KN03	3 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	N-24
AD7672BQ03	3 $\mu$ s	-25°C to +85°C	$\pm 1$ LSB	Q-24
AD7672KP03	3 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	P-28A
AD7672BE03	3 $\mu$ s	-25°C to +85°C	$\pm 1$ LSB	E-28A
AD7672KN05	5 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	N-24
AD7672BQ05	5 $\mu$ s	-25°C to +85°C	$\pm 1$ LSB	Q-24
AD7672TQ05	5 $\mu$ s	-55°C to +125°C	$\pm 1$ LSB	Q-24
AD7672LN05	5 $\mu$ s	0°C to +70°C	$\pm 1/2$ LSB	N-24
AD7672CQ05	5 $\mu$ s	-25°C to +85°C	$\pm 1/2$ LSB	Q-24
AD7672UQ05	5 $\mu$ s	-55°C to +125°C	$\pm 1/2$ LSB	Q-24
AD7672KP05	5 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	P-28A
AD7672TE05	5 $\mu$ s	-55°C to +125°C	$\pm 1$ LSB	E-28A
AD7672LP05	5 $\mu$ s	0°C to +70°C	$\pm 1/2$ LSB	P-28A
AD7672UE05	5 $\mu$ s	-55°C to +125°C	$\pm 1/2$ LSB	E-28A
AD7672KN10	10 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	N-24
AD7672BQ10	10 $\mu$ s	-25°C to +85°C	$\pm 1$ LSB	Q-24
AD7672TQ10	10 $\mu$ s	-55°C to +125°C	$\pm 1$ LSB	Q-24
AD7672LN10	10 $\mu$ s	0°C to +70°C	$\pm 1/2$ LSB	N-24
AD7672CQ10	10 $\mu$ s	-25°C to +85°C	$\pm 1/2$ LSB	Q-24
AD7672UQ10	10 $\mu$ s	-55°C to +125°C	$\pm 1/2$ LSB	Q-24
AD7672KP10	10 $\mu$ s	0°C to +70°C	$\pm 1$ LSB	P-28A
AD7672TE10	10 $\mu$ s	-55°C to +125°C	$\pm 1$ LSB	E-28A
AD7672LP10	10 $\mu$ s	0°C to +70°C	$\pm 1/2$ LSB	P-28A
AD7672UE10	10 $\mu$ s	-55°C to +125°C	$\pm 1/2$ LSB	E-28A

## NOTES

<sup>1</sup>Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.

<sup>2</sup>To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.

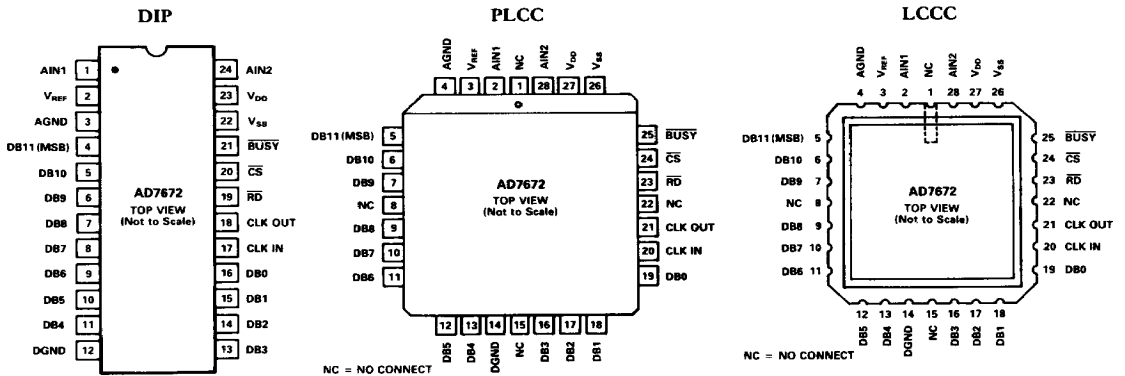
<sup>3</sup>D = Ceramic DIP; E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

# AD7672

## DIP PIN FUNCTION DESCRIPTION

DIP Pin No.	Mnemonic	Description
1	AIN1	Analog Input.
2	V <sub>REF</sub>	Voltage Reference Input. The AD7672 is specified with V <sub>REF</sub> = -5V.
3	AGND	Analog Ground.
4 . . . 11	DB11 . . . DB4	Three-state data outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low. DB11 is the most significant bit (MSB).
13 . . . 16	DB3 . . . DB0	
12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description.
19	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion.
20	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion.
21	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
22	V <sub>SS</sub>	Negative Supply, -12V.
23	V <sub>DD</sub>	Positive Supply, +5V.
24	AIN2	Analog Input.

## PIN CONFIGURATIONS



### OPERATING FROM A NEGATIVE SUPPLY GREATER THAN $-12\text{V}$

The AD7672 is designed to operate with a  $V_{SS}$  input of  $-12\text{V} \pm 10\%$ . In applications where the negative supply is greater than  $-12\text{V}$ , then a Zener diode in series with  $V_{SS}$  can be used to reduce the supply. The Zener diode should have a dynamic impedance of not greater than  $40\Omega$ . An example is given in Figure 3. The diode has a Zener voltage of  $3\text{V}$ , which makes it suitable for a negative supply of  $-15\text{V} \pm 7\%$ .

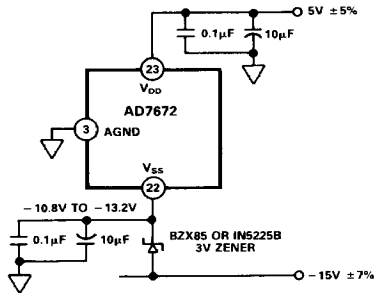


Figure 3. Operation from Nominal Power Supplies of  $5\text{V}$  and  $-15\text{V}$

### CONVERTER DETAILS

Conversion start is controlled by the  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the analog inputs (AIN1 & AIN2) connect to the comparator input via  $5\text{k}\Omega$  resistors. The DAC which has  $2.5\text{k}\Omega$  output impedance connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog inputs. The MSB decision is made  $80\text{ns}$  (typically) after the second falling edge of  $\text{CLK IN}$  following a conversion start (see Figure 5). Similarly, the succeeding bit decisions are made approximately  $80\text{ns}$  after a  $\text{CLK IN}$  falling edge until conversion

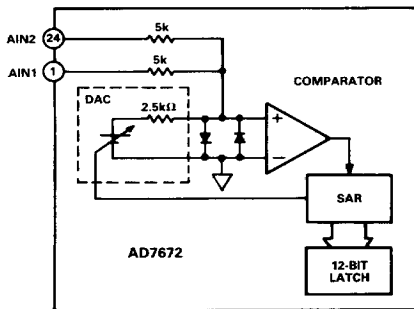


Figure 4. AD7672 AIN Input

is finished. At the end of conversion, the DAC output current balances the current from the analog inputs. The SAR contents (12-bit data word) which represent the analog input signal are loaded into a 12-bit latch.

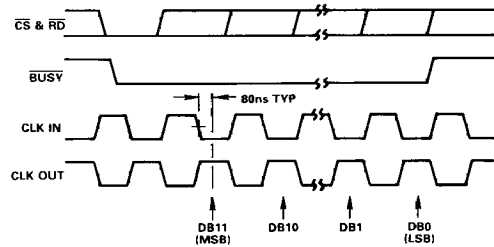


Figure 5. Operating Waveforms Using an External Clock Source for  $\text{CLK IN}$

### CONTROL INPUTS SYNCHRONIZATION

In applications where the  $\overline{\text{RD}}$  control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13  $\text{CLK IN}$  periods. This is because the ADC waits for the first falling  $\text{CLK IN}$  edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion,  $\overline{\text{RD}}$  must go low on either the rising edge of  $\text{CLK IN}$  or the falling edge of  $\text{CLK OUT}$ . This ensures a fixed conversion time that is 12.5 times the  $\text{CLK IN}$  period.

### DRIVING THE ANALOG INPUTS

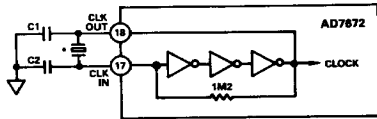
During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the  $\text{CLK IN}$  frequency (i.e.,  $4\text{MHz}$  when  $\text{CLK IN} = 4\text{MHz}$ ). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample and hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically  $11\text{mV}$  with a  $200\text{ns}$  settling time.

Suitable devices capable of driving the AD7672 analog inputs are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

### INTERNAL CLOCK OPERATION

Figure 6 shows the AD7672 internal clock circuit. A crystal or ceramic resonator may be connected between  $\text{CLK IN}$  (Pin 17) and  $\text{CLK OUT}$  (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/ceramic resonator may be omitted and an external clock source may be connected to  $\text{CLK IN}$ . For an external clock the mark/space ratio must be 50/50. An inverted  $\text{CLK IN}$  will appear at the  $\text{CLK OUT}$  pin as shown in the operating waveforms of Figure 5.

# AD7672



**NOTES**  
 AD7672XK03 - 4MHz CRYSTAL/CERAMIC RESONATOR  
 AD7672XK06 - 2.5MHz CRYSTAL/CERAMIC RESONATOR  
 AD7672XK10 - 1.25MHz CRYSTAL/CERAMIC RESONATOR  
 C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 6. AD7672 Internal Clock Circuit

## ANALOG INPUT RANGES

The AD7672 provides three user selectable analog input ranges; 0 to +5V, 0 to +10V and ±5V. Figure 7 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

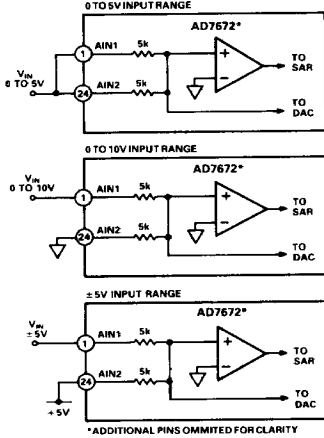


Figure 7. Analog Input Range Configurations

## UNIPOLAR OPERATION

Figure 8 shows how to configure an AD584 to produce a reference voltage of -5V for unipolar operation.

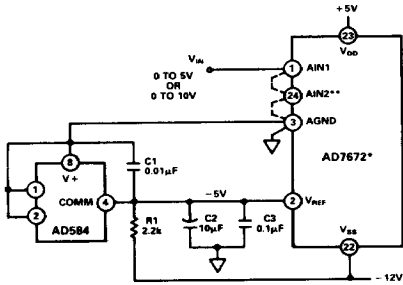


Figure 8. Unipolar Operation Using the AD584 as a Reference

The ideal input/output characteristic is shown in Figure 9. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs . . . FS - 3/2 LSBs). The output code is natural binary with 1LSB = FS/4096. FS is either +5V or +10V depending on the analog inputs configuration.

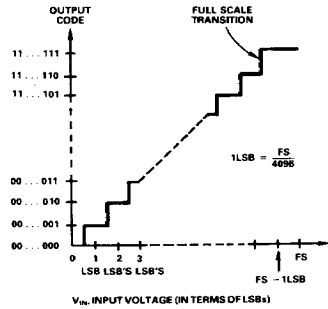


Figure 9. AD7672 Ideal Input/Output Transfer Characteristic for Unipolar Operation.

## OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog input signal is quantized, digitally processed and recreated using a DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important consideration in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

## UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 10). For zero offset error apply a voltage equal to 1/2LSB at  $V_{IN}$  and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

- 0 to +5V Range: 1/2LSB = 0.61mV
- 0 to +10V Range: 1/2LSB = 1.22mV

For zero full-scale error apply an analog input voltage equal to FS-3/2LSBs (last code transition) at  $V_{IN}$  and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

- 0 to +5V Range: FS-3/2LSBs = 4.99817
- 0 to +10V Range: FS-3/2LSBs = 9.99634

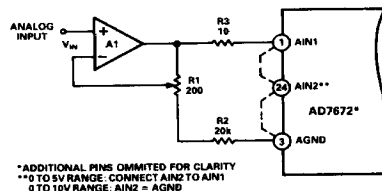


Figure 10. Unipolar Operation with Gain Error Adjust



**BIPOLAR OPERATION**

Bipolar operation is achieved by providing a +10V span at the AIN1 input which is offset to  $\pm 5V$  by applying +5V at the AIN2 input. This requires two reference voltages; -5V for the  $V_{REF}$  input and +5V for the AIN2 input. Figure 11 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. Alternatively, a convenient solution is to use the AD588 voltage reference as in Figure 12. This device generates the required  $\pm 5V$  with a minimum of additional components. It also offers excellent temperature stability with voltage drifts as low as 1.5ppm/°C.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 13. The LSB size is  $(10/4096)V = 2.44mV$ .

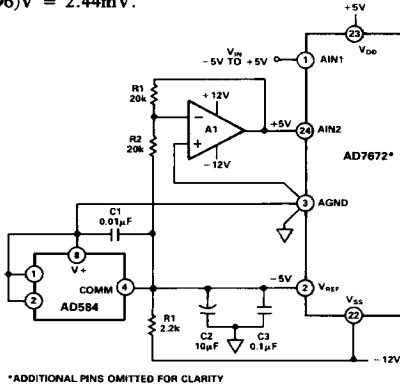


Figure 11. Bipolar Operation Using an AD584 and an AD711 Op Amp

**BIPOLAR OFFSET AND GAIN ADJUSTMENT**

In applications where absolute accuracy is important then offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the AIN1 or the AIN2 input when the analog input is at  $-FS/2 + 1/2LSB$ . This can be achieved by adjusting the offset of an external amplifier used to drive either of these analog inputs. Alternatively the AD588 voltage reference contains a balance control input which can be used to trim the offset to zero. An additional potentiometer (R2 in Figure 14) is required. The trim procedure is as follows:

Apply  $-4.99878V (-FS/2 + 1/2LSB)$  at  $V_{IN}$  and adjust R2 until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be adjusted at either the last positive code transition or the mid-scale transition (bipolar zero error adjust). Adjusting the positive end of the transfer function is in keeping with more conventional ADC calibration techniques where the user fixes the two end points as in the unipolar case. Bipolar zero adjustment is required in some applications (e.g., motor control) where the user must be guaranteed that the 0111 1111 1111 to 1000 0000 0000 transition occurs exactly when the analog input is  $1/2LSB$  below AGND. The trim procedures for both cases are as follows. (See Figure 14.)

**Last Code Transition Adjust**

Apply a voltage of 4.99634 volts ( $FS/2 - 3/2LSBs$ ) at  $V_{IN}$ . Adjust R5 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

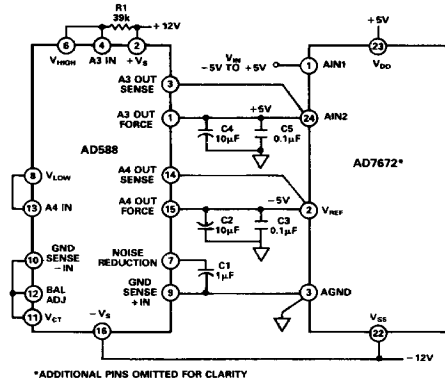


Figure 12. Bipolar Operation Using an AD588 Voltage Reference

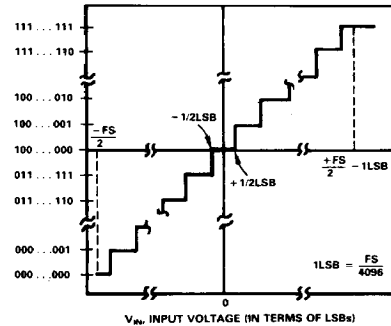


Figure 13. Ideal Input/Output Transfer Characteristic for Bipolar Operation

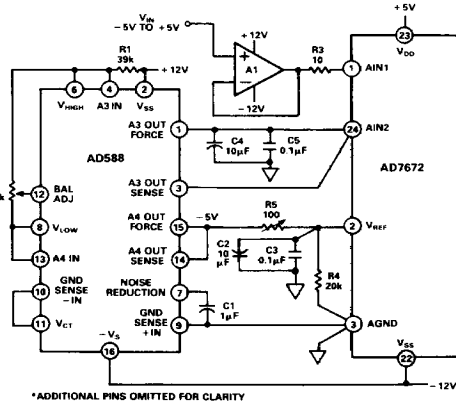


Figure 14. Bipolar Operation with Offset and Gain Error Adjust

**Bipolar Zero Error Adjust**

Apply a voltage of  $-1.22mV$  at  $V_{IN}$  and adjust R5 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

# AD7672

## TIMING AND CONTROL

Conversion start and data read operations are controlled by two of the AD7672 digital inputs;  $\overline{CS}$  and  $\overline{RD}$ . Figure 15 shows the equivalent logic circuit of these inputs. A high-to-low logic transition on  $\overline{CS}$  and  $\overline{RD}$  initiates a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the  $\overline{BUSY}$  output, and this is low while conversion is in progress.

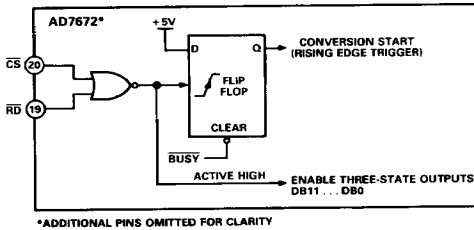


Figure 15. Internal Logic for Control Inputs  $\overline{CS}$  and  $\overline{RD}$

There are two modes of operation as outlined by the timing diagrams of Figures 16 and 17. Slow Memory Mode is designed for microprocessors that can be driven into a WAIT state, a READ operation brings  $\overline{CS}$  and  $\overline{RD}$  low, which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode, which does not require microprocessor WAIT states. A READ operation brings  $\overline{CS}$  and  $\overline{RD}$  low which initiates a conversion and reads the previous conversion result. The data format for both modes is designed for parallel interfacing.

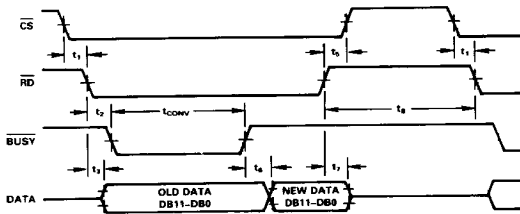


Figure 16. Slow Memory Mode Timing Diagram

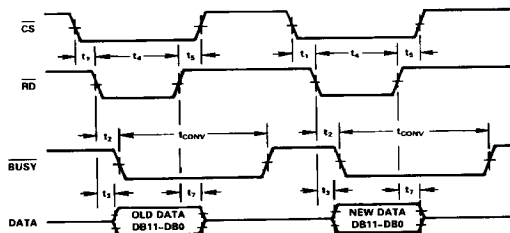


Figure 17. ROM Mode Timing Diagram

## SLOW MEMORY MODE

Figure 16 shows the timing diagram for Slow Memory Mode.  $\overline{CS}$  and  $\overline{RD}$  going low triggers a conversion and the AD7672 acknowledges by taking  $\overline{BUSY}$  low. Data from the previous conversion appears on the three-state data outputs.  $\overline{BUSY}$  returns high at the end of conversion when the output latches have been updated and the conversion result is placed on the output data bus.

## ROM MODE

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion are available on the data outputs while  $\overline{CS}$  and  $\overline{RD}$  are low. This data may be disregarded if not required. A second READ operation reads the new data and starts another conversion. A delay at least as long as the AD7672 conversion time must be allowed between READ operations.

## MICROPROCESSOR INTERFACING

The AD7672 is designed to interface to microprocessors as a memory mapped device. The  $\overline{CS}$  and  $\overline{RD}$  inputs are common control inputs to all peripheral memory interfacing.

## MC68000 MICROPROCESSOR

Figure 18 shows a typical interface for the MC68000. The AD7672 is operating in the Slow Memory Mode. Assuming the AD7672 is located at address C000 then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

**Move.W \$C000,D0**

At the beginning of the instruction cycle when the ADC address is selected,  $\overline{BUSY}$  and  $\overline{CS}$  assert  $\overline{DTACK}$ , so that the 68000 is forced into a WAIT state. At the end of conversion  $\overline{BUSY}$  returns high and the conversion result is placed in the D0 register of the UP.

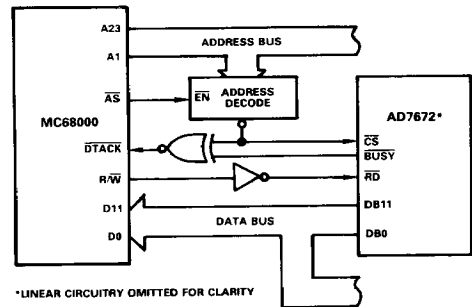


Figure 18. AD7672 - MC68000 Interface

**8085A, Z-80 MICROPROCESSORS**

Figure 19 shows an AD7672 interface for the Z-80 and 8085A. The AD7672 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the Figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. The following LOAD instruction starts a conversion and reads the conversion result into the HL register pair.

For the 8085A LHL (B000)  
 For the Z-80 LDHL (B000)

This is a two byte read instruction. During the first read operation,  $\overline{BUSY}$  forces the microprocessor to wait for the AD7672 conversion. At the end of conversion the low byte (DB7-DB0) is loaded into the HL register pair and the high byte (DB11-DB8) is latched into a 74HC374. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

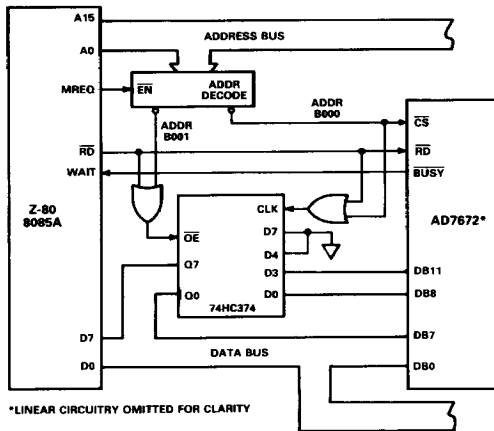


Figure 19. AD7672 - 8085A/Z80 Interface

**IBM PC\* COMPUTER**

The -12V power supply operation of the AD7672 makes it an ideal choice for the IBM PC. A typical interface is shown in Figure 20. The AD7672 is configured in the ROM mode. Two addresses are required to read the 12-bit ADC data over the 8-bit data bus. An I/O read instruction to the ADC address (B000) starts a conversion and reads the low data byte (DB7-DB0). This data is from the previous conversion. The high byte (DB11-DB8) may be read with a similar I/O instruction to the 74HC374 latch (address B001). Alternatively the up-to-date data may be read at the end of conversion. The AD7672  $\overline{BUSY}$  may be used to interrupt the IBM PC as shown in Figure 20. The data is then read with two I/O instructions as before. Note a read instruction to the ADC should not be attempted while conversion is in progress.

\*IBM PC is a trademark of International Business Machines Corp.

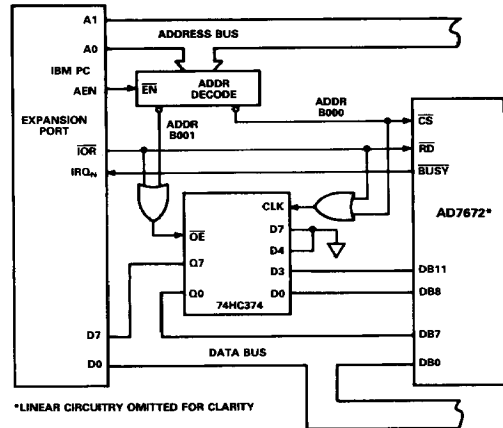


Figure 20. AD7672 - IBM PC Interface

**ADSP-2100 DIGITAL SIGNAL PROCESSOR**

The ADSP-2100 like other digital signal processors requires very fast data access times beyond the capabilities of the AD7672. This problem is easily overcome by inserting 74HC374 latches in the data bus as in Figure 21. Again for this interface a single instruction is sufficient to read the AD7672 conversion result.

MRO = DM (ADC ADDRESS)

This instruction initiates a conversion and reads the previous conversion result into the MRO register.  $\overline{CS}$  and  $\overline{RD}$  are gated so that they remain low for the duration of the conversion. Note that no WAIT states are inserted even though the AD7672 is configured for a Slow Memory mode. At the end of conversion,  $\overline{BUSY}$  going high latches the new result into the 74HC374 latches. An RC delay is inserted to compensate for the data setup time after  $\overline{BUSY}$  ( $t_s$ ).

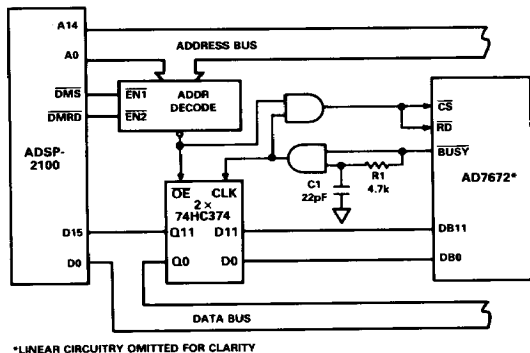


Figure 21. AD7672 - ADSP-2100 Interface

# AD7672

## TMS32010 MICROCOMPUTER

Figure 22 shows an AD7672-TMS32010 interface. The AD7672 is operating in the ROM mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The AD7672 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into the accumulator and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

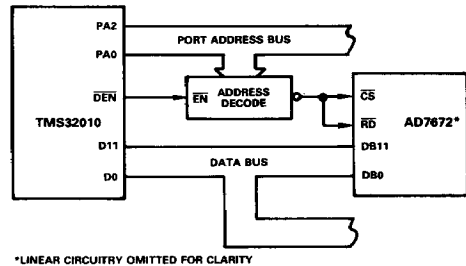


Figure 22. AD7672 - TMS32010 Interface

## APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. For 12-bit performance the AD7672's comparator is required to make bit decisions to an accuracy of 0.61mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

## LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 3 (AGND) or as close as possible to the AD7672 as shown in Figure 23. Connect all other grounds and Pin 12 (AD7672 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths, while guarding the analog circuitry from digital noise. Keep analog and digital grounds separate and only join them at the AD7672 AGND pin.

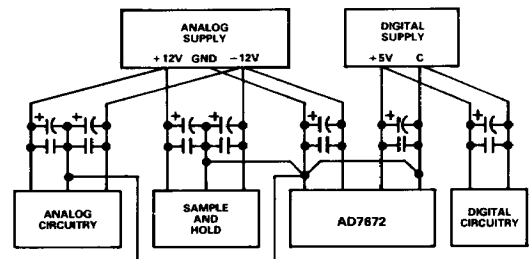


Figure 23. Power Supply Grounding Practice

**NOISE:** Keep the input signal leads to AIN and signal return leads from AGND (Pin3) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

Microprocessor applications generate noisy environments, making 12-bit performance difficult to achieve, especially when the ADC is connected to a continuously active bus. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7672 data bus.