ANALOG DEVICES

LC²MOS
16-Bit, High Speed Sampling ADCs
AD7884/AD7885

FEATURES
Monolithic Construction
Fast Conversion: 5.3 µs
High Throughput: 166 kSPS
Low Power: 250 mW

APPLICATIONS
Automatic Test Equipment
Medical Instrumentation
Industrial Control
Data Acquisition Systems
Robotics

GENERAL DESCRIPTION

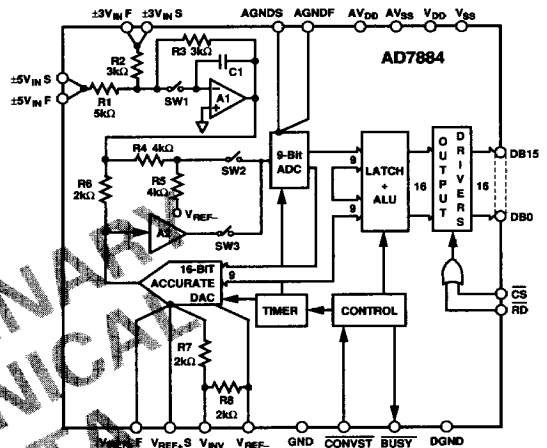
The AD7884/AD7885 is a 16-bit monolithic analog-to-digital converter with internal sample-and-hold and a conversion time of 5.3 µsec. The maximum throughput rate is 166 kSPS. It uses a two pass flash architecture to achieve this speed. Two input ranges are available: ±5 V and ±3 V. Conversion is initiated by the $\overline{\text{CONVST}}$ signal. The result can be read into a microprocessor using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs on the device. The AD7884 has a 16-bit parallel reading structure while the AD7885 has a byte reading structure. The conversion result is in 2s complement code.

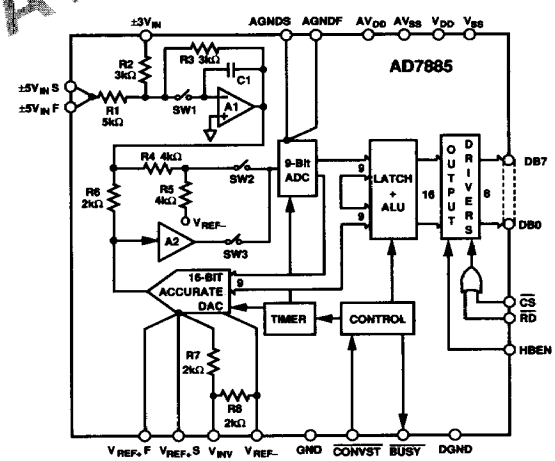
The AD7884/AD7885 has its own internal oscillator which controls conversion. It runs from ±5 V supplies and needs a V_{REF+} of +3 V.

The AD7884 is available in 40-pin plastic and cerdip packages and in a 44-pin PLCC package.

The AD7885 is available in 28-pin plastic and cerdip packages and in a 28-pin PLCC package.

FUNCTIONAL BLOCK DIAGRAMS





AD7884/AD7885—SPECIFICATIONS[1, 2]

(V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, V_{REF+}S = +3 V; AGND = DGND = GND = 0 V; f_{SAMPLE} = 166 kHz. All specifications T_{MIN} to T_{MAX}, unless otherwise noted).

Parameter	A Version[1, 2]	B, T Versions[1, 2]	Units	Test Conditions/Comments
DC ACCURACY				
Resolution	16	16	Bits	
Minimum Resolution for Which No Missing Codes Are Guaranteed	16	16	Bits	
Integral Nonlinearity		±0.003	% FSR max	
Differential Nonlinearity		±0.0015	% FSR max	
Positive Gain Error		±0.01	% FSR max	
Gain TC[3]		±2	ppm FSR/°C typ	
Bipolar Zero Error	±0.025	±0.01	% FSR max	
Bipolar Zero TC[3]		±2	ppm FSR/°C typ	
Negative Gain Error		±0.01	% FSR max	
Offset TC[3]		±2	ppm FSR/°C typ	
Noise	120	120	μV rms typ	78 μV rms typical in ±3 V Input Range
DYNAMIC PERFORMANCE				
Signal to (Noise + Distortion) Ratio	88	88	dB min	Input Signal: ±5 V, 1 kHz Sine Wave
	28	28	dB min	Input Signal: ±5 mV, 1 kHz Sine Wave
	82	82	dB min	Input Signal: ±5 V, 25 kHz Sine Wave
Total Harmonic Distortion	−94	−94	dB max	Input Signal: ±5 V, 1 kHz Sine Wave
	−83	−83	dB max	Input Signal: ±5 V, 25 kHz Sine Wave
Peak Harmonic or Spurious Noise	−92	−92	dB max	Input Signal: ±5 V, 25 kHz Sine Wave
Intermodulation Distortion (IMD)				
2nd Order Terms	−92	−92	dB max	f_A = 24.5 kHz, f_B = 25 kHz, f_{SAMPLE} = 166 kHz
3rd Order Terms	−92	−92	dB max	f_A = 24.5 kHz, f_B = 25 kHz, f_{SAMPLE} = 166 kHz
CONVERSION TIME				
Conversion Time	5.3	5.3	μs max	
Acquisition Time	1.5	1.5	μs min	
Throughput Rate	166	166	kSPS max	There is an overlap between conversion and acquisition.
ANALOG INPUT				
Voltage Range	±5	±5	Volts	
	±3	±3	Volts	
Input Current	±2	±2	mA max	
REFERENCE INPUT				
Reference Input Current	3	3	mA max	V_{REF} + S = +3 V
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V± 5%
Input Current, I_{IN}	±10	±10	μA max	Input Level = 0 V to V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB15–DB0				
Floating-State Leakage Current	10	10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	V nom	±5% for Specified Performance
I_{DD}	30	30	mA max	Typically 25 mA
I_{SS}	30	30	mA max	Typically 25 mA
Power Supply Rejection Ratio				
$\Delta Gain/\Delta V_{DD}$	86	86	dB typ	
$\Delta Gain/\Delta V_{SS}$	86	86	dB typ	
Power Dissipation	300	300	mW max	Typically 250 mW

NOTES
[1]Temperature Ranges are as follows: A, B Versions: −40°C to +85°C; T Version: −55°C to +125°C.
[2]V_{IN} = ±5 V.
[3]Sample tested to ensure compliance.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = GND = 0 V. See Figures 2, 3, 4 and 5.)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (A, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_1	50	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	100	100	100	ns min	$\overline{CONVST}$ to $\overline{BUSY}$ Low Delay
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_4	60	60	75	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	57	57	70	ns max	Data Access Time after $\overline{RD}$
t_7[3]	5	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	50	50	ns max	
t_8	40	40	40	ns min	New Data Valid before Rising Edge of $\overline{BUSY}$
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_{10}	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{11}	60	60	75	ns min	HBEN Low Pulse Duration
t_{12}	60	60	75	ns min	HBEN High Pulse Duration
t_{13}	40	40	40	ns max	Propagation Delay from HBEN Falling to Data Valid
t_{14}	40	40	40	ns max	Propagation Delay from HBEN Rising to Data Valid

NOTES

[1]Timing specifications in bold print are 100% production tested. All other times are sample tested at +5°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]t_6 is measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[3]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 100 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (% FSR)	SNR (dB)	Package Option*
AD7884AN	−40°C to +85°C		88	N-40
AD7884BN	−40°C to +85°C	±0.003	88	N-40
AD7884AP	−40°C to +85°C		88	P-44
AD7884BP	−40°C to +85°C	±0.003	88	P-44
AD7884TQ	−55°C to +125°C	±0.003	88	Q-40
AD7885AN	−40°C to +85°C		88	N-28
AD7885BN	−40°C to +85°C	±0.003	88	N-28
AD7885AP	−40°C to +85°C		88	P-28
AD7885BP	−40°C to +85°C	±0.003	88	P-28
AD7885TQ	−55°C to +125°C	±0.003	88	Q-28

*N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.

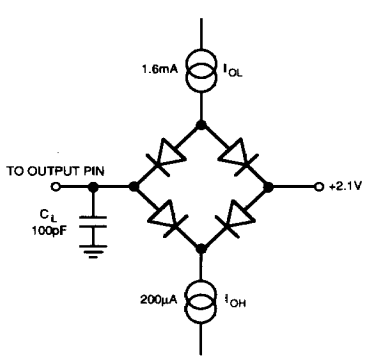


Figure 1. Load Circuit for Access Time and Bus Relinquish Time

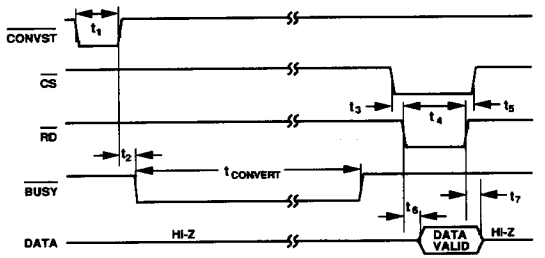


Figure 2. AD7884 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

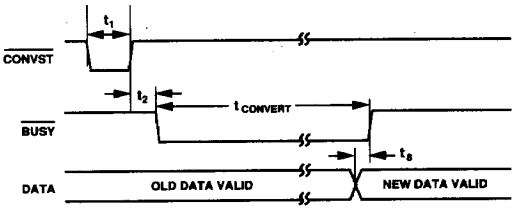


Figure 3. AD7884 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

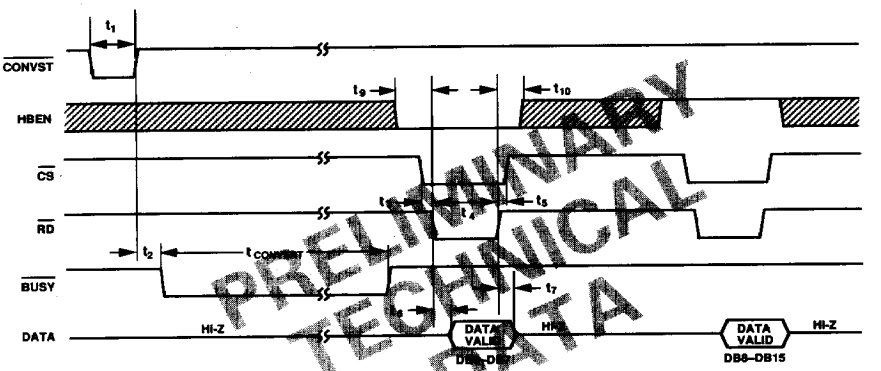


Figure 4. AD7885 Timing Diagram, Using $\overline{CS}$ and $\overline{RD}$

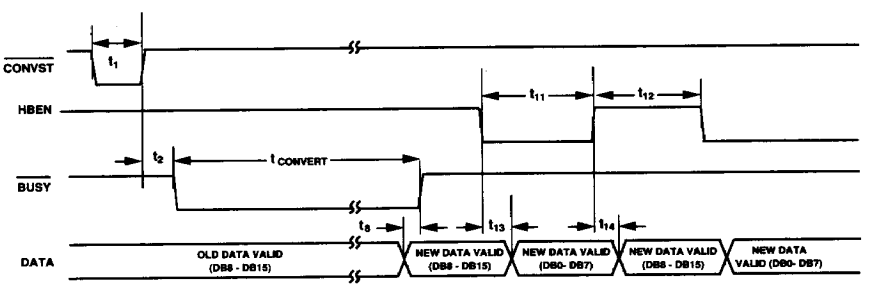


Figure 5. AD7885 Timing Diagram, with $\overline{CS}$ and $\overline{RD}$ Permanently Low

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND Pins to DGND	−0.3 V to V_{DD} +0.3 V
GND to DGND	−0.3 V to V_{DD} +0.3 V
$V_{IN}S$, $V_{IN}F$ to AGND	V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF+} to AGND	V_{SS} −0.3 V to V_{DD} +0.3 V
V_{REF-} to AGND	V_{SS} −0.3 V to V_{DD} +0.3 V
V_{INV} to AGND	V_{SS} −0.3 V to V_{DD} +0.3 V
Digital Inputs to DGND	−0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD} +0.3 V
Operating Temperature Range	
Commercial Plastic (A, B Versions)	−40°C to +85°C
Industrial Cerdip (A, B Versions)	−40°C to +85°C
Extended Cerdip (T Versions)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C
Power Dissipation (Any Package) to +75°C	1000 mW
Derates above +75°C by	10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

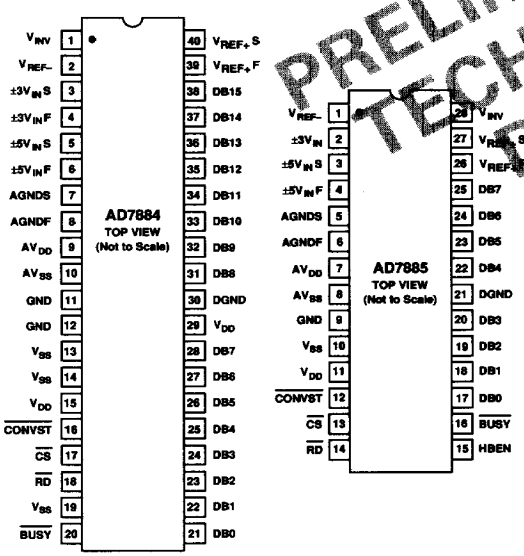
2

CAUTION

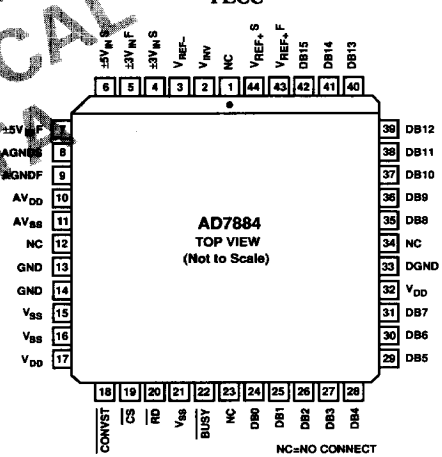
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

DIP



PLCC



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN FUNCTION DESCRIPTION

AD7884 Pin	AD7885 Pin	Description
V_{INV}	V_{INV}	This pin is connected to the inverting terminal of an op amp, as in Figure 6 and allows the inversion of the supplied +3 V reference.
V_{REF-}	V_{REF-}	This is the negative reference input and it can be obtained by using an external amplifier to invert the positive reference input. In this case, the amplifier output is connected to V_{REF-}. See Figure 6.
$\pm 3V_{IN}S$	—	This is the analog input sense pin for the ±3 volt analog input range on the AD7884.
$\pm 3V_{IN}F$	—	This is the analog input force pin for the ±3 volt analog input range on the AD7884. When using this input range, the ± 5 $V_{IN}F$ and ± 5 $V_{IN}S$ pins should be tied to AGND.
—	$\pm 3V_{IN}$	This is the analog input pin for the ±3 volt analog input range on the AD7885. When using this input range, the ± 5 $V_{IN}F$ and ± 5 $V_{IN}S$ pins should be tied to AGND.
$\pm 5V_{IN}S$	$\pm 5V_{IN}S$	This is the analog input sense pin for the ±5 volt analog input range on both the AD7884 and the AD7885.
$\pm 5V_{IN}F$	$\pm 5V_{IN}F$	This is the analog input force pin for the ±5 volt analog input range on both the AD7884 and AD7885. When using this input range, the ± 3 $V_{IN}F$ and ± 3 $V_{IN}S$ pins should be tied to AGND.
AGNDS	AGNDS	This is the ground return sense pin for the 9-bit ADC and the on-chip residue amplifier.
AGNDF	AGNDF	This is the ground return force pin for the 9-bit ADC and the on-chip residue amplifier.
AV_{DD}	AV_{DD}	Positive analog power rail for the sample-and-hold amplifier and the residue amplifier.
AV_{SS}	AV_{SS}	Negative analog power rail for the sample-and-hold amplifier and the residue amplifier.
GND	GND	This is the ground return for sample-and-hold section.
V_{SS}	V_{SS}	Negative supply for the 9-bit ADC.
V_{DD}	V_{DD}	Positive supply for the 9-bit ADC and all device logic.
$\overline{CONVST}$	$\overline{CONVST}$	This asynchronous control input starts conversion.
$\overline{CS}$	$\overline{CS}$	Chip Select control input.
$\overline{RD}$	$\overline{RD}$	Read control input. This is used in conjunction with $\overline{CS}$ to read the conversion result from the device output latch.
—	HBEN	High Byte Enable. Active high control input for the AD7885. It selects either the high or the low byte of the conversion for reading.
$\overline{BUSY}$	$\overline{BUSY}$	Busy output. The Busy output goes low when conversion begins and stays low until it is completed, at which time it goes high.
DB0–DB15	—	16-bit parallel data word output on the AD7884.
—	DB0–DB7	8-bit parallel data byte output on the AD7885.
DGND	DGND	Ground return for all device logic.
$V_{REF+}F$	$V_{REF+}F$	Reference force input.
$V_{REF+}S$	$V_{REF+}S$	Reference sense input. The device operates from a +3 V reference.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Error
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal (AGND).

Positive Gain Error
This is the deviation of the last code transition (01 . . . 110 to 01 . . . 111) from the ideal ($+V_{REF+}$ S − 1 LSB).

Negative Gain Error
This is the deviation of the first code transition (10 . . . 000 to 10 . . . 001) from the ideal ($-V_{REF+}$S + 1 LSB)

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\ to\ (Noise + Distortion) = (6.02N + 1.76)\ dB$$

Thus for a 16-bit converter, this is 98 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7884/AD7885, it is defined as:

$$THD\ (dB) = 20\ log\ \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

The AD7884/AD7885 is tested using the CCIFF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Power Supply Rejection Ratio
This is the ratio, in dBs, of the change in positive gain error to the change in V_{DD} or V_{SS}. It is a dc measurement.

OPERATIONAL DIAGRAM

An operational diagram for the AD7884/AD7885 is shown in Figure 6. It is set up for an analog input range of ±5 V. If a ±3 V input range is required, A1 should drive ±3 V_{IN}S and ±3 V_{IN}F with ±5 V_{IN}S, ±5 V_{IN}F being tied to system AGND.

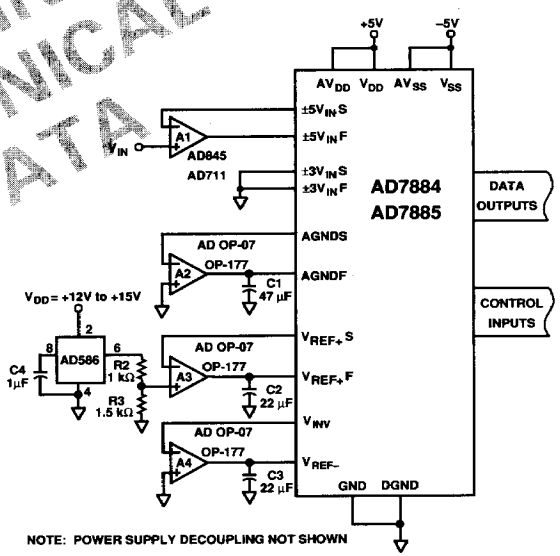


Figure 6. AD7884/AD7885 Operational Diagram

The chosen input buffer amplifier (A1) should have low noise and distortion and fast settling time for high bandwidth applications. Both the AD711 and the AD845 are suitable amplifiers.

A2 is the force, sense amplifier for AGND. The AGNDS pin should be at zero potential. Therefore, the amplifier must have a very low input offset voltage and good noise performance. For these reasons, either the AD OP-07 or OP-177 is recommended. The output of A2 is decoupled with a 47 µF solid tantalum capacitor to AGND to deal with the fast current transients on the

AGNDS pin. The stability of this arrangement is marginal and if the user wishes to improve the phase margin, the circuit given in Figure 7 may be used. A feedback capacitor (R_F) of 47 μF should be used. This circuit compensates for the load capacitor by adding a low frequency zero and ensures an adequate phase margin.

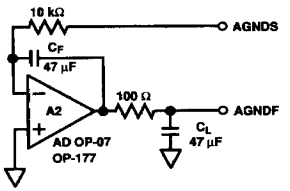


Figure 7. Compensation Circuit for A2

The required +3 V reference is derived from the AD586. The +5 V output is divided down to +3 V by R2 and R3 before being buffered by A3. A4 is a unity gain inverter which provides the −3 V negative reference. The gain setting resistors are on-chip and are factory trimmed to ensure precise tracking of V_{REF+}. Figure 6 shows A3 and A4 as either AD OP-07s or OP-177s. If these amplifiers are used, then the outputs should be decoupled to AGND with 22 μF solid tantalum capacitors as shown. This is to deal with the rapidly changing reference input impedance of the AD7884/AD7885. These can also be compensated with the circuit of Figure 7 to give improved phase margin. A feedback capacitor (C_F) of 22 μF should be used. An alternative to this arrangement which yields the same noise performance is to use very wideband amplifiers (AD845 for example) for A3 and A4. These have the ability to respond to the rapidly changing reference input impedance without any decoupling to AGND. Thus, there is a saving in decoupling capacitors and compensation circuitry. The disadvantage is that these high speed amplifiers do not have as good dc offset performance as the AD OP-07 or the OP-177. This will result in increased system gain error.

CIRCUIT DESCRIPTION

Analog Input Section

The analog input section of the AD7884/AD7885 is shown in Figure 8. It contains both the input signal conditioning and sample-and-hold amplifier. When the ±3 V_{IN}S and ±3 V_{IN}F inputs are tied to 0 V, the input section has a gain of −0.6 and transforms an input signal of ±5 volts to the required ±3 volts. When the ±5 V_{IN}S and ±5 V_{IN}F inputs are grounded, the input section has a gain of −1 and so the analog input range is now ±3 volts. Resistors R4 and R5, at the amplifier output, further condition the ±3 volts signal to be 0 to −3 volts. This is the required input for the 9-bit A/D converter section.

With SW1 closed, the output of A1 follows the input (the sample-and-hold is in the track mode). On the rising edge of the $\overline{\text{CONVST}}$ pulse, SW1 goes open circuit, and capacitor C1 holds the voltage on the output of A1. The sample-and-hold is now in the hold mode. The aperture delay time for the sample-and-hold is nominally 50 ns.

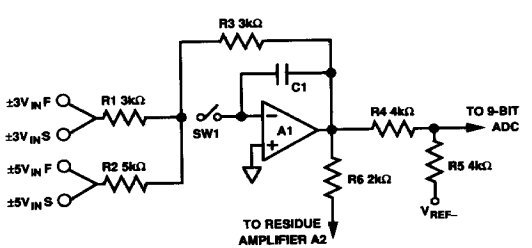


Figure 8. AD7884/AD7885 Analog Input Section

A/D Converter Section

The AD7884/AD7885 uses a two-pass flash technique in order to achieve the required speed and resolution. When the $\overline{\text{CONVST}}$ control input goes from low to high, the sample-and-hold amplifier goes into the hold mode and a 0 V to −3 V signal is presented to the input of the 9-bit ADC. The first phase of conversion generates the 9 MSBs of the 16-bit result and transfers these to the latch and ALU combination. They are also fed back to the 9 MSBs of the 16-bit DAC. The 7 LSBs of the DAC are permanently loaded with 0s. The DAC output is subtracted from the analog input with the result being amplified and offset in the Residue Amplifier Section. The signal at the output of A2 is proportional to the error between the first phase result and the actual analog input signal and is digitized in the second conversion phase. This second phase begins when the 16-bit DAC and the Residue Error Amplifier have both settled. First, SW2 is turned off and SW3 is turned on. The 9-bit result is transferred to the output latch and ALU. An error correction algorithm now compensates for the offset inserted in the Residue Amplifier Section and errors introduced in the first pass conversion and combines both results to give the 16-bit answer.

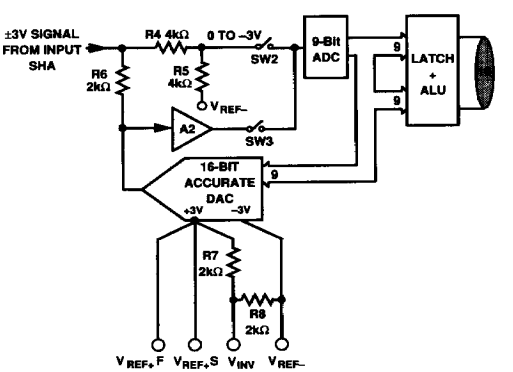


Figure 9. A/D Converter Section

Timing and Control Section

Figure 10 shows the timing and control sequence for the AD7884/AD7885. When the part receives a $\overline{\text{CONVST}}$ pulse, the conversion begins. The input sample-and-hold goes into the hold mode 50 ns after the rising edge of $\overline{\text{CONVST}}$ and $\overline{\text{BUSY}}$ goes low. This is the first phase of conversion and takes 3.35 μs to complete. The second phase of conversion begins when SW2 is turned off and SW3 turned on. The Residue Amplifier and SHA section (A2 in Figure 9) goes into hold mode at this point and allows the input sample-and-hold to go back into sample mode. Thus, while the second phase of conversion is ongoing, the input sample-and-hold is also acquiring the input signal for the next conversion. This overlap between conversion and acquisition allows throughput rates of 166 kSPS to be achieved.

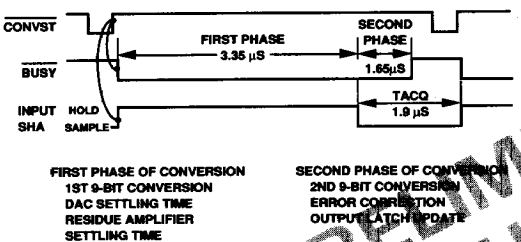


Figure 10. Timing and Control Sequence

USING THE AD7884/AD7885

Analog Input Ranges

The AD7884/AD7885 can be set up to have either a ±3 volts analog input range or a ±5 volts analog input range. Figures 11 and 12 show the necessary corrections for each of these. The output code is 2s complement and the ideal code table for both input ranges is shown in Table I.

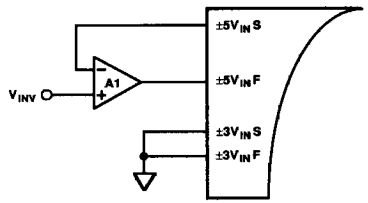


Figure 11. ±5 V Input Range Connections

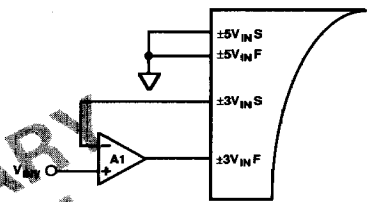


Figure 12. ±3 V Input Range Connections

Reference Considerations

The AD7884/AD7885 operates from a ±3 volt reference. This can be derived simply from any single +5 volt reference as shown in Figure 6.

The critical performance specification for a reference in a 16-bit application is noise. The reference pk-pk noise should be insignificant in comparison to the ADC noise. The AD7884/AD7885 has a typical rms noise of 120 μV. For example a reasonable target would be to keep the total rms noise less than 125 μV. To do this the reference noise needs to be less than 35 μV rms. Using a crest factor of 3.3 this corresponds to a pk-pk noise of 230 μV. Both the AD586 and the AD REF-02 noise is lower than this, making both suitable.

Table I. Ideal Output Code Table for the AD7884/AD7885

Analog Input			Digital Output
In Terms of FSR[2]	±3 V Range[3]	±5 V Range[4]	Code Transition[1]
+FSR/2 − 1 LSB	2.999908	4.999847	011 . . . 111 to 011 . . . 110
+FSR/2 − 2 LSBs	2.999817	4.999695	011 . . . 110 to 011 . . . 101
+FSR/2 − 3 LSBs	2.999726	4.999543	011 . . . 101 to 011 . . . 100
AGND + 1 LSB	0.000092	0.000153	000 . . . 001 to 000 . . . 000
AGND	0.000000	0.000000	000 . . . 000 to 111 . . . 111
AGND − 1 LSB	−0.000092	−0.000153	111 . . . 111 to 111 . . . 110
−(FSR/2 − 3 LSBs)	−2.999726	−4.999543	100 . . . 011 to 100 . . . 010
−(FSR/2 − 2 LSBs)	−2.999817	−4.999695	100 . . . 010 to 100 . . . 001
−(FSR/2 − 1 LSB)	−2.999908	−4.999847	100 . . . 001 to 100 . . . 000

NOTES

[1]This table applies for $V_{REF+}S$ = +3 V.

[2]FSR (Full-Scale Range) is 6 volts for the ±3 V input range and 10 volts for the ±5 V input range.

[3]1 LSB on the ±3 V range is FSR/2^{16} and is equal to 91.5 μV.

[4]1 LSB on the ±5 V range is FSR/2^{16} and is equal to 152.6 μV.

The buffer amplifier used to drive the device V_{REF+} should have low enough noise performance so as not to affect the overall system noise requirement. The ADOP-07, AD845 and OP-177 are all suitable.

Decoupling and Grounding

The AD7884 has one AV_{DD} pin and two V_{DD} pins. It also has one AV_{SS} pin and three V_{SS} pins. The AD7885 has one AV_{DD} pin, one V_{DD} pin, one AV_{SS} pin and one V_{SS} pin. Figure 6 shows how a common +5 V supply should be used for the positive supply pins and a common −5 V supply for the negative supply pins.

For decoupling purposes, the critical pins on both devices are the AV_{DD} and AV_{SS} pins. Each of these should be decoupled to system AGND with 10 μF tantalum and 0.1 μF ceramic capacitors right at the pins. With the V_{DD} and V_{SS} pins, it is sufficient to decouple each of these with ceramic 1 μF capacitors.

AGNDS, AGNDF are the ground return points for the on-chip 9-bit ADC. They should be driven by a buffer amplifier as shown in Figure 6.

The GND pin is the analog ground return for the on-chip linear circuitry. It should be connected to system analog ground.

The DGND pin is the ground return for the on-chip digital circuitry. It should be connected to the ground terminal of the V_{DD} and V_{SS} supplies. If a common analog supply is used for AV_{DD} and V_{DD} then DGND should be connected to the common ground point.

Power Supply Sequencing

If the AD7884/AD7885 is being powered from separate analog and digital supplies, then care should be taken with power supply sequencing. AV_{DD} should always come up before V_{DD} and AV_{SS} should always come up before V_{SS}. If this cannot be guaranteed, Schottky diodes (HP5082-2810 or equivalent) should be used to ensure that V_{DD} never exceeds AV_{DD} by more than 0.3 V and that V_{SS} never goes below AV_{SS} by more than 0.3 V.

AD7884/AD7885 PERFORMANCE

Linearity

The linearity of the AD7884/AD7885 is determined by the on-chip 16-bit D/A converter. This is a segmented DAC which is laser trimmed for 16-bit DNL performance to ensure that there are no missing codes in the ADC transfer function. Figure 13 shows a typical INL plot for the AD7884/AD7885.

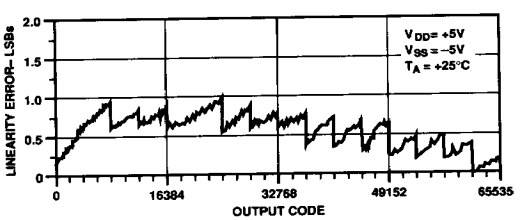


Figure 13. AD7884/AD7885 Typical Linearity Performance

Noise

In an A/D converter, noise exhibits itself as code uncertainty in dc applications and as the noise floor (in an FFT, for example) in ac applications.

In a sampling A/D converter like the AD7884/AD7885, all information about the analog input appears in the baseband from dc to 1/2 the sampling frequency. An antialiasing filter will remove unwanted signals above fs/2 in the input signal but the converter wideband noise will alias into the baseband. In the AD7884/AD7885, this noise is made up of sample-and-hold noise and a/d converter noise. The sample-and-hold section contributes 51 μV rms and the ADC section contributes 59 μV rms. These add up to a total rms noise of 78 μV. This is the input referred noise in the ±3 V analog input range. When operating in the ±5 V input range, the input gain is reduced to −0.6. This means that the input referred noise is now increased by a factor of 1.66 to 120 μV rms.

Figure 14 shows a histogram plot for 5000 conversions of a dc input using the AD7884/AD7885 in the ±5 V input range. The analog input was set at the center of a code transition. All codes other than the center code are due to the ADC noise. In this case, the spread is five codes.

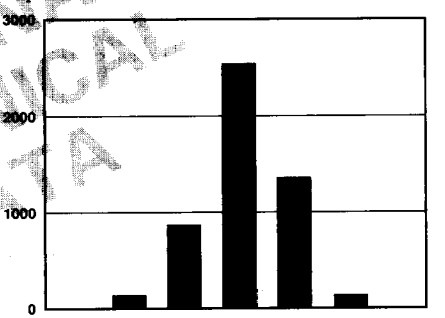


Figure 14. Histogram of 5000 Conversions of a DC Input

If the noise in the converter is too high for an application, it can be reduced by oversampling and digital filtering. This involves sampling the input at higher than the required word rate and then averaging to arrive at the final result. The very fast conversion time of the AD7884/AD7885 makes it very suitable for oversampling. For example, if the required input bandwidth is 50 kHz, the AD7884/AD7885 could be oversampled by a factor of 2. This yields a 3 dB improvement in the effective SNR performance. The noise performance in the ±5 volt input range is now effectively 85 μV rms and the resultant spread of codes for 2500 conversions will be four. This is shown in Figure 15.

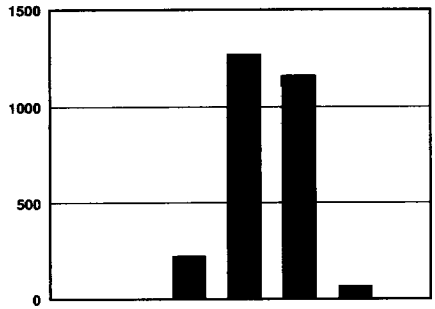


Figure 15. Histogram of 2500 Conversions of a DC Input Using a ×2 Oversampling Ratio

Dynamic Performance

With a combined conversion and acquisition time of 6 μs, the AD7884/AD7885 is ideal for wide bandwidth signal processing applications. Signal to (Noise + Distortion), Total Harmonic Distortion, Peak Harmonic or Spurious Noise and Intermodulation Distortion are all specified. Figure 16 shows a typical FFT plot of a 1.8 kHz, ±5 V input after being digitized by the AD7884/AD7885.

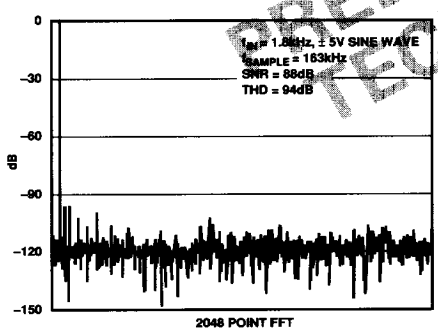


Figure 16. AD7884/AD7885 FFT Plot

MICROPROCESSOR INTERFACING

The AD7884/AD7885 is designed on a high speed process which results in very fast interfacing timing. The AD7884 has a full 16-bit parallel bus and the AD7885 has an 8-bit wide bus.

AD7884–MC68000 Interface

Figure 17 shows a general interface diagram for the MC68000, 16-bit microprocessor to the AD7884. In Figure 17, conversion is initiated by bringing $\overline{CSA}$ low (i.e., writing to the appropriate address). This allows the processor to maintain control over the complete conversion process. In some cases it may be more desirable to control conversion independent from the processor. This can be done by using an external sampling timer.

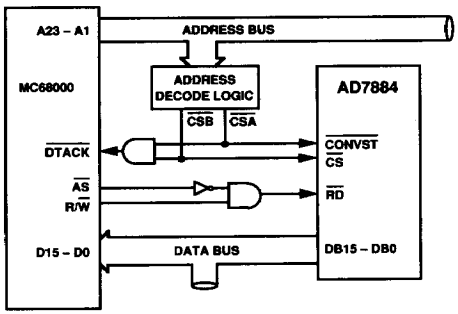


Figure 17. AD7884 to MC68000 Interface

Once conversion has been started, the processor must wait until it is completed before reading the result. There are two ways of ensuring this. The first way is to simply use a software delay to wait for 6.5 μs before bringing $\overline{CS}$ and $\overline{RD}$ low to read the data. The second way is to use the $\overline{BUSY}$ output of the AD7884 to generate an interrupt in the MC68000. Because of the nature of its interrupts, the MC68000 requires additional logic (not shown in Figure 17) to allow it to be interrupted correctly. For full information on this, consult the MC68000 User's Manual.

AD7885 to 8088 Interface

The AD7885, with its byte (8 + 8) data format, is ideal for use with the 8088 microprocessor. Figure 18 is the interface diagram. Conversion is started by enabling $\overline{CSA}$. At the end of conversion, data is read into the processor. The read instructions are:

```
MOV AX, C001    Read 8 MSBs of data
MOV AX, C000    Read 8 LSBs of data
```

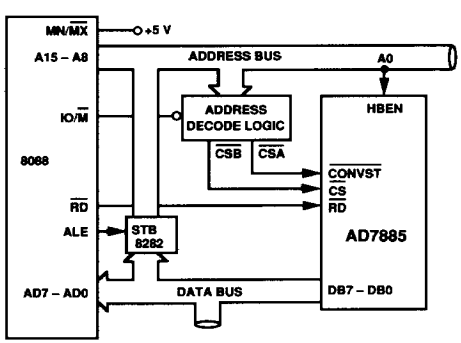


Figure 18. AD7885 to 8088 Interface

AD7884 to ADSP-2101 Interface

Figure 19 shows an interface between the AD7884 and the ADSP-2101. Conversion is initiated using a timer which allows very accurate control of the sampling instant. The AD7884 $\overline{BUSY}$ line provides an interrupt to the ADSP-2101 when conversion is completed. The $\overline{RD}$ pulse width of the processor can be programmed using the Data Memory Wait State Control Register. The result can then be read from the ADC using the following instruction:

MR0 = DM (ADC)

where MR0 is the ADSP-2101 MR0 register, and
ADC is the AD7884 address.

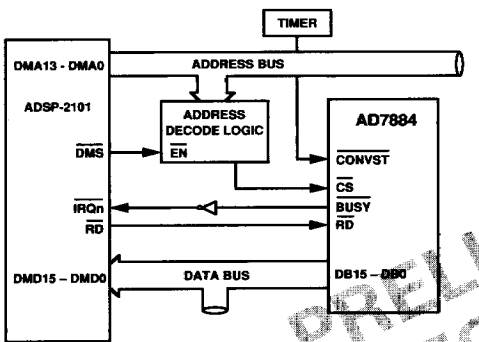


Figure 19. AD7884 to ADSP-2101 Interface

Stand-Alone Operation

If $\overline{CS}$ and $\overline{RD}$ are tied permanently low on the AD7884, then, when a conversion is completed, output data will be valid on the rising edge of $\overline{BUSY}$. This makes the device very suitable for stand-alone operation. All that is required to run the device is an external $\overline{CONVST}$ pulse which can be supplied by a sample timer. Figure 20 shows the AD7884 set up in this mode with the $\overline{BUSY}$ signal providing the clock for the 74HC574 3-state latches.

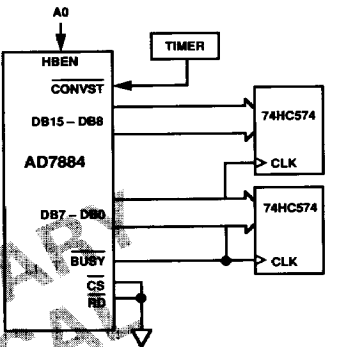


Figure 20. Stand-Alone Operation