High Speed 8-Bit A/D Converters

AD9028/AD9038

FEATURES
300 MSPS Encode Rate
250 MHz Large Signal Input Bandwidth
Low Input Capacitance: 17 pF
Excellent SNR
Single −5.2 V Power Supply
Overflow Bit & Bit Invert Functions
1:2 Demultiplexed Outputs (AD9038)
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Digital Oscilloscopes
Waveform Digitizers
Radar Receivers
Electronic Countermeasures

GENERAL DESCRIPTION

The AD9028 and AD9038 are ECL-compatible 8-bit, high speed flash analog-to-digital converters. Both are fabricated in an advanced bipolar VLSI process which ensures exceptionally wide analog input bandwidth (250 MHz) and encode rates up to 300 MSPS.

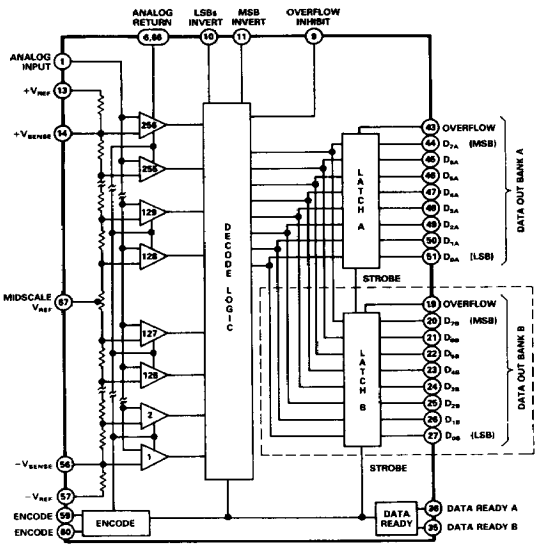
Output data for the AD9028 include Overflow and Data Ready signals; control pins allow the user to invert the MSB and/or LSBs. The AD9038 combines the features of the AD9028 with on-board demultiplexing circuits to provide two sets of output data. These ease the task of interfacing the converter by reducing the data rate to half the encode rate.

The analog input is designed for 0 to −2.0 volt operation. Sense pins for the $+V_{REF}$ and $-V_{REF}$ inputs allow full-scale calibration of the input range; a tap at the midpoint of the reference ladder is available to minimize integral nonlinearity. Dynamic performance is enhanced by driving the ANALOG RETURN pins with a buffered analog input; see the Applications section.

There are two linearity grades of each device. Commercial temperature ranges of 0 to +70°C and military temperature ranges of −55°C to +125°C are available. Both components are offered in a ceramic 68-pin LCC, and a ceramic 68-pin leaded package. These packages are specially designed for low thermal impedance.

The AD9028/AD9038 A/D Converter is available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9028/AD9038/883B data sheet for detailed specifications.

FUNCTIONAL BLOCK DIAGRAM



AD9028/AD9038—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

ANALOG INPUT . . . . . $-V_S$ to +0.5 V
ANALOG RETURN . . . . . 0 V to +2.0 V
$-V_S$ to GROUND . . . . . +0.5 V dc to −6.0 V dc
$+V_{REF}$, $-V_{REF}$, MIDSCALE V_{REF} . . . . . −2.1 V to +0.1 V
$+V_{REF}$ to $-V_{REF}$ . . . . . 2.1 V
MIDSCALE V_{REF}, $+V_{SENSE}$, $-V_{SENSE}$ Current . . . . ±4 mA
MSB INVERT, LSBs INVERT, OVERFLOW INHIBIT, ENCODE, $\overline{\text{ENCODE}}$, HYSTERESIS . . . . . $-V_S$ to 0 V
ENCODE to $\overline{\text{ENCODE}}$ . . . . . 4 V
Digital Output Current . . . . . 20 mA
ANALOG $-V_S$ to DIGITAL $-V_S$ . . . . . ±0.5 V
Operating Temperature Range
AD9028/AD9038KE/KZ/JE/JZ . . . . . 0 to +70°C
AD9028/AD9038TE/TZ/SE/SZ/883 . . . . . −55°C to +125°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Temperature (Soldering, 10sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS ($-V_S = -5.2$ V; $+V_{REF} = 0$ V; $-V_{REF} = -2$ V; ANALOG RETURN = 0 V, unless otherwise noted)

Parameter (Conditions)	Temp	Level	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ/883 Min	Typ	Max	Units
RESOLUTION			8			8			8			8			Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
Integral NonLinearity	+25°C	I		0.8	1.0		0.6	0.75		0.8	1.0		0.6	0.75	LSB
	Full	VI		1.0	1.2		0.8	1.0		1.0	1.2		0.8	1.0	LSB
No Missing Codes	Full	VI	GUARANTEED			GUARANTEED									
ANALOG INPUT															
Input Bias Current[3]	+25°C	I		125	250		125	250		125	250		125	250	μA
	Full	VI			400			400			400			400	μA
Input Resistance	+25°C	I	50	75		50	75		50	75		50	75		kΩ
Input Capacitance[3]	+25°C	III		17	21		17	21		17	21		17	21	pF
Analog Bandwidth[4]	+25°C	V		250			250			250			250		MHz
REFERENCE INPUT															
Reference Ladder Resistance	+25°C	I	24	40	60	24	40	60	24	40	60	24	40	60	Ω
	Full	VI	20		75	20		75	20		75	20		75	Ω
Ladder Tempco	Full	V		0.13			0.13			0.13			0.13		Ω/°C
Ref. Input Bandwidth	Full	V		30			30			30			30		MHz
Reference Ladder Offset[4]	+25°C	I		32	45		32	45		32	45		32	45	mV
(Top)	Full	VI			47			47			47			47	mV
Reference Ladder Offset[4]	+25°C	I		26	37		26	37		26	37		26	37	mV
(Bottom)	Full	VI			39			39			39			39	mV
Offset Drift Coefficient	Full	V		20			20			20			20		μV/°C
SWITCHING PERFORMANCE[4, 5]															
Maximum Conversion Rate	+25°C	I	300	325		300	325		300	325		300	325		MSPS
Aperture Delay (t_A)	+25°C	V		1.4			1.4			1.4			1.4		ns
Aperture Uncertainty (Jitter)	+25°C	V		3			3			3			3		ps, rms
Output Delay (t_{OD})	+25°C	I	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	4.7	6	7.3	ns
Output Rise Time	+25°C	I		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Fall Time	+25°C	I		1.0	1.6		1.0	1.6		1.0	1.6		1.0	1.6	ns
Output Time Skew	+25°C	I		0.25	0.7		0.25	0.7		0.25	0.7		0.25	0.7	ns
Data Ready															
Output Delay (t_{DR})	+25°C	I	4.1	5.4	6.7	4.1	5.4	6.7	4.8	6.1	7.4	4.8	6.1	7.4	ns
ENCODE INPUT															
Logic "1" Voltage	Full	IV	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI		125	285		125	285		125	285		125	285	μA
Logic "0" Current	Full	VI		100	285		100	285		100	285		100	285	μA
Input Capacitance	+25°C	V		3.6			3.6			3.6			3.6		pF
Pulse Width (High)[6]	+25°C	I	1			1			1			1			ns
Pulse Width (Low)[6]	+25°C	I	2			2			2			2			ns

Parameter (Conditions)	Temp	Level	AD9028JE/JZ SE/SZ/883 Min	Typ	Max	AD9028KE/KZ TE/TZ/883 Min	Typ	Max	AD9038JE/JZ SE/SZ/883 Min	Typ	Max	AD9038KE/KZ TE/TZ/883 Min	Typ	Max	Units
DYNAMIC PERFORMANCE[7]															
Transient Response	+25°C	V		3			3			3			3		ns
Overvoltage Recovery Time	+25°C	V		3			3			3			3		ns
Effective Number of Bits (ENOB)															
Analog Input @ 9.3 MHz	+25°C	I	7.0	7.1		7.2	7.5		7.0	7.2		7.2	7.5		Bits
@ 49 MHz	+25°C	I	6.5	7.0		6.5	7.0		6.5	7.0		6.5	7.0		Bits
@ 92 MHz	+25°C	I	5.4	5.8		5.4	5.8		5.4	5.8		5.4	5.8		Bits
In-Band Harmonics															
Analog Input @ 9.3 MHz	+25°C	I	48	53		54	56		48	53		54	56		dBc
@ 49 MHz	+25°C	I	41	48		41	48		41	48		41	48		dBc
@ 92 MHz	+25°C	I	36	40		36	40		36	40		36	40		dBc
Signal-to-Noise Ratio[8]															
Analog Input @ 9.3 MHz	+25°C	I	44	45		45.5	47		44	45		45.5	47		dB
@ 49 MHz	+25°C	I	40	43		40	43		40	43		40	43		dB
@ 92 MHz	+25°C	I	33	36		33	36		33	36		33	36		dB
Signal-to-Noise Ratio[8] (without harmonics)															
Analog Input @ 9.3 MHz	+25°C	I	45.5	48		45.5	48		45.5	48		45.5	48		dB
@ 49 MHz	+25°C	I	43	46		43	46		43	46		43	46		dB
@ 92 MHz	+25°C	I	38	43		38	43		38	43		38	43		dB
Two-Tone Intermodulation Distortion Rejection[9]	+25°C	I	42	49		42	49		42	49		42	49		dB
DIGITAL OUTPUTS[5]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			1.5			−1.5			1.5	V
POWER SUPPLY															
Analog Return	+25°C	V		14.4			14.4			14.4			14.4		mA
Negative Supply Current	+25°C	I		390	475		390	475		430	495		430	495	mA
($-V_S$ = −5.2 V)	Full	VI			515			515			550			550	mA
Power Dissipation	+25°C	V		2.0			2.0			2.2			2.2		W
Ref. Ladder Dissipation	+25°C	V		100			100			100			100		mW
Power Supply															
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V
Rejection Ratio (PSRR)	+25°C	I		1.2	3		1.2	3		1.2	3		1.2	3	mV/V

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:68-pin leaded ceramic chip carrier θ_{JA}=31°C/W, θ_{JC}=1.1°C/W; 68-pin ceramic LCC θ_{JA}=36°C/W, θ_{JC}=2.6°C/W.

[3]Measured with analog input = 0 V.

[4]See definitions of specifications.

[5]Outputs terminated through 100 Ω to −2.0 V; C_L<4 pF

[6]ENCODE command rise/fall times should be less than 2.5 ns for normal operation.

[7]Measured at 250 MSPS encode rate; analog return is tied to +1 V dc. (See text and diagrams.)

[8]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[9]Intermodulation measured with analog input frequencies of 60 MHz and 70 MHz at 7 dB below full scale.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

- I – 100% production tested.
- II – 100% production tested at +25°C, and sample tested at specified temperatures.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

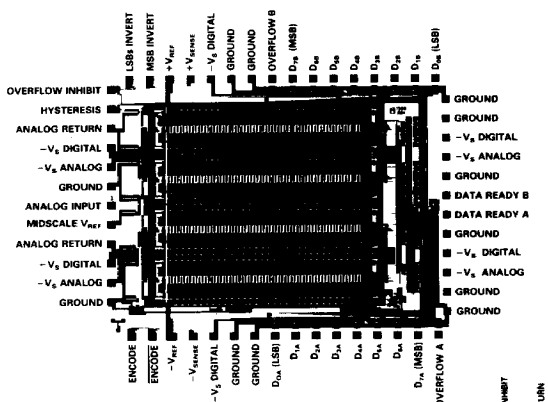
RECOMMENDED OPERATING CONDITIONS

Parameter	Input Voltage Min	Nominal	Max
$-V_S$	−5.46	−5.2	−4.94
$+V_{REF}$	$-V_{REF}$	0	+0.1
$-V_{REF}$	−2.1	−2.0	$+V_{REF}$
ANALOG INPUT	$-V_{REF}$		$+V_{REF}$
ANALOG RETURN	Analog In		Analog In +2.0 V

ORDERING GUIDE

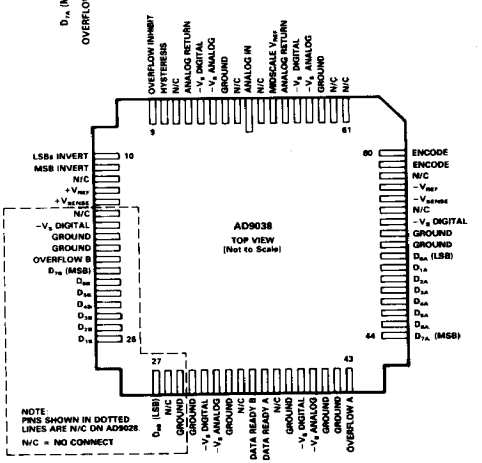
Model	Temperature	Description	Package Option[1]
AD9028JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9028JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9028SE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028TE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9028SZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9028TZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038JE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038KE	0 to +70°C	68-Pin Ceramic LCC	E-68A
AD9038JZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038KZ	0 to +70°C	68-Pin Leaded Ceramic	Z-68
AD9038SE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038TE/883[2]	−55°C to +125°C	68-Pin Ceramic LCC	E-68A
AD9038SZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68
AD9038TZ/883[2]	−55°C to +125°C	68-Pin Leaded Ceramic	Z-68

NOTES
[1]E = Ceramic Leadless Chip Carrier; Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.
[2]For specifications, refer to Analog Devices *Military Products Databook*.



MECHANICAL INFORMATION

Die Dimensions	.178 × 148 × 15 (±2) mils
Pad Dimensions	.4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	.Nitride
Die Attach	.Gold Eutectic
Bond Wire	1.3 mil, Gold; Gold Ball Bonding



AD9028/AD9038 Pin Designations
(Note: Chip Cavity Opening Is On Bottom of Package.)

AD9028/AD9038 PIN DESCRIPTIONS

Pin No.	Name	Function
1	ANALOG INPUT	Analog input is nominally between 0 and −2 Volts.
6, 66	ANALOG RETURN	Normally grounded; supplies current to input comparator circuits. Pins can be tied to postive potential (+2.0 V max), or buffered version of analog input to reduce capacitance and enhance dynamic performance. (See Applications.)
36	DATA READY A	Rising edge of signal can be used to externally latch D_{0A}–D_{7A}.
35	DATA READY B	Rising edge of signal can be used to externally latch D_{0B}–D_{7B}.
44–51	D_{7A}–D_{0A}	ECL digital data from Data Bank A.
20–27	D_{7B}–D_{0B}	ECL digital data from Data Bank B.
59, 60	ENCODE, ENCODE	Differential ECL convert signals.
3, 17, 18, 29, 30, 33, 38, 41, 42, 52, 53, 63	GROUND	All ground pins should be connected together.
8	HYSTERESIS	Normally grounded; hysteresis control pin.
10	LSBs INVERT	Normally connected to $-V_S$. When grounded, lower order bits are inverted.
67	MIDSCALE V_{REF}	Normally floating; midpoint of reference resistor ladder. Can be adjusted to minimize integral nonlinearity.
11	MSB INVERT	Normally connected to $-V_S$. When grounded, MSB is inverted.
43	OVERFLOW A	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
19	OVERFLOW B	ECL-compatible output indicating ANALOG IN > $+V_{SENSE}$.
9	OVERFLOW INHIBIT	Normally floating or tied to $-V_S$. When grounded, OVERFLOW A and B are disabled; D0–D7 remain at ECL logic "1" when ANALOG IN > $+V_{SENSE}$.
13	$+V_{REF}$	Normally 0 V; sets voltage reference at top of ladder.
57	$-V_{REF}$	Normally −2 V; sets voltage reference at bottom of ladder.
4, 32, 40, 64	$-V_S$ ANALOG	−5.2 Volts; analog supply voltage.
5, 16, 31, 39, 54, 65	$-V_S$ DIGITAL	−5.2 Volts; digital supply voltage.
14	$+V_{SENSE}$	Voltage sense line to most positive comparator reference input.
56	$-V_{SENSE}$	Voltage sense line to most negative comparator reference input.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Output Delay
The delay between the 50% point of the falling edge of the ENCODE command and the 50% point of the rising edge of DATA READY A or DATA READY B.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Effective Number of Bits (ENOB)
ENOB is a measure of ac linearity and is calculated from a sine wave curve fit according to the following expression:

$$ENOB = N - LOG_2 [\text{ rms error (actual)/rms error (ideal) }]$$

N is the resolution (number of bits) of the converter. The actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

In-Band Harmonics
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Maximum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Output Delay
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of output data.

Output Time Skew
Bit-to-bit time variations among D0 to D7 outputs. In the AD9028 and AD9038 specifications, time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 8-bit accuracy after an analog input signal 150% of full scale is reduced to the full scale (0 to −2 V) range of the converter.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage. In the AD9028 and AD9038 units, $-V_S$ (−5.2 V) is within ±5% of its nominal value for this test.

DEFINITIONS OF SPECIFICATIONS (continued)

Reference Ladder Offset
The deviation between the top (or bottom) comparator transition voltage as measured at the analog input, and the voltage at the $+V_{REF}$ (or $-V_{REF}$) pin. This is valuable in determining the accuracy and adjustment range for $\pm V_{REF}$ sources.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 8-bit accuracy when a step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

THEORY OF OPERATION

Refer to the AD9038 Block Diagram. Both units use a "flash," or parallel, A/D architecture. The analog input voltage range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally 0 to -2 V. An internal resistor ladder divides this reference into 255 levels, each representing a single quantization level.

The A/D conversion, triggered by the ENCODE signal, is performed by 255 comparators. The output of the comparators indicates the appropriate quantization level of the analog input signal. The decoding logic processes the comparator outputs and provides an 8-bit code to the output stage.

Flash architecture has an advantage over other A/D architectures because the conversion occurs in one step, and the performance of the converter is limited primarily by the speed and matching of the individual comparators. A state-of-the-art bipolar process and careful comparator design give the AD9028/AD9038 excellent ac performance. A proprietary decoding scheme minimizes error codes, and control pins allow the user to select among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

APPLICATIONS

Voltage References
The AD9028/AD9038 requires that the user provide two voltage references: $+V_{REF}$ and $-V_{REF}$, as shown in Figure 1. These two voltages are applied across an internal resistor ladder (nominally 40 Ω) and set the analog input voltage range of the converter. Each voltage reference should be driven from a stable, low impedance source. The reference connections should be capacitively coupled to ground to bypass noise.

Applying a voltage greater than 2.1 V across the internal resistor ladder will cause current densities to exceed rated values, and may cause permanent damage to the AD9028/AD9038. The design of the reference circuit should limit the voltage available to the references.

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to 100 μA.

The voltage at the midpoint of the resistor ladder, MIDSCALE VREF, can be adjusted to improve the integral linearity of individual devices.

A suggested application in Figure 4 shows a reference circuit which nulls out the offset errors using two op amps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amp; resistors at the base and emitter stabilize their operation.

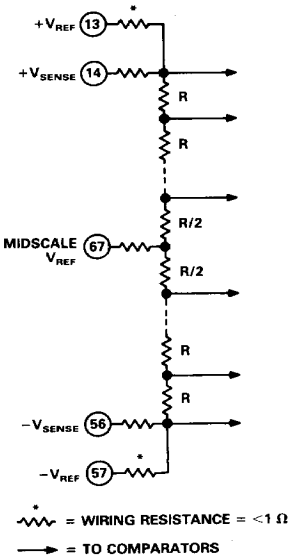


Figure 1. Reference Ladder

Analog Input Signal
The analog input circuit of the AD9028/AD9038 consists of 255 comparator inputs and can be represented by a single transistor as shown in Figure 2.

Typically, the ANALOG INPUT has an input resistance of 100 kΩ. Input capacitance is characterized in Figure 3.

With ANALOG RETURN (collector of the input transistor) connected to ground, collector base capacitance causes the analog input capacitance to be dependent on the analog input voltage. This varying capacitance is typical of flash converters, and requires that the ANALOG INPUT be driven from a low impedance source. This source must be capable of driving a capacitive load to avoid distorting the analog input signal at high

frequencies. In applications where the analog source cannot adequately drive the input capacitance, harmonic distortion will increase; the effect will be greatest on the second harmonic.

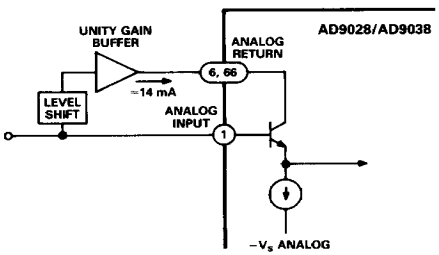


Figure 2. Preferred Analog Input Configuration

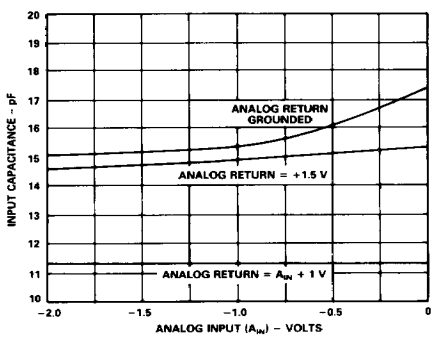


Figure 3. Input Capacitance vs. Input Voltage

AC performance of the AD9028/AD9038 can be improved by connecting the ANALOG RETURN to a dc voltage between ground and +1.5 V. This reduces the analog input capacitance and lessens its dependence on the analog input voltage (see Figure 3).

The circuits shown in Figure 2 and Figure 4 show the ANALOG RETURN driven by a buffered version of the signal presented to the ANALOG INPUT. The dc level of this signal is 1 V higher than the analog input, and thus reduces the analog input capacitance as described above. In addition, the signal cancels the ac voltage between the ANALOG RETURN and ANALOG INPUT connections, which minimizes the collector-base component of the analog input capacitance. The analog input capacitance characteristics under this condition are also shown in Figure 3.

In any of the configurations described above, the user should drive the analog signal from a low distortion, low noise amplifier. A good choice is the AD9611, a wide bandwidth operational amplifier with excellent ac performance.

Selection of the buffer is also important for applications in which the analog input signal is applied to the ANALOG RETURN. The gain of the buffer should be set as close to 1 as possible, and the buffer should have a low phase shift at the frequencies of interest. It must also be able to supply the current required, typically 14 mA.

Harmonic distortion at the ANALOG RETURN is not as critical as that at the ANALOG INPUT, but should remain less than 40 dB (out to 100 MHz) to maximize converter performance. The input impedance at this node is approximately 6.5 kΩ in parallel with 25 pF. Monolithic wideband operational amplifiers and closed loop buffers should be suitable for driving this input.

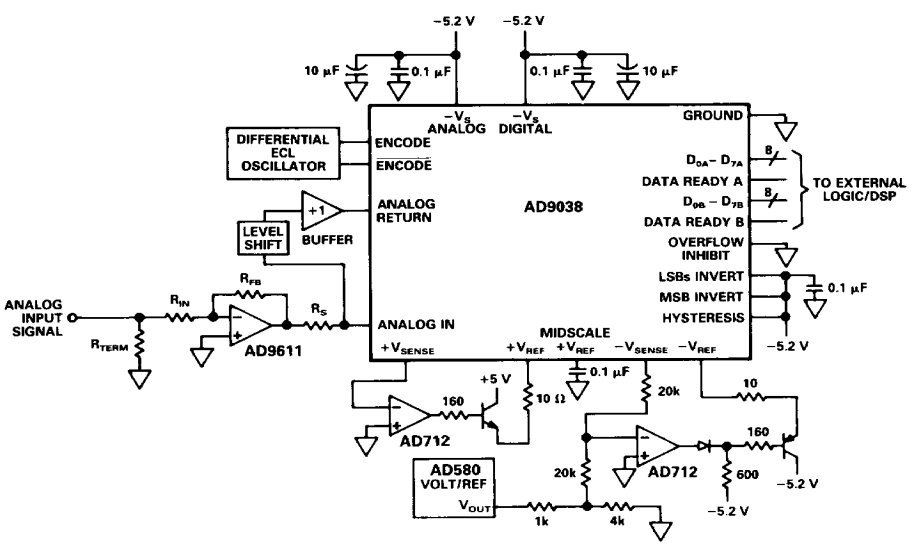


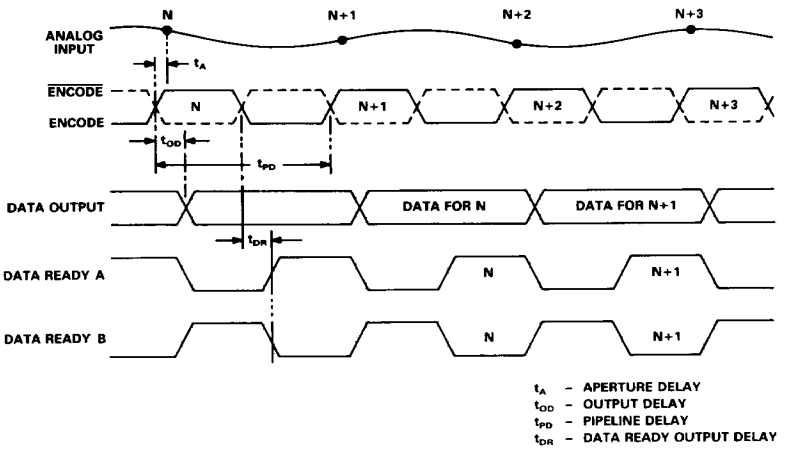
Figure 4. AD9038 Typical Application

Timing

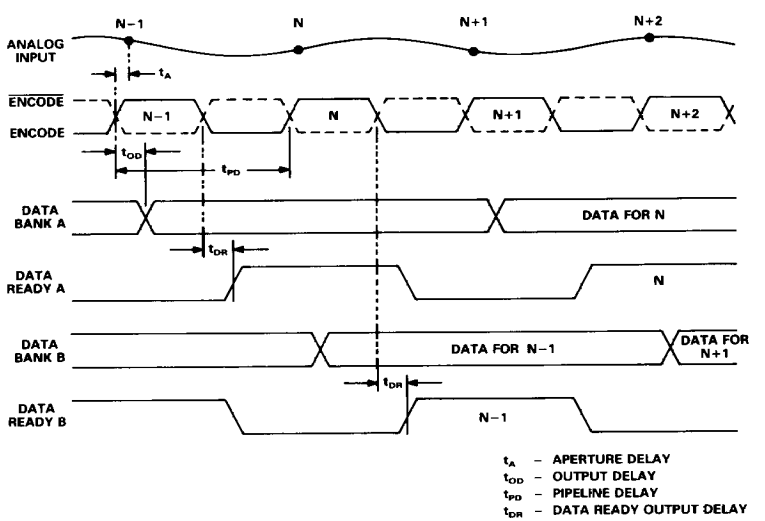
In the AD9028, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators. The falling edge of the ENCODE signal returns the comparators to track mode and triggers the Data Ready signal.

ENCODE and $\overline{\text{ENCODE}}$ are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal and allow optimum ac performance. In applications with a fixed, high frequency encode rate, converter performance is also improved (jitter reduced) by using a crystal oscillator as the system clock.

The AD9028 is designed to operate with a 50% duty cycle ENCODE signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE signal is driven differentially, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges, and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9028 package to avoid reflections.



AD9028 Timing Diagram



AD9038 Timing Diagram

Output data of the AD9028, D_{0A}–D_{7A} and OVERFLOW A, as well as the data ready signals, are also ECL compatible, and should be terminated through 100 Ω to −2 V (or an equivalent load). The output data can be latched on the rising edge of the DATA READY A output. For the AD9028, the DATA READY B output is simply the complement of DATA READY A.

Timing for the AD9038 is similar to the AD9028, except at the output, where the data is demultiplexed to two separate ports. Successive data samples alternate between the two ports, reducing the output data rate at either port to one-half the encode rate. Data at port A (D_{0A}–D_{7A} and OVERFLOW A) can be latched externally using the rising edge of DATA READY A. The rising edge of DATA READY B can be used to latch the data at port B (D_{0B}–D_{7B} and OVERFLOW B).

The data ready outputs for both the AD9028 and AD9038 are designed to track timing shifts over temperature.

Data Format

The format of the output data is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs and should be connected to GROUND or $-V_S$. The AD9028/AD9038 Truth Table gives information to choose among Binary, Inverted Binary, Twos Complement and Inverted Twos Complement coding.

The OVERFLOW INHIBIT pin controls how the converter handles overflow situations (ANALOG INPUT > $+V_{SENSE}$). For normal operation, the OVERFLOW INHIBIT is connected to $-V_S$, and the output data bits (D_{0A}–D_{7A} or D_{0B}–D_{7B}) will be at a logic LOW when ANALOG INPUT > $+V_{SENSE}$ (return to zero operation). The overflow bit (OVERFLOW A or OVERFLOW B) will indicate this condition with a logic HIGH. When the ANALOG INPUT is in range (< $+V_{SENSE}$), the overflow bit will remain at logic LOW.

If the OVERFLOW INHIBIT pin is connected to ground, the overflow bit will be disabled, and the output data will remain at logic high for overflow conditions. The overflow bits are not affected by the bit invert control pins (MSB INVERT and LSBs INVERT).

Layout and Power Supplies

Proper layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths matched to avoid propagation delay mismatch. Proper ECL terminations should be located near the packages of successive gates.

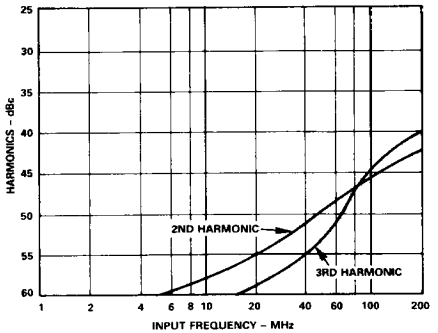
In high speed circuits, layout of the ground circuit is the most important factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground.

Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane.

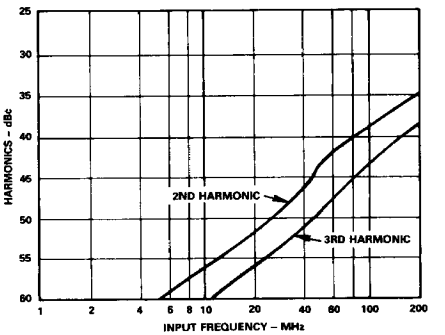
It is especially important to maintain the continuity of the ground plane under and around the AD9028/AD9038. If the system design separates the digital and analog grounds, analog ground is the preferred ground point for the A/D section of the system.

The tops of the AD9028/AD9038 packages are internally connected to the device substrates, and electrically connected to $-V_S$. The top of the package is designed to serve as a heat sink; the bottom of the package is not internally connected.

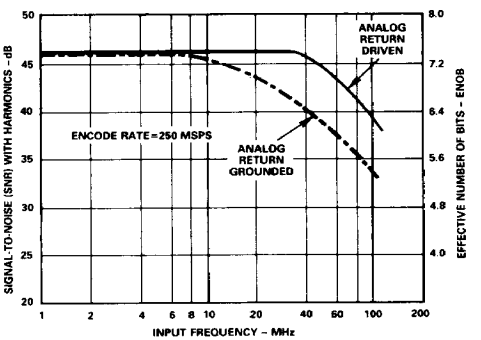
Sockets limit the dynamic performance and should be used only for prototypes or evaluation.



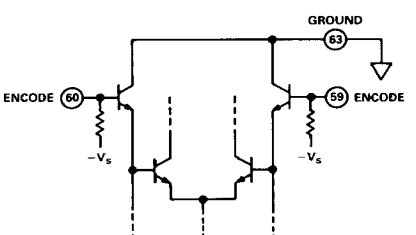
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Driven



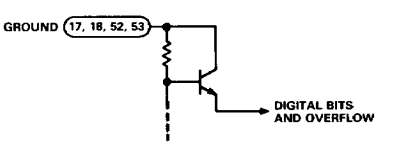
AD9028/AD9038 Harmonics vs. Input Frequency with Analog Return Grounded



AD9028/AD9038 SNR and ENOB vs. Input Frequency



Encode and $\overline{\text{Encode}}$ Equivalent Circuits

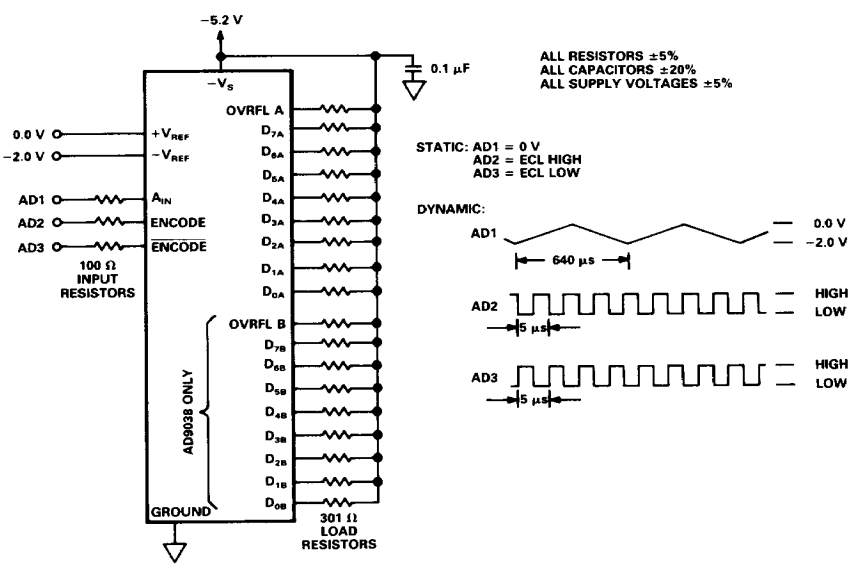


Equivalent Digital Outputs

Step	Range	Ovrfl. Inh.	Offset Binary		Twos Complement	
			True	Inverted	True	Inverted
	0 = −2 V FS = 0 V		MSB INV. = "0" LSBs INV. = "0"	MSB INV. = "1" LSBs INV. = "1"	MSB INV. = "1" LSBs INV. = "0"	MSB INV. = "0" LSBs INV. = "1"
256	≥0.000	"0"	(1)00000000	(1)11111111	(1)10000000	(1)01111111
256	≥0.000	"1"	(0)11111111	(0)00000000	(0)01111111	(0)10000000
255	−0.008	x	11111111	00000000	01111111	10000000
254	−0.016	x	11111110	00000001	01111110	10000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
129	−0.992	x	10000000	01111111	00000000	11111111
128	−1.000	x	01111111	10000000	11111111	00000000
127	−1.008	x	01111110	10000001	11111110	00000001
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
02	−1.992	x	00000010	11111101	10000010	01111101
01	−2.000	x	00000001	11111110	10000001	01111110
00	<−2.000	x	00000000	11111111	10000000	01111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT, LSBs INVERT, and OVERFLOW INHIBIT are considered dc controls.

AD9028/AD9038 Truth Table



AD9028/AD9038 Burn-In Diagram