ANALOG DEVICES

Low Cost, 16-Bit Accurate Sample-and-Hold Amplifier

AD1154

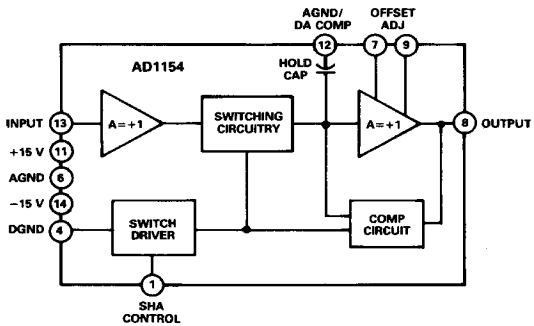
FEATURES

Low Nonlinearity: ±7.6 ppm max (1/2 LSB @ 16-Bit Accuracy)
Fast Acquisition Time to ±0.00076%: 3.5 μs
Low Droop Rate: 0.02 μV/μs
Aperture Jitter: 150 ps
±10 V Input Range
Hold Mode Feedthrough Rejection of −106 dB
14-Pin Metal DIP
Gain of +1 V/V
Low Cost

APPLICATIONS

Medical and Analytical Instrumentation
Automatic Test Equipment
Data Acquisition for Signal Processing
Simultaneous Sample-and-Hold
Peak Measurement Detection
Event Analysis

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1154 is a high accuracy, low cost sample-and-hold amplifier (SHA) designed to be used in high resolution data acquisition systems. It is complete with internal hold capacitor and proprietary capacitor trimmed compensation circuitry. Its accuracy (0.00076% of full scale range) and dynamic performance allow it to be used with high speed 16-bit A/D converters. The AD1154's low price enables users to upgrade the front end performance of 14-bit systems without increasing system cost. Its gain accuracy and droop rate in "hold" mode also allow accurate conversion by slower 16-bit A/D converters having conversion times of up to 7.6 ms.

The AD1154 is a hybrid noninverting sample-and-hold amplifier (SHA) with a gain of +1 V/V. It can be utilized in most inverting SHA applications by inverting the digital data. The AD1154 is packaged in a compact 14-pin metal DIP.

Typical applications for the AD1154 include data acquisition systems, strobed measurement systems, peak hold circuits and simultaneous sample-and-hold functions. The AD1154 is available in two grades, both operating over the −25°C to +85°C temperature range. The "A" grade is specified for 15-bit accurate systems, while the "B" grade offers superior performance for true 16-bit applications.

PRODUCT HIGHLIGHTS

1. Fast acquisition and low jitter make it the right choice for high speed, high accuracy data acquisition.
2. Its low droop rate (0.02 μV/μs) allows it to be used in slower systems without noticeable performance degradation.
3. The AD1154 is ideal for systems requiring wide dynamic range.
4. Low price reduces overall system cost.
5. Unity gain buffer architecture allows ease of use.

AD1154—SPECIFICATIONS (typical @ 25°C and nominal power supply of ±15 V unless otherwise noted)

Model	AD1154AW	AD1154BW	Units
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage (No Damage)	$\pm V_S$	*	V
Input Impedance	10^{12}	*	Ω
Input Capacitance	10	*	pF
DIGITAL INPUT (TTL COMPATIBLE)			
Sample Mode Logic "1"	2.0 min	*	V
Hold Mode Logic "0"	0.8 max	*	V
Logic "1" Current	1	*	μA
Logic "0" Current	3	*	μA
ANALOG OUTPUT			
Voltage ($R_{LOAD} \geq 2$ kΩ)	±10 min	*	V
Short Circuit Current	20	*	mA
Impedance	0.1	*	Ω @ 1 kHz
DC ACCURACY/STABILITY			
Gain	+1	*	V/V
Gain Error	±0.003 (±0.01 max)	*	%
Gain Temperature Coefficient	±0.1 (±1 max)	*	ppm/°C
Nonlinearity			
Sample Mode[1]	±0.0015	*	%
Hold Mode	±0.0015 max	±0.00076 max	%
Per mV of Offset Adjust (Hold Mode)	±0.3	*	ppm/mV
Offset Error (Adjustable to Zero)	±3 (±20 max)	*	mV
Offset Error @ T_{min}, T_{max}[2]	±0.6	*	mV
Offset Tempco per mV of Offset Adjust	±0.5	*	μV/°C/mV
SAMPLE MODE DYNAMICS			
Small Signal Bandwidth (−3 dB)	1	*	MHz
Full Power Bandwidth	120	*	kHz
Slew Rate	10	*	V/μs
Noise (dc to 1 MHz)	40	*	μV rms
SAMPLE-TO-HOLD SWITCHING			
Aperture Delay	80	*	ns
Aperture Uncertainty (Jitter)	150	*	ps
Offset Step (Pedestal)	±8	*	mV
Switching Transient			
Amplitude	±75	*	mV
Settling to ±0.003%	0.4	*	μs
Settling to ±0.00076%	1	*	μs
Dielectric Absorption Error (Uncompensated)	0.003	*	%
HOLD MODE DYNAMICS			
Droop Rate	0.2 (0.7 max)	0.1 (0.35 max)	μV/μs
Droop Rate @ T_{max}	5	2.5	μV/μs
Feedthrough Rejection (20 V p-p @ 10 kHz)	−106 (−96 max)	*	dB
HOLD-TO-TRACK SWITCHING			
Acquisition Time to ±0.00076% of 20 V[3]	5 (8 max)	3.5 (5 max)	μs
POWER REQUIREMENTS			
Nominal Voltage for Rated Performance (V_S)	±15 (±3%)	*	V
Power Supply Rejection	20	*	μV/V
Supply Current			
$+V_S$	10	*	mA
$-V_S$	10	*	mA
Power Dissipation	300	*	mW
TEMPERATURE RANGE			
Rated Performance	−25 to +85	*	°C
Storage	−40 to +125	*	°C
PACKAGE	14-Pin DIP	*	

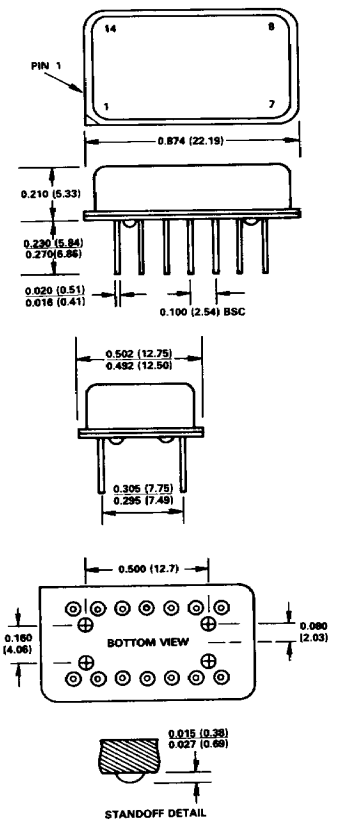
NOTE
[1]The AD1154 was designed specifically for 16-bit accurate sample/hold applications (tailored for hold mode performance), but it may be used as a track-and-hold amplifier with 15-bit accurate tracking performance.
[2]Error at +25°C adjusted to zero.
[3]Tested with 5 kΩ load.
*Specification same as AD1154AW.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

14-LEAD METAL PLATFORM DIP



PIN DESIGNATIONS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SHA CONTROL	8	SHA OUTPUT
2	NO CONNECTION	9	OFFSET ADJUST
3	NO CONNECTION	10	NO CONNECTION
4	DIGITAL GROUND	11	+15 V
5	NO CONNECTION	12	ANA GND/DA COMP
6	ANALOG GROUND	13	SHA INPUT
7	OFFSET ADJUST	14	−15 V

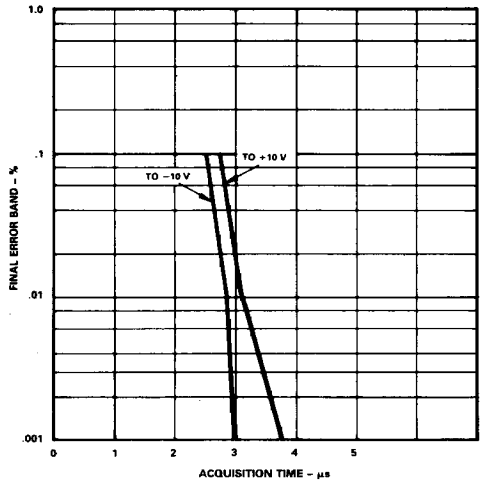


Figure 1. Acquisition Time vs. Final Error Band for 20 Volt Step

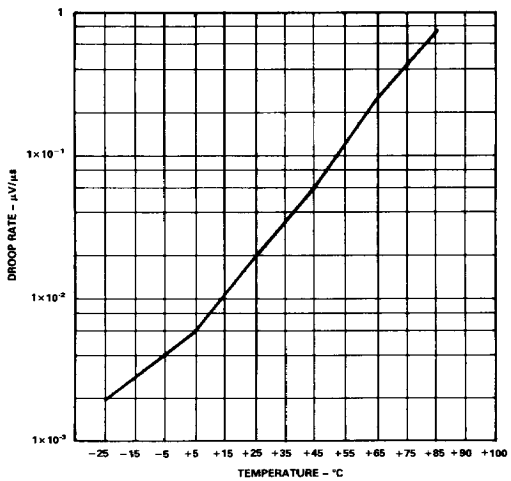


Figure 2. Droop Rate vs. Temperature

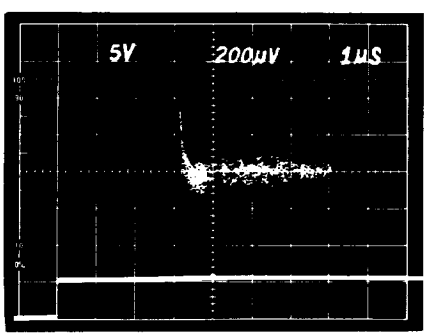


Figure 3. Hold-to-Sample Acquisition Time

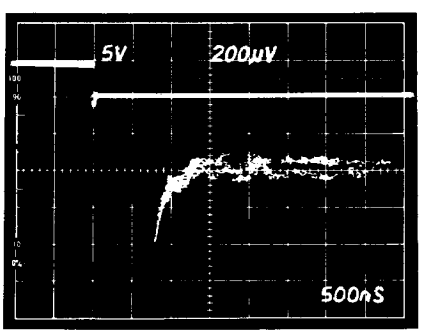


Figure 4. Sample-to-Hold Settling Time

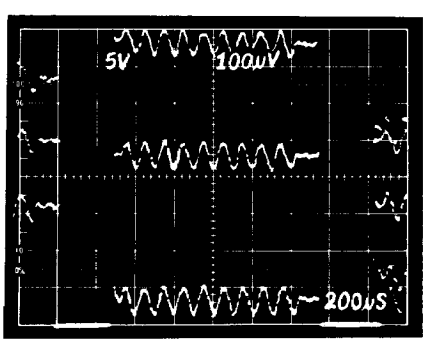


Figure 5. Input Feedthrough

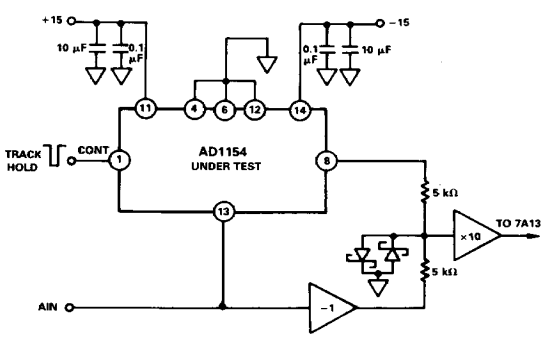


Figure 6. Acquisition Time Test Circuit

TERMINOLOGY

Accuracy is the peak deviation of the output from a straight line through the endpoints of the transfer function. It is expressed as a percentage of the full scale output range. Note that this parameter is measured in hold mode because the actual voltage to be converted is the voltage present at the output of the device during the hold mode.

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample/track command has been given assuming that the input amplifier has settled. This includes switch delay time, slewing time and settling time for a given output voltage change.

Aperture Time is the time required after the hold command for the switch to open fully. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter is the range of variation in the aperture time. If the aperture time is "tuned out" by advancing the hold command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution.

Charge Transfer (or offset step or pedestal) is the charge transferred to the storage capacitor when switching to the hold mode.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB.

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in hold. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

Switching Transient Settling Time is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

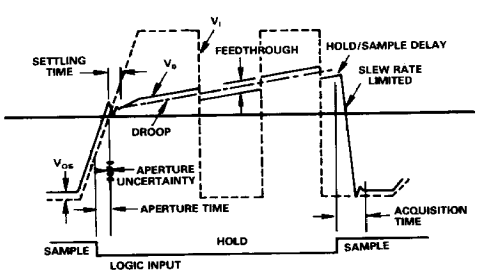


Figure 7. T/H Characteristics

INVERTING VS. NONINVERTING ARCHITECTURE

The AD1154 has a gain of +1 V/V. Many S/H amplifiers use an inverting architecture and hence have a gain of −1 V/V. The AD1154, because of its noninverting architecture, does not have an externally accessible summing point. This pin is found on most inverting S/Hs and is typically not used. In applications where the summing junction is not connected, the AD1154 can be used as a direct hardware replacement by tying Pin 12 to ground, but the output is of opposite polarity.

GROUNDING CONSIDERATIONS

The AD1154 is a true 16-bit performance sample/hold amplifier. In order to insure proper operation of the device, great care must be taken in managing the ground tracks. It is recommended that Pins 4, 6 and 12 of the AD1154 be tied together directly outside of the package. This point should then be tied to the analog ground of the A/D converter, as shown in Figure 8. This track should be as short and wide as possible to minimize voltage drops. Also note from the figure that any other analog grounds in the signal path should be joined to the A/D converter analog ground.

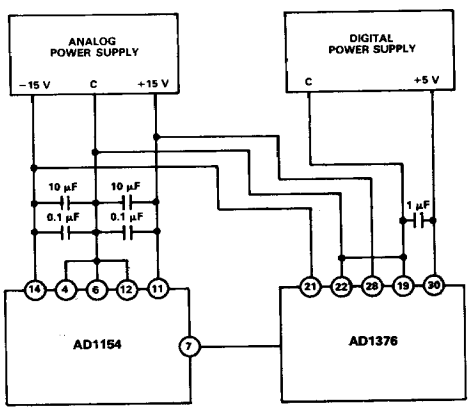


Figure 8. Basic Grounding and Power Supply Bypassing Practice

DIELECTRIC ABSORPTION COMPENSATION

The hold capacitor used in the AD1154 is a high quality ceramic chip capacitor. This capacitor's dielectric absorption characteristics are typically better than high quality film capacitors. In addition, the AD1154 provides a means for compensating for the dielectric absorption of the capacitor if better performance is required. If dielectric absorption compensation is not used, Pin 12 should be tied to ground. Please refer to the section titled "DISCUSSION OF DIELECTRIC ABSORPTION" for more detailed information.

POWER SUPPLY BYPASSING

The AD1154 utilizes high speed amplifiers in its design. These amplifiers require quiet power supplies that are free from spikes. For maximum performance it is recommended that both power supplies be bypassed with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors located as close to the device as possible (see Figure 8).

DISCUSSION OF DIELECTRIC ABSORPTION

The hold capacitor of the AD1154 was chosen for its low dielectric absorption (D.A.) characteristics. D.A. is directly affected by the sample/hold mode switching durations and input levels. The AD1154 provides the user with a pin for external D.A. compensation circuitry. The AD1154's uncompensated D.A. performance is inherently superior, and in most applications the D.A. compensation pin should be connected to ground. Where additional compensation is desired to tailor the AD1154 to a specific user's application, only three resistors and a capacitor are required to optimize the AD1154's D.A. performance (see Figure 11).

If a capacitor is charged to a voltage, discharged for a moderate period of time, and then open circuited, the voltage on the capacitor will begin to creep back towards its initial value. This creep voltage is known as dielectric absorption. Dielectric absorption occurs because the dielectric material doesn't polarize instantly, the molecules need time to align themselves. As a result, not all of the energy stored in a capacitor can be quickly recovered upon discharge.

A first order model of the hold capacitor to include dielectric absorption effects is shown in Figure 9. In addition to the main capacitance, C_M, and the insulation resistance, R_I, there is an

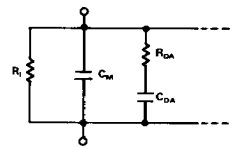


Figure 9. First Order Model of D. A. Effects

R_{DA} and a C_{DA}. When the capacitor is charged to some value, C_{DA} is also charged. When the capacitor is discharged, C_{DA} also discharges. But it must discharge through R_{DA}, and, if the capacitor is not discharged for a long enough period of time, C_{DA} will not completely discharge. As a result, when the capacitor is open circuited, C_{DA} will discharge into C_M causing the voltage across it to creep back towards its initial value. The actual model of the capacitor should contain additional R_{DA}s and C_{DA}s with increasing time constants in parallel with the one shown.

Figure 10 shows a circuit suitable for measuring the dielectric absorption of sample/hold amplifiers. The circuit operates as follows: R1 and C1 set the frequency of the SHA control; R2 and C2 set the amount of acquisition time allowed for the SHA. See the timing diagram of Figure 10.

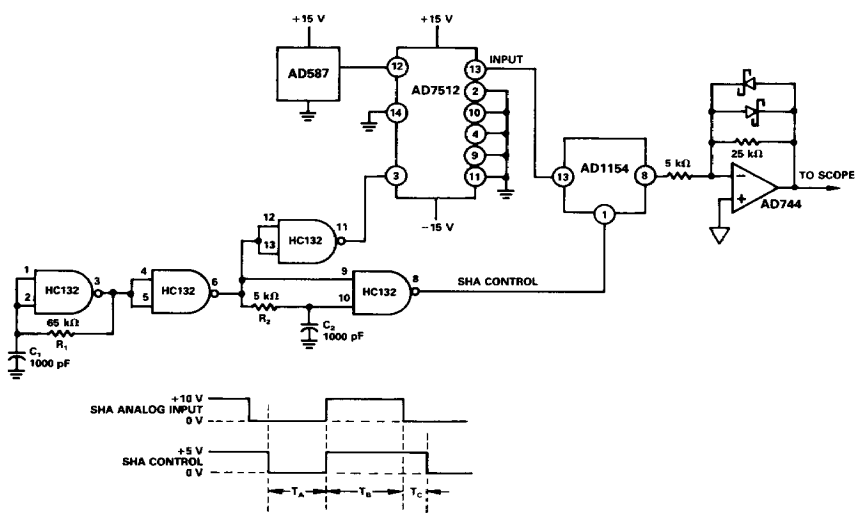


Figure 10. Dielectric Absorption Measurement Circuit

During T_B, the CONTROL line is high, the AD1154 is in the sample mode and the analog input charges the hold capacitor to +10 V. During T_C the analog input to the SHA is switched to ground, effectively shorting the hold capacitor for the remainder of the sample period. During T_A, the SHA is switched into hold mode and the hold capacitor is open circuited. The dielectric rebound can be observed on the oscilloscope during T_A. Refer to Figure 12.

Note that the dielectric absorption error is dependent on several factors: it is a function of how long the capacitor is charged (T_B), how long it is discharged (T_C) and how long it is observed while open circuited (T_A). These parameters can be modified by changing R1, R2, C1 and C2.

The AD1154 provides a pin to compensate for dielectric absorption. To use it, the circuit of Figure 11 must be employed.

To find the optimum values for R1, R2, R3 and C1 follow this procedure:

1. Adjust the D.A. measurement circuit (see Figure 10) to represent a typical sampling rate.
2. Observe the dielectric absorption error on the oscilloscope.
3. Pick (R1||R2) • C1 to be equal to the approximate time constant (T_{const}) of the dielectric rebound on the oscilloscope (see photo in Figure 12).

4. R3 is used to adjust the magnitude of the compensation. To find an initial approximation for R3, the following relationship can be used:
   $R3 = [\text{Magnitude of D.A. error} \times (R1+R2)]/10 \times 1/(e^{-T_C/T_{CONST}} - e^{-T_A/T_{CONST}})$
5. R3 can then be fine trimmed for the flattest output during hold.

Using this method it is possible to reduce the effect of dielectric absorption by a factor of four or five. The typical values for resistors and capacitor given in Figure 11 are for a sample time of 20 μs, acquisition time of 5 μs and a hold time of 20 μs. When determining the values, R3 should be less than 10 Ω, and C1 should be as small as possible.

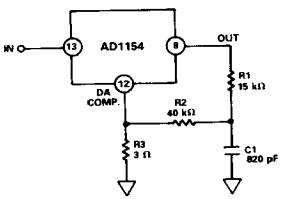


Figure 11. D/A Compensation Circuit with Typical Values

DYNAMIC SIGNALS

The primary purpose of using a sample/hold in front of an A/D converter is to hold the input constant while the A/D performs its conversion. Without a sample/hold, a 16-bit A/D converter would not be able to accurately digitize any signal whose slew rate exceeded 1 LSB divided by the conversion time. Or, for a 15 μs A/D with an input range of ±10 V this says:

Input Signal Slew $Rate_{MAX}$ = 1 LSB ÷ Conversion Time = 20.3 V/S

Since the maximum slew rate of a sinusoid is defined as:

Slew $Rate_{MAX}$ = 2 • π • Amplitude • Frequency

This translates into a maximum input frequency of:

$F_{IN\ MAX}$ = Slew $Rate_{MAX}$ ÷ (2 • π • Amplitude) = 0.32 Hz

By using a sample/hold, however, the maximum slew rate of the input signal is now limited by the aperture jitter of the sample/hold, which is usually orders of magnitude better than a conversion time. Specifically, for an AD1154 the analysis is:

Input Signal Slew $Rate_{MAX}$ = 1 LSB ÷ Aperture Jitter = 2.035 V/μs.

Now the maximum input frequency becomes:

$F_{IN\ MAX}$ = Slew $Rate_{MAX}$ ÷ (2 • π • Amplitude) = 32.4 kHz.

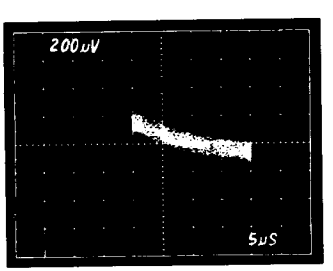


Figure 12. Dielectric Absorption

This represents a dramatic improvement over using the A/D converter by itself. The AD1154's 222 kHz throughput ($1/(T_{ACQ} + T_{SETT})$) and 150 ps aperture jitter allow it to digitize input signals of up to 32 kHz to 16-bit accuracy or up to a 128 kHz signal to 14-bits.

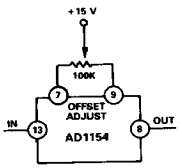


Figure 13. Offset Adjust Circuit

OPERATING INSTRUCTIONS

Offset Adjust

In most data acquisition systems only one offset adjustment is made. Usually the offset adjust of the A/D converter is used to null the combined system offsets. However, the offset or pedestal of the AD1154 can be nulled by connecting a trim potentiometer between Pins 7 and 9, and tying the wiper to +15 V (refer to Figure 13.) To null the pedestal, ground the input of the SHA and toggle the SHA CONTROL. Then adjust the pot until the output of the SHA in hold mode reads 0 V. Please note that each millivolt of offset adjust adjustment degrades linearity by 0.3 ppm.

APPLICATIONS

50kHz Sampling A/D System

Figure 14 shows a typical connection of the AD1154 to the AD1376 (16-bit 15.5 μs A/D converter). This combination will result in an A/D conversion system capable of sampling a 25 kHz signal at a 50 kHz throughput rate. (Where Throughput Rate = $T_{ACQ} + T_{SETTLE} + T_{CONV}$ = 3.5 μs + 1 μs + 15.5 μs = 20 μs.) This example has an input range of ±10 V, power consumption of < 1 W and 16-bit resolution. The accuracy of this system is limited to the AD1376's 14-bit performance.

Track-and-Hold

The AD1154's design is optimized for sample-and-hold applications and is internally compensated to guarantee 16-bit (0.00076%) hold mode gain nonlinearity. Even though the AD1154 is tailored specifically as a SHA, it may be used as a track-and-hold amplifier providing 15-bit (0.0015%) track mode gain nonlinearity.

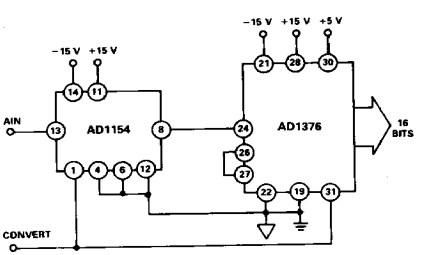


Figure 14. 50 kHz Sampling A/D Conversion System