Octal Sample-and-Hold with Multiplexed Input

SMP-18

FEATURES
High Speed Version of SMP-08
Internal Hold Capacitors
Low Droop Rate
TTL/CMOS Compatible Logic Inputs
Single or Dual Supply Operation
Break-Before-Make Channel Addressing
Compatible With CD4051 Pinout
Low Cost

APPLICATIONS
Multiple Path Timing Deskew for A.T.E.
Memory Programmers
Mass Flow/Process Control Systems
Multichannel Data Acquisition Systems
Robotics and Control Systems
Medical and Analytical Instrumentation
Event Analysis
Stage Lighting Control

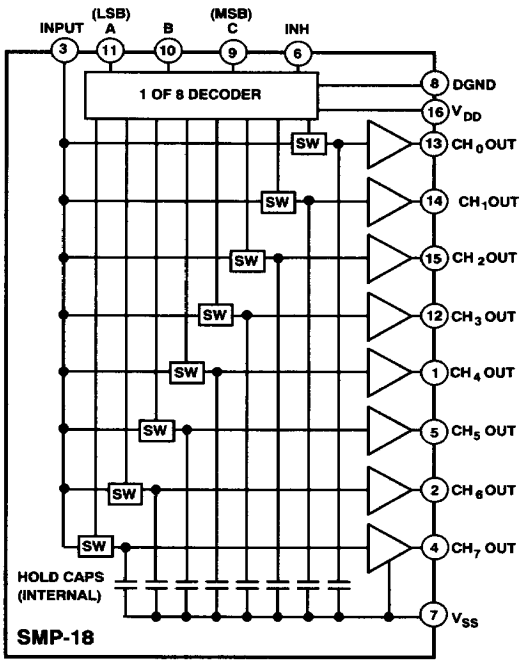
GENERAL DESCRIPTION

The SMP-18 is a monolithic octal sample-and-hold; it has eight internal buffer amplifiers, input multiplexer, and internal hold capacitors. It is manufactured in an advanced oxide isolated CMOS technology to obtain high accuracy, low droop rate, and fast acquisition time. The SMP-18 has a typical linearity error of only 0.01% and can accurately acquire a 10-bit input signal to ±1/2 LSB in less than 2.5 microseconds. The SMP-18's output swing includes the negative supply in both single and dual supply operation.

The SMP-18 was specifically designed for systems that use a calibration cycle to adjust a multiple of system parameters. The low cost and high level of integration make the SMP-18 ideal for calibration requirements that have previously required an ASIC, or high cost multiple D/A converters.

The SMP-18 is also ideally suited for a wide variety of sample-and-hold applications including amplifier offset or VCA gain adjustments. One or more SMP-18s can be used with single or multiple DACs to provide multiple set points within a system.

FUNCTIONAL BLOCK DIAGRAM



The SMP-18 offers significant cost and size reduction over discrete designs. It is available in a 16-pin hermetic or plastic DIP or surface mount SOIC package. The SMP-18 is a higher speed direct replacement for the SMP-08.

4

SMP-18 SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V, V_{SS} = −5 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		−3 V ≤ V_{IN} ≤ +3 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 0 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 0 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 0 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 0 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 0 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 0 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	−3.0		+3.0	V
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, −3 V to +3 V to 0.1%		3.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate	SR			6		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		−3 V to +3 V Step		−72		dB
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	V_{SS} = ±5 V to ±6 V	60	75		dB
Supply Current	I_{DD}	T_A = +25°C		5.5	7.5	mA
		−40°C ≤ T_A ≤ +85°C		7.5	9.5	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with t_r = t_f = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +12 V, V_{SS} = 0 V, DGND = 0 V, R_L = No Load, T_A = −40°C to +85°C for SMP-18F, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Linearity Error		60 mV ≤ V_{IN} ≤ 10 V		0.01		%
Buffer Offset Voltage	V_{OS}	T_A = +25°C, V_{IN} = 6 V		2.5	10	mV
		−40°C ≤ T_A ≤ +85°C, V_{IN} = 6 V		3.5	20	mV
Hold Step	V_{HS}	V_{IN} = 6 V		4	6	mV
Droop Rate	$\Delta V_{CH}/\Delta t$	T_A = +25°C, V_{IN} = 6 V		2	40	mV/s
Output Source Current	I_{SOURCE}	V_{IN} = 6 V[1]	1.2			mA
Output Sink Current	I_{SINK}	V_{IN} = 6 V[1]	0.5			mA
Output Voltage Range		R_L = 20 kΩ	0.06		10.0	V
		R_L = 10 kΩ	0.06		9.5	
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V_{INH}		2.4			V
Logic Input Low Voltage	V_{INL}				0.8	V
Logic Input Current	I_{IN}	V_{IN} = 2.4 V		0.5	1	µA
DYNAMIC PERFORMANCE[2]						
Acquisition Time	t_{AQ}	T_A = +25°C, 0 to 10 V to 0.1%		2.5		µs
Hold Mode Settling Time	t_H	To ±1 mV of Final Value		1		µs
Channel Select Time	t_{CH}			90		ns
Channel Deselect Time	t_{DCS}			45		ns
Inhibit Recovery Time	t_{IR}			90		ns
Slew Rate[3]	SR			7		V/µs
Capacitive Load Stability		<30% Overshoot		500		pF
Analog Crosstalk		0 to 10 V Step		−72		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY CHARACTERISTICS						
Power Supply Rejection Ratio	PSRR	$10.8\ V \le V_{DD} \le 13.2\ V$	60	75		dB
Supply Current	I_{DD}	$T_A = +25°C$		6.0	8.0	mA
		$-40°C \le T_A \le +85°C$		8.0	10.0	mA

NOTES
[1]Outputs are capable of sinking and sourcing over 10 mA but offset is guaranteed at specified load levels.
[2]All input control signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[3]Slew rate is measured in the sample mode with a 0 to 10 V step from 20% to 80%.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to DGND . . . . . −0.3 V, 17 V
V_{DD} to V_{SS} . . . . . −0.3 V, 17 V
V_{LOGIC} to DGND . . . . . −0.3 V, V_{DD}
V_{IN} to DGND . . . . . V_{SS}, V_{DD}
V_{OUT} to DGND . . . . . V_{SS}, V_{DD}
Analog Output Current . . . . . ±20 mA
(Not short-circuit protected)
Operating Temperature Range
FQ, FP, FS . . . . . −40°C to +85°C
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
16-Pin Hermetic DIP (Q)	94	12	°C/W
16-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOIC (S)	92	27	°C/W

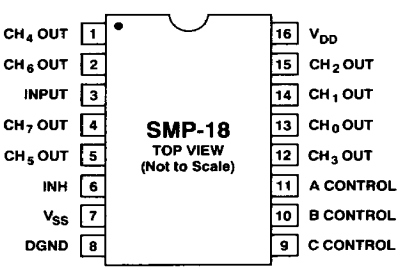
NOTES
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

4

CAUTION

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to the above maximum rating conditions for extended periods may affect device reliability.
2. Digital inputs and outputs are protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam or packaging at all times until ready to use. Use proper antistatic handling procedures.
3. Remove power before inserting or removing units from their sockets.

PIN CONNECTIONS

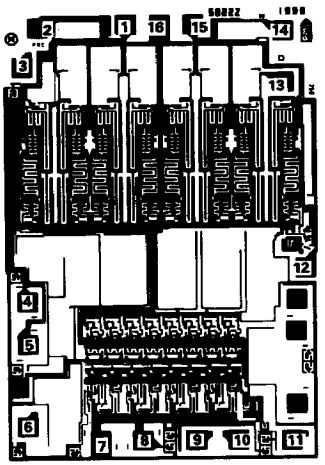


ORDERING GUIDE*

Package: 16-Pin DIP/SOIC		Operating
Cerdip 16-Pin	Plastic 16-Pin	Temperature Range
TBA†		MIL
SMP-18FQ	SMP-18FP	XIND
	SMP-18FS	XIND

NOTES
*Burn-in is available on industrial temperature range parts in cerdip and plastic DIP packages.
†Consult factory for 883 data sheet.

DICE CHARACTERISTICS



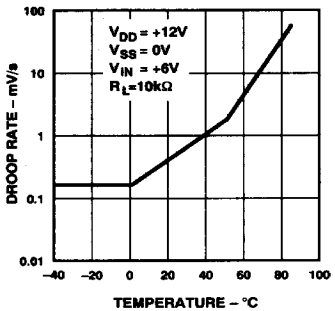
DIE SIZE 0.080 x 0.120 INCH, 9,600 sq. mils
(2.032 x 3.048 mm, 6.193 sq. mm)

1. CH_4 OUT
2. CH_6 OUT
3. INPUT
4. CH_7 OUT
5. CH_5 OUT
6. INH
7. V_{SS}
8. DGND
9. C CONTROL
10. B CONTROL
11. A CONTROL
12. CH_3 OUT
13. CH_0 OUT
14. CH_1 OUT
15. CH_2 OUT
16. V_{DD}

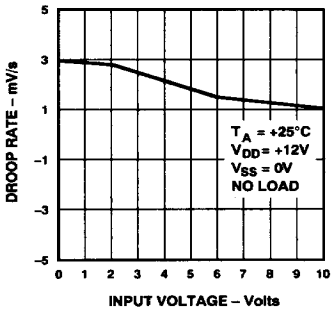
WAFER TEST LIMITS (@ V_{DD} = +12 V, V_{SS} = DGND = 0 V, R_L = No Load, T_A = +25°C for SMP-18GBC, unless otherwise specified)

Parameter	Symbol	Conditions	Limits	Units
Buffer Offset Voltage	V_{OS}	V_{IN} = +6 V	20	mV max
Droop Rate	$\Delta V_{CH}/\Delta t$	V_{IN} = +6 V	40	mV/s max
Output Source Current	I_{SOURCE}	V_{IN} = +6 V	1.2	mA min
Output Sink Current	I_{SINK}	V_{IN} = +6 V	0.5	mA min
Output Voltage Range		R_L = 20 kΩ	0.06/10.0	V max/min
		R_L = 10 kΩ	0.06/9.5	V max/min
LOGIC CHARACTERISTICS				
Logic Input High Voltage	V_{INH}		2.4	V min
Logic Input Low Voltage	V_{INL}		0.8	V max
Logic Input Current	I_{IN}	V_{IN} = 2.4 V	1	μA max
SUPPLY CHARACTERISTICS				
Power Supply Rejection Ratio	PSRR	10.8 V ≤ V_{DD} ≤ 13.2	60	dB min
Supply Current	I_{DD}		8.0	mA max

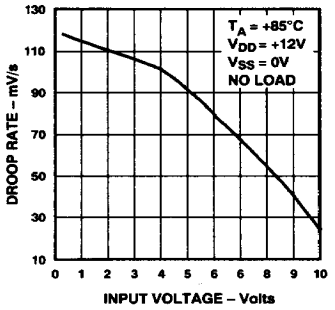
NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.



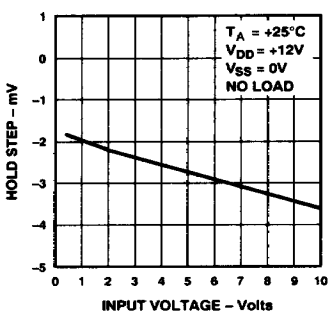
Droop Rate vs. Temperature



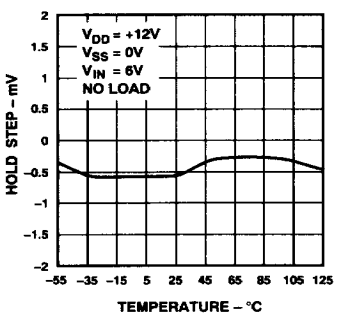
Droop Rate vs. Input Voltage



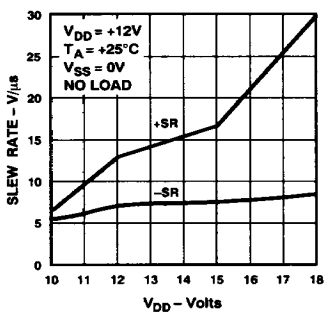
Droop Rate vs. Input Voltage



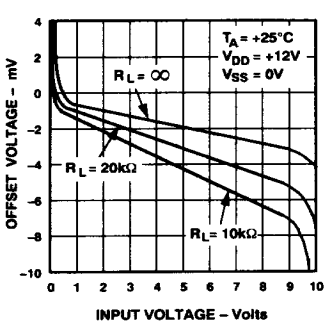
Hold Step vs. Input Voltage



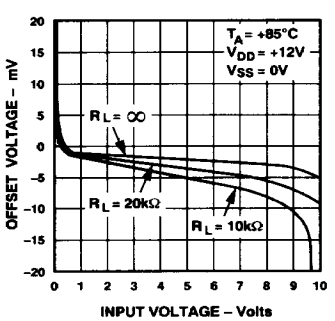
Hold Step vs. Temperature



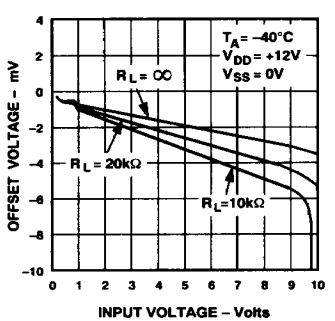
Slew Rate vs. V_{DD}



Offset Voltage vs. Input Voltage

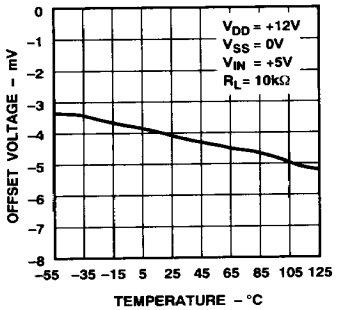


Offset Voltage vs. Input Voltage

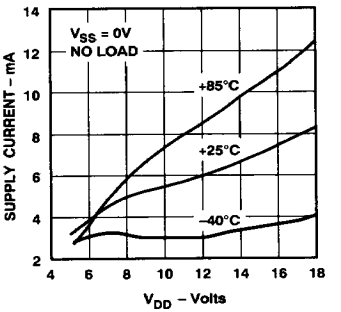


Offset Voltage vs. Input Voltage

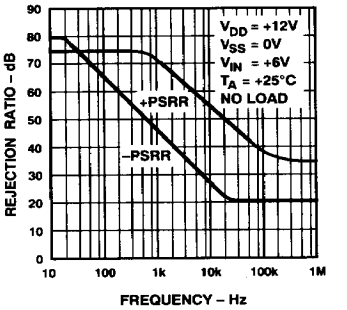
SMP-18—Typical Performance Characteristics



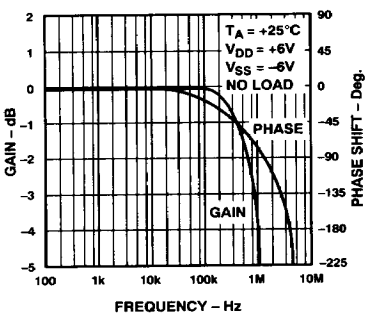
Offset Voltage vs. Temperature



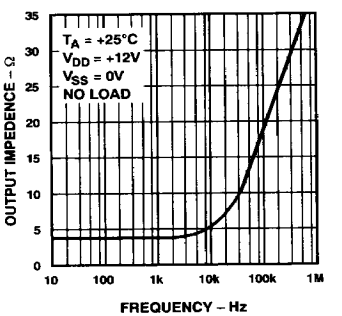
Supply Current vs. V_{DD}



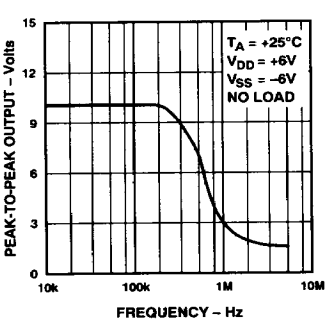
Sample Mode Power Supply Rejection



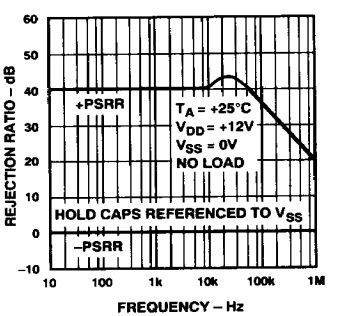
Gain, Phase Shift vs. Frequency



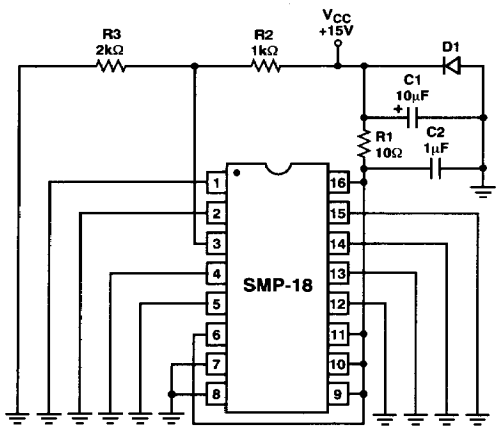
Output Impedance vs. Frequency



Maximum Output Voltage vs. Frequency



Hold Mode Power Supply Rejection



Burn-in Circuit

APPLICATIONS INFORMATION

The SMP-18, a multiplexed octal S/H, minimizes board space in systems requiring cycled calibration or an array of control voltages. When used in conjunction with a low cost 10-bit D/A, the SMP-18 can easily be integrated into microprocessor based systems. Since the SMP-18 features break-before-make switching and an internal decoder, no external logic is required. The SMP-18 has an internally regulated TTL supply so that TTL/CMOS compatibility is maintained over the full supply range. See Figure 1 for channel decode address information.

POWER SUPPLIES

The SMP-18 is capable of operating with either single or dual supplies, over a voltage range of 7 to 15 volts. Based on the supply voltages chosen, V_{DD} and V_{SS} establish the output voltage range, which is:

$$(V_{SS} + 0.06\ V) \leq V_{OUT} \leq (V_{DD} - 2\ V)$$

Note that several specifications, including acquisition time, offset and output voltage, compliance will degrade for supply voltages of less than 7 V.

If split supplies are used, the negative supply should be bypassed with a 0.1 μF capacitor in parallel with a 10 μF to ground. The internal hold capacitors are connected to this supply pin and any noise will appear at the outputs.

In single supply applications, it is extremely important that the V_{SS} (negative supply) pin is connected to a clean ground. The hold capacitors are internally tied to the V_{SS} (negative) rail. Any ground noise or disturbance will directly couple to the output of the sample-and-hold, degrading the signal-to-noise performance. The analog and digital ground traces on the circuit board should be physically separated to reduce digital switching noise from entering the analog circuitry.

POWER SUPPLY SEQUENCING

V_{DD} should be applied to the SMP-18 before the logic input signals. The SMP-18 has been designed to be immune to latch-up, but standard precautions should still be taken.

OUTPUT BUFFERS (Pins 1, 2, 4, 5, 12, 13, 14, 15)

The buffer offset specification is 10 mV; this is less than 1/2 LSB of an 8-bit DAC with 10 V full scale. The hold step (magnitude of step caused in the output voltage when switching from sample-to-hold mode, also referred to as the pedestal error or sample-to-hold offset) is about 4 mV with little variation over the full output voltage range. The droop rate of a held channel is 2 mV/s typical and 40 mV/s maximum.

The buffers are designed to drive loads connected to ground. The outputs can source more than 20 mA, over the full voltage range, but have limited current sinking capability near V_{SS}. In split supply operation, symmetrical output swings can be obtained by restricting the output range to 2 V from either supply.

On-chip SMP-18 buffers eliminate potential stability problems associated with external buffers; outputs are stable with capacitive loads up to 500 pF. However, since the SMP-18's buffer outputs are not short circuit protected, care should be taken to avoid shorting any output to the supplies or ground.

SIGNAL INPUT (Pin 3)

The signal input should be driven from a low impedance voltage source such as the output of an op amp. The op amp should have a high slew rate and fast settling time if the SMP-18's acquisition time characteristics are to be maintained. As with all CMOS devices, all input voltages should be kept within range of the supply rails ($V_{SS} \leq V_{IN} \leq V_{DD}$) to avoid the possibility of latch-up. If single supply operation is desired, op amps such as the OP-21, OP-80, or OP-90 that have input and output voltage compliances including ground, can be used to drive the inputs. Split supplies, such as ±7.5 V, can be used with the SMP-18.

APPLICATION TIPS

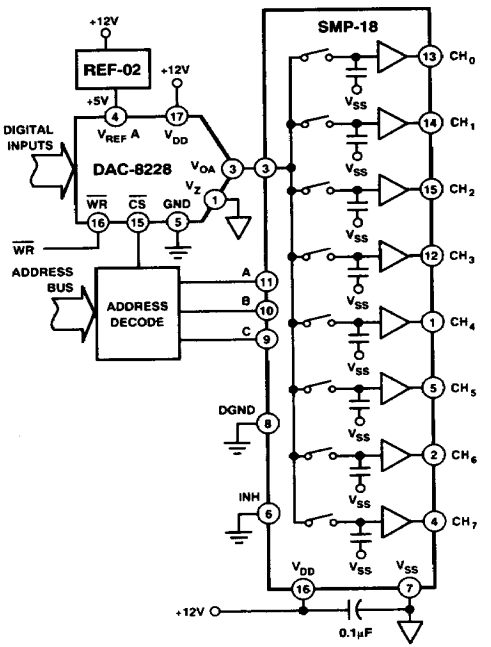
All unused digital inputs should be connected to logic LOW. For analog inputs that may become temporarily disconnected, a resistor to V_{DD}, V_{SS} or analog ground should be used with a value ranging from 200 kΩ to 1 MΩ.

Do not apply signals to the SMP-18 with power off unless the input current is limited to less than 10 mA.

TYPICAL APPLICATIONS

An 8-Channel Multiplexed D/A Converter

Figure 1 illustrates a typical multiplexing function of the SMP-18. It is used to sample-and-hold eight different output voltages corresponding to eight different digital codes from a D/A converter. The SMP-18's droop rate of 40 mV/s requires a refresh once every 250 ms before the voltage drifts beyond 1/2 LSB accuracy (1 LSB of an 8-bit DAC is equivalent to 19.5 mV, out of a full-scale voltage of 5 V). For a 10-bit DAC, the refresh rate must be less than 60 ms, and for a 12-bit system, 15 ms. This implementation is very cost effective compared to using multiple DACs as the number of output channels increases.



CHANNEL DECODING

PIN 9 C	PIN 10 B	PIN 11 A	PIN 6 INH	CH	PIN
0	0	0	0	0	13
0	0	1	0	1	14
0	1	0	0	2	15
0	1	1	0	3	12
1	0	0	0	4	1
1	0	1	0	5	5
1	1	0	0	6	2
1	1	1	0	7	4
X	X	X	1	NONE	–

Figure 1. 8-Channel Multiplexed D/A Converter