MOTOROLA

MC74F2970/ Am2970

MEMORY TIMING CONTROLLER

Advance Information

MEMORY TIMING CONTROLLER

The MC74F2970 will be dual marked with the AMD part number Am2970 to indicate plug-in compatibility. Dual marking will also apply to the MC74F2968A referred to in this data sheet. Both devices will be referred to as MC74F2970 and MC74F2968A in the remainder of this specification.

DESCRIPTION — The MC74F2970 is a high performance Memory Timing Controller (MTC). The MC74F2970 is designed to be used in memory systems which use the MC74F2968A Dynamic Memory Controller (DMC). All control signals needed by the DMC are generated by the MC74F2970 MTC.

The MC74F2970 uses a delay line to provide maximum flexibility to the memory system designer, allowing achievement of maximum performance. The delay line is the timing reference from which the MTC generates the control signals.

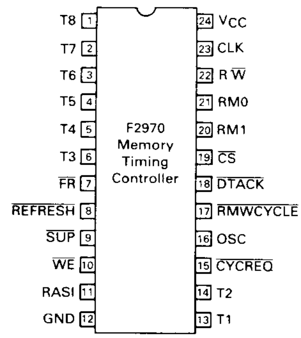
The MC74F2970 provides an internal refresh interval timer to generate refresh requests independent of the CPU. This guarantees proper refresh timing under all combinations of CPU and DMA requests.

The MC74F2970 will be supplied in 24-lead, 300 mil plastic and ceramic DIP packages as well as 28-lead PLCC packages.

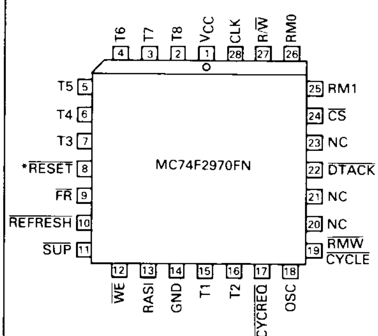
The MC74F2970:

- Provides complete timing control for 64K/256K DRAM memory systems in configurations up to 1 Megaword by 16 bits utilizing the MC74F2968A DMC.
- Supports extended cycle timing needed for byte-write operations
- Internal or external control of refresh
- Burst (up to 512 cycle), distributed, or hidden refresh
- Memory access/refresh request arbitration

CONNECTION DIAGRAMS
Top View



N Suffix — Case 724-02 (Plastic)
J Suffix — Case 758-01 (Ceramic)



FN Suffix — Case 776-02 (PLCC)

*RESET input available only in PLCC

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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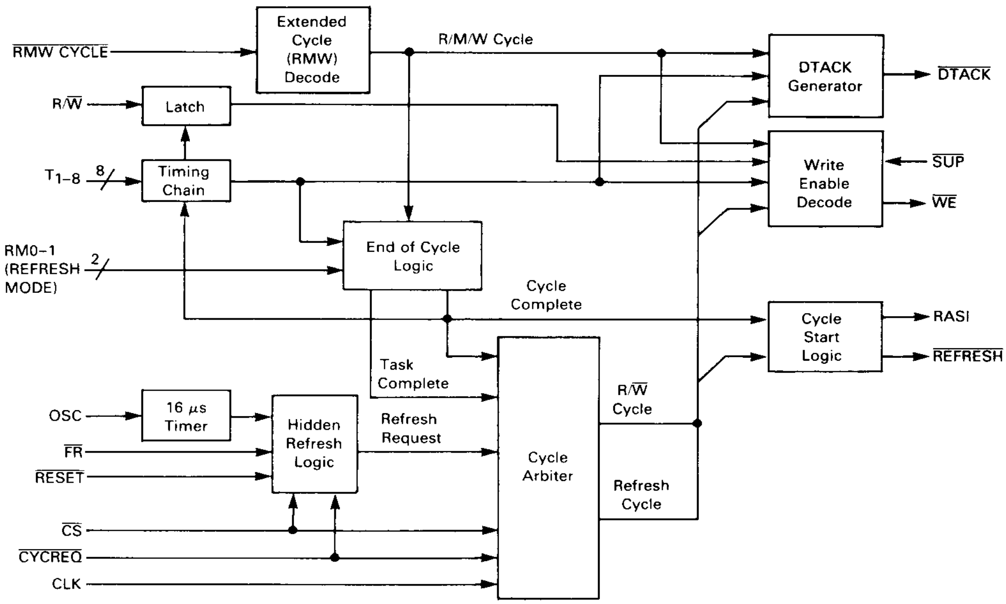
F2970 DYNAMIC MEMORY TIMING CONTROLLER
BLOCK DIAGRAM



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PIN DESCRIPTION

Name	I/O	Description
CS	I	When CHIP SELECT is low, it indicates that the bank/board controlled by the F2970 is selected and enabled. A memory read/write cycle can only be performed when CS is active, while refresh cycles are independent of CS. When CS is HIGH, all memory requests (HIGH-to-LOW transition of CYCREQ) will be interpreted as 'Hidden Refresh' requests.
CYCREQ	I	When CS is LOW, this input will generate an internal memory request for the F2970 on the HIGH-to-LOW transition of CYCREQ.
DTACK	O	The HIGH-to-LOW transition of DTACK informs the CPU that a write cycle has begun, or that valid data will be on the system bus at the correct time during a read cycle.
FR	I	This input is used to force a refresh cycle at user-designated times. The falling edge of FR latches an internal refresh request. If the memory is busy, the refresh is done at the completion of the current cycle.
REFRESH	O	This output, when low, indicates that a refresh cycle will be performed. It should be connected to the MC1 input of the F2968A Dynamic Memory Controller. The MC0 input of the DMC should be tied low.
OSC	I	This input, when connected to an external R/C circuit is used to generate an internal refresh clock. If FR is not active, the oscillator will initiate the refresh cycles.
RM0, RM1	I	The REFRESH MODE inputs control the type of refresh cycle the F2970 will perform, as described in Table 1.
CLK	I	For systems requiring synchronous arbitration of memory access and refresh requests, this input would receive the system clock. For asynchronous arbitration, this input must be tied high.
RASI	O	The ROW ADDRESS STROBE drives the delay line and the RASI input of the DMC. The rising edge initiates a memory access for the DMC and starts the timing reference.
R/W	I	This input indicates a memory read request when HIGH, and a write request when LOW.

PIN DESCRIPTION

Name	I/O	Description
$\overline{SUP}$	I	When $\overline{SUPPRESS}$ is driven LOW, it inhibits access to memory by disabling $\overline{WE}$. It can be used to prevent illegal access in memory-access protected systems.
$\overline{WE}$	O	$\overline{WRITE\ ENABLE}$, when LOW, causes data to be written to memory. $\overline{WE}$ is inhibited if $\overline{SUP}$ is LOW. This output can drive a 500 pF load.
$\overline{RMWCYCLE}$	I	This input, when LOW, indicates that the current cycle is a read-modify-write cycle. The F2970 will adjust the necessary timing for an extended cycle. This input is not latched and must be valid for the entire memory cycle, given that it meets the set-up time with respect to the first timing tap that is driven by the delay-line.
T1–T8	I	These inputs are the positive-edge triggered timing tap outputs from the timing reference (delay-line). They provide the necessary timing information for the F2970 to control memory cycles. The definition of the eight timing taps is given in Table 2.
$\overline{RESET}$	I	This input is provided only in the PLCC package. It is intended to be connected to the $\overline{RESET}$ signal of the processor, so that the F2970 is reset during the system initialization sequence when $\overline{RESET}$ is LOW. The functioning of the different modes of operation is not affected when $\overline{RESET}$ is HIGH.

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ARCHITECTURE

The MC74F2970 Memory Timing Controller replaces much of the MSI "glue" logic which is commonly necessary in controlling dynamic memory systems. It is responsible for controlling/arbitrating memory access, refresh, and hand shaking with the processor. The MTC also provides an extended (Read-Modify-Write) cycle which is needed for byte operations.

These tasks are performed by the following functions in the block diagram.

Memory Access Control:
Cycle Arbiter
Cycle Start Logic
Timing Chain Logic
$\overline{WE}$ Decode
End of Cycle Logic

Refresh Support:
Refresh Timer
Hidden Refresh Logic

Processor Interface:
$\overline{DTACK}$ Logic

CYCLE ARBITER

This circuitry determines whether a refresh or a read/write cycle is to be performed. If a refresh and read/write cycle are requested at the same time, the read/write cycle is performed first followed by the refresh cycle.

The arbiter can be synchronous through the use of the CLK input. In this mode, the $\overline{CYCREQ}$ and refresh inputs are examined on the negative edge of the CLK input.

The arbiter can also function asynchronously (with the CLK input tied HIGH). In this mode, the first memory request to occur will be serviced, but not until after an internal delay to avoid metastable states.

CYCLE START LOGIC

This block decodes the internal state of the F2970 and initiates a memory cycle by asserting RASI. Before the memory cycle is started, this block indicates which type of access the F2968A Dynamic Memory Controller will perform via the $\overline{REFRESH}$ output.

TIMING CHAIN LOGIC

Since timing information is only contained in the positive edge of the Timing tap inputs, (an output is asserted on the positive edge of Tx and negated on the positive edge of Ty) this block conditions these inputs into usable signals for the various decode blocks.

It is possible to have 2 positive transitions on some timing inputs during an extended cycle preceded by a normal cycle. To facilitate design, the F2970 will only recognize the following sequence of positive transitions on the extended cycle timing inputs:

T4: $\overline{WE}$ asserted
T7: Reset of RASI
T8: End of extended cycle

For example, a positive edge of T8 before a positive edge on T4 will be ignored.

$\overline{WE}$ DECODE (OR WRITE ENABLE DECODE)

This block decodes the internal states of the F2970 and asserts $\overline{WE}$ on T3 for write cycles or T4 for read-modify-write cycles. $\overline{WE}$ is forced HIGH if $\overline{SUP}$ is LOW.

END OF CYCLE LOGIC

This block determines when a memory cycle or memory task is complete. A memory cycle will end on the positive edge of T6 or T8, depending on whether a normal or extended (read-modify-write) cycle is being executed. Normally, a memory task consists of a single memory access. However, this block also contains counter logic to keep track of multiple access tasks such as burst refreshes.

REFRESH TIMER

This block provides an on-chip refresh interval timer whose frequency is determined by an external RC network. If the refresh clock is provided via the $\overline{FR}$ input, the internal oscillator may be disabled by connecting the OSC pin to ground.

HIDDEN REFRESH LOGIC

This block determines the source of the internal refresh clock which could be either the FR input, or the output of the internal oscillator. In addition, this block will also assert "hidden refresh" requests under certain conditions.

A complete description of the refresh modes is covered under System Considerations.

DTACK LOGIC

This logic decodes the type of memory access and asserts DATA TRANSFER ACKNOWLEDGE (DTACK) at the appropriate time. DTACK is asserted on T1 for normal read/write cycles and on T2 for read-modify-write cycles. DTACK is negated when CYCREQ is taken HIGH.

SYSTEMS CONSIDERATIONS

The F2970 allows maximum performance and flexibility for dynamic memory systems. It receives and arbitrates memory access requests, initiates the read/write cycles and handshakes with the processor.

The MTC performs four types of memory cycles — read, write, refresh and read-modify-write. The timing of these cycles is shown in Figures 3 through 10.

Other types of memory access such as Nibble Mode, Page Mode and Static Column are possible by adding additional "glue" logic.

SYNCHRONOUS versus ASYNCHRONOUS ARBITRATION

The F2970 arbitrates between processor (read/write) and refresh requests for a memory cycle. Synchronous arbitration requires that the inputs requiring memory, FR and CYCREQ, be clocked into the F2970. In many applications, the phase relationship of the system block to the FR and CYCREQ inputs may change to the point where setup and hold time requirements cannot be guaranteed. In these instances, asynchronous arbitration (CLK tied HIGH) can be used. Timing for synchronous and asynchronous arbitration can be found in Figures 3 and 4.

REFRESH OPERATIONS

The MTC can support a variety of refresh schemes. The type of refresh is controlled via the RM0, RM1 and FR inputs. Basic refresh types include distributed, or a 128, 256, or 512 cycle burst. It has to be noted that any burst refresh request will be ignored while the F2970 is servicing consecutive processor requests.

The internal refresh clock is equivalent to the FR input, or the output of the internal oscillator as follows:

- In the burst mode of operation, the FR input is always the refresh clock.
- The FR input can also be used as the refresh clock in the distributed refresh (non-burst) mode. However, the internal oscillator takes over as the refresh clock if it goes through three cycles without a LOW level appearing on the FR input. This provision allows the primary refresh clock (FR) to be interrupted while it is in the HIGH logic state, and for refresh operations to be resumed at the internal oscillator frequency.
- It is also possible to use the on-chip oscillator as the refresh clock in the distributed refresh mode. In this case, the FR input should be tied HIGH. However, since the on-chip oscillator is asynchronous to the external CLK input, it is necessary to provide a synchronous refresh clock via the FR input if synchronous arbitration is desired.

The F2970 has the ability to increase memory bandwidth by inserting refresh requests when the processor is accessing other devices or I/O (CYCREQ = LOW, CS = HIGH). A hidden refresh can only be performed once every refresh clock period, and occurs only with distributed refreshing. When a hidden refresh is performed, the F2970 will skip the next refresh request. (See Figure 1.)

Depending on the system configuration and operation, it is possible for the DRAM to appear "static" providing that a hidden refresh can be performed every refresh clock period.

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FIGURE 1 — HIDDEN REFRESH CYCLE

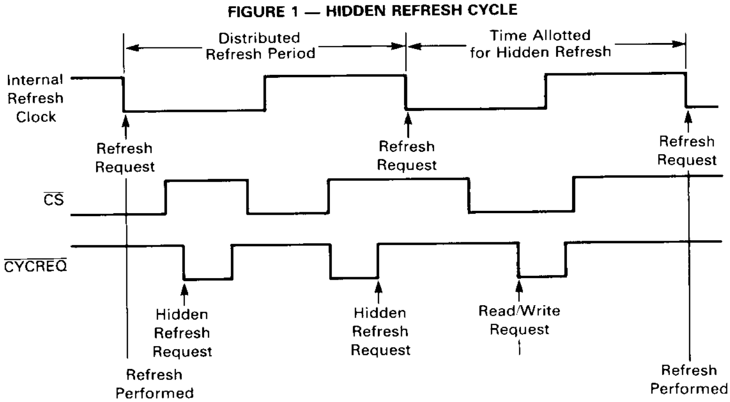


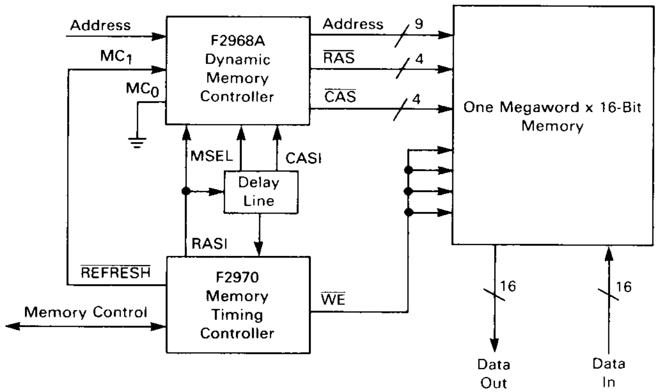
TABLE 1 — REFRESH MODES

RM1	RM0	Refresh Mode
0	0	Not Burst (Distributed)
0	1	128-Cycle Burst
1	0	256-Cycle Burst
1	1	512-Cycle Burst

TABLE 2 — TIMING TAP DEFINITION

Tap No.	Function
T1	Controls when $\overline{DTACK}$ will go active during read cycles.
T2	Controls when $\overline{DTACK}$ will go active during read-modify-write cycles.
T3	Indicates when valid data is available on the memory bus during write cycles.
T4	Indicates when valid data is available on the memory bus during read-modify-write cycles.
T5	Controls the rising edge of $\overline{RAS}$ (falling edge of RASI) on read, write and refresh cycles.
T6	Indicates that a new memory cycle may begin after a read, write or refresh cycle. (T5 + trp)
T7	Controls the rising edge of $\overline{RAS}$ (falling edge of RASI) on read-modify-write cycles.
T8	Indicates that a new memory cycle may begin after a read-modify-write cycle. (T7 + trp)

FIGURE 2 — ONE MEGAWORD DYNAMIC MEMORY SYSTEM



MAXIMUM RATINGS

Rating	Symbol	Value	Units
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (Except OSC)	V_{in}	−0.5 to +5.5	V
Output Voltage $\overline{DTACK}$	V_{out}	−0.5 to +5.5	V
Output Voltage (all others)	V_{out}	−0.5 to V_{CC} value	V
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	140	°C

THERMAL CHARACTERISTICS

Characteristics	Package	Symbol	Value	Units
Thermal Resistance	24-Ld Plastic	θ_{JA}	50	°C/W
	24-Ld Ceramic		50	
	28-Ld PLCC		50	

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature	0	25	70	°C

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Max	Units	Test Conditions	
V_{IH}	Input HIGH Voltage Except OSC		2.0		V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage Except OSC			0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage on All Outputs Except $\overline{DTACK}$		2.4		V	V_{CC} = MIN, I_{OH} = −1.0 mA	
V_{OL}	Output LOW Voltage	$\overline{WE}$		0.5	V	V_{CC} = MIN	I_{OL} = 2.4 mA
				0.8			I_{OL} = 12 mA
		Others		0.5	V		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	$\overline{SUP}$, $\overline{CS}$		40	μA	V_{CC} = MAX	V_{IN} = 2.7 V
		Others Except OSC		20			
		All Except OSC		100			V_{IN} = 5.5 V
I_{IL}	Input LOW Current	$\overline{SUP}$, $\overline{CS}$		−800	μA	V_{CC} = MAX	V_{IN} = 0.5 V
		Others Except OSC		−400			
I_{OS}	Output Short Circuit Current (1)		−50	−250	mA	V_{CC} = MAX	V_{OUT} = 0 V
I_{CC}	Supply Current			125	mA	V_{CC} = MAX	OSC Input LOW All Others HIGH
I_{OX}	Output HIGH Current on $\overline{DTACK}$ Output			250	μA	V_{CC} = MIN	V_{OH} = 5.5 V

(1) Not more than one output should be shorted at a time

AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE (C_L = 50 pF unless otherwise specified)

Test No.	Symbol	Path From	Path To	Ref. Fig.	System Operating Conditions	Min	Max
1	t_{PLH}	CLK High-to-Low	RASI	3, 5	Synchronous Read/Write Cycles		23
2		$\overline{CYCREQ}$ High-to-Low		6	Asynchronous Read/Write Cycles		30
3		T6 Low-to-High		3	Async. Back-to-Back Cycles ($\overline{RMWCYCLE}$ = 1)		46
4		T8 Low-to-High		3	Async. Back-to-Back Cycles ($\overline{RMWCYCLE}$ = 0)		50
5	t_{PHL}	T5 Low-to-High	RASI	3	All modes ($\overline{RMWCYCLE}$ = 1)		21
6		T7 Low-to-High		3	All modes ($\overline{RMWCYCLE}$ = 0)		23
7	t_{SKEW}	$\overline{REFRESH}$ High-to-Low	RASI Low-to-High	3, 7	All Refresh Cycles	18	
8		$\overline{REFRESH}$ Low-to-High	RASI High-to-Low	3, 7	All Refresh Cycles	5	
9	t_{PHL}	T1 Low-to-High	$\overline{DTACK}$	5, 6	Read/Write Cycles ($\overline{RMWCYCLE}$ = 1)		16
10		T2 Low-to-High		5, 6	Read/Write Cycles ($\overline{RMWCYCLE}$ = 0)		16
11	t_{PLH}	$\overline{CYCREQ}$ Low-to-High	$\overline{DTACK}$	5, 6	Read/Write Cycles		31

AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE — continued (C_L = 50 pF unless otherwise specified)

Test No.	Symbol	Path From	Path To	Ref. Fig.	System Operating Conditions		Min	Max
12	t_{PHL}	T3 Low-to-High	$\overline{WE}$	5, 6	Write Cycle $\overline{RMWCYCLE}$ = 1	C_L = 50 pF		13
						C_L = 150 pF		21
						C_L = 500 pF		31
13	t_{PHL}	T4 Low-to-High	$\overline{WE}$	5, 8	Write Cycle $\overline{RMWCYCLE}$ = 0	C_L = 50 pF		13
						C_L = 150 pF		21
						C_L = 500 pF		31
14	t_{PLH}	T5 Low-to-High	$\overline{WE}$	5, 6	Write Cycle $\overline{RMWCYCLE}$ = 1	C_L = 50 pF		24
						C_L = 150 pF		30
						C_L = 500 pF		40
15	t_{PLH}	T7 Low-to-High	$\overline{WE}$	5, 8	Write Cycle $\overline{RMWCYCLE}$ = 0	C_L = 50 pF		32
						C_L = 150 pF		38
						C_L = 500 pF		48
16	t_{PHL}	$\overline{CYCREQ}$ High-to-Low	$\overline{REFRESH}$	9	Async. Hidden Refresh Cycles			44
17	t_{PHL}	CLK High-to-Low	$\overline{REFRESH}$	7	Sync. Refresh Cycles			18
18	t_{PHL}	$\overline{FR}$ High-to-Low	$\overline{REFRESH}$	8	Async. Refresh Cycles			44
19	t_{PHL}	T6 Low-to-High	$\overline{REFRESH}$	4	Back-to-Back Refresh Cycles ($\overline{RMWCYCLE}$ = 1)			46
20	t_{PHL}	T8 Low-to-High	$\overline{REFRESH}$	4	Back-to-Back Refresh Cycles ($\overline{RMWCYCLE}$ = 0)			46
21	t_{SET}	$\overline{CS}$ High-to-Low	$\overline{CYCREQ}$ High-to-Low	5, 6	Read/Write Cycles		0	
22	t_{SET}	$\overline{CS}$ Low-to-High	$\overline{CYCREQ}$ High-to-Low	9	Hidden Refresh Cycles		0	
23	t_{HOLD}	$\overline{CS}$ Low-to-High	$\overline{CYCREQ}$ Low-to-High	5, 6	Read/Write Cycles		5	
24	t_{HOLD}	$\overline{CS}$ High-to-Low	$\overline{CYCREQ}$ High-to-Low		Hidden Refresh Cycles		26	
25	t_{SET}	$\overline{CYCREQ}$ High-to-Low	CLK High-to-Low	4, 5	Read/Write Cycles		18	
26	t_{SET}	$\overline{CYCREQ}$ High-to-Low	CLK High-to-Low		Hidden Refresh Cycles		32	
27	t_{SET}	$\overline{FR}$ High-to-Low	CLK High-to-Low	7	Forced Refresh Cycles		34	
28	t_{SET}	T6 Low-to-High	CLK High-to-Low		Back-to-Back Cycles $\overline{RMWCYCLE}$ = 1		35	
29	t_{SET}	T8 Low-to-High	CLK High-to-Low		Back-to-Back Cycles $\overline{RMWCYCLE}$ = 0		35	
30	t_{SET}	R/$\overline{W}$ (1 or 0)	T3 Low-to-High	5, 6	All modes		4	
31	t_{HOLD}	R/$\overline{W}$ (1 or 0)	T3 Low-to-High	5, 6	All modes		10	
32	t_{SET}	$\overline{SUP}$ (1 or 0)	T3 Low-to-High	5, 6	Write Cycles $\overline{RMWCYCLE}$ = 1		5	
33	t_{SET}	$\overline{SUP}$ (1 or 0)	T4 Low-to-High	5, 8	$\overline{RMWCYCLE}$ = 0		5	
34	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T5 Low-to-High	5, 8	Write Cycles $\overline{RMWCYCLE}$ = 1		22	
35	t_{HOLD}	$\overline{SUP}$ (1 or 0)	T7 Low-to-High	5, 8	$\overline{RMWCYCLE}$ = 0		28	
36	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T1 Low-to-High				21	
37	t_{SET}	$\overline{RMWCYCLE}$ (1 or 0)	T2 Low-to-High				16	

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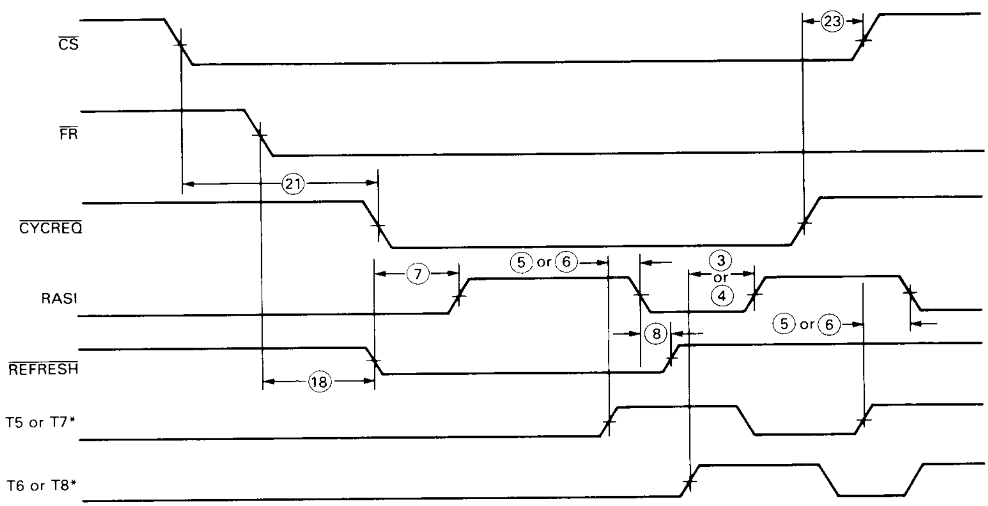
AC CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE — continued (C_L = 50 pF unless otherwise specified)

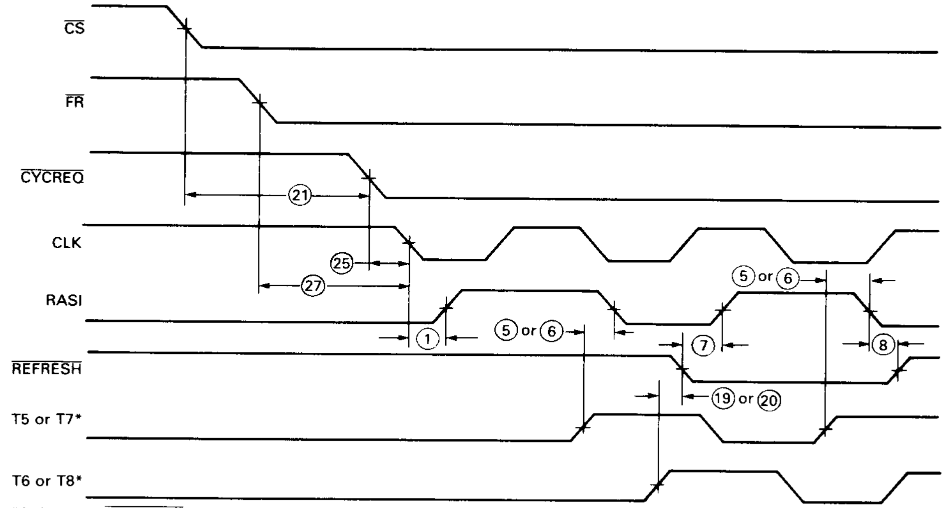
Test No.	Symbol	Path From	Path To	Ref. Fig.	System Operating Conditions	Min	Max
38	t_{SET}	$\overline{\text{RMWCYCLE}}$ (1 or 0)	T3 Low-to-High	5, 6		10	
39	t_{SET}	$\overline{\text{RMWCYCLE}}$ (1 or 0)	T4 Low-to-High	5, 6		10	
40	t_{SET}	T4 Low-to-High	T7 Low-to-High	8	$\overline{\text{RMWCYCLE}}$ = 0	15	
41	t_{SET}	T7 Low-to-High	T8 Low-to-High	8	$\overline{\text{RMWCYCLE}}$ = 0	15	
42	t_{PW}	T1–T8 High		8	All Cycles	10	
43	t_{PW}	$\overline{\text{FR}}$ High		8	Forced Refresh Cycles	15	
44	t_{PW}	CLK High or Low		5	All Synchronous Cycles	10	
45	t_{PW}	$\overline{\text{CYCREQ}}$ Low		9	Hidden Refresh Cycles	15	

FIGURE 3 — ASYNCHRONOUS ARBITRATION



*Active when $\overline{\text{RMWCYCLE}}$ 0

FIGURE 4 — SYNCHRONOUS ARBITRATION



*Active when RMWCYCLE = 0

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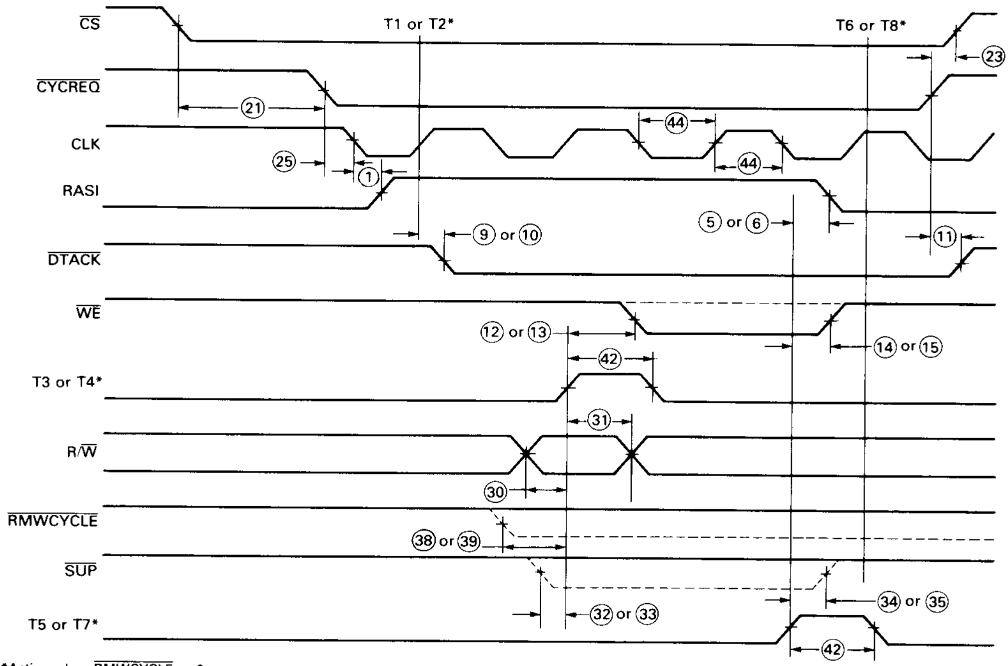
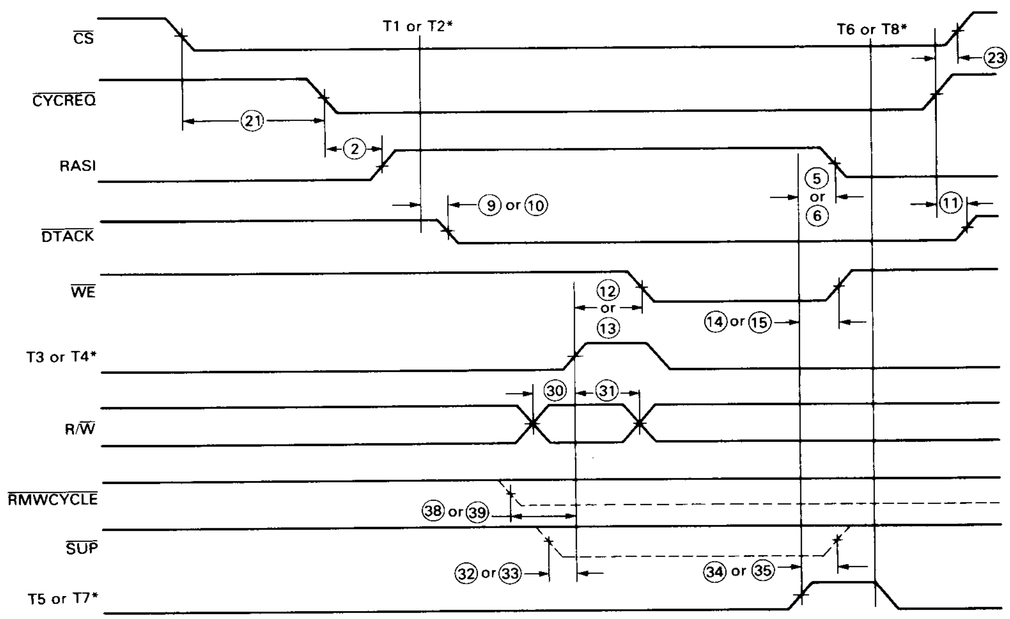
FIGURE 5 — SYNCHRONOUS READ/WRITE



*Active when RMWCYCLE = 0

FIGURE 6 — ASYNCHRONOUS READ/$\overline{WRITE}$



*Active when $\overline{RMWCYCLE}$ = 0

FIGURE 7 — SYNCHRONOUS FORCED REFRESH (SHOWN WHEN $\overline{RMWCYCLE}$ = 1)

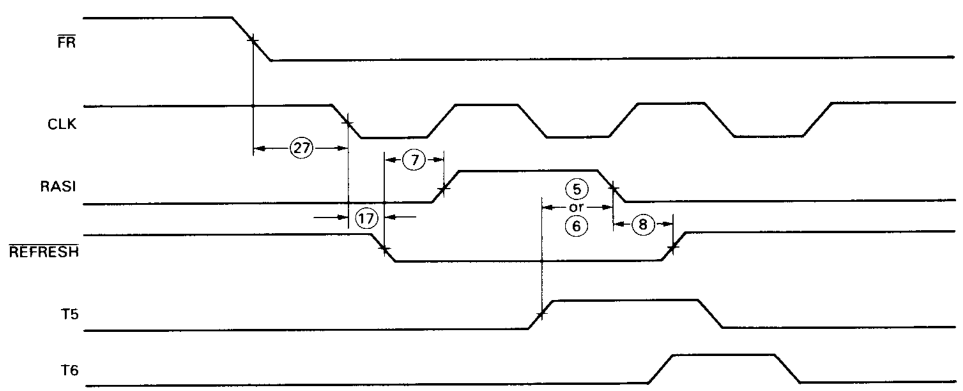


FIGURE 8 — ASYNCHRONOUS FORCED REFRESH
(SHOWN WHEN $\overline{RMWCYCLE}$ = 0)

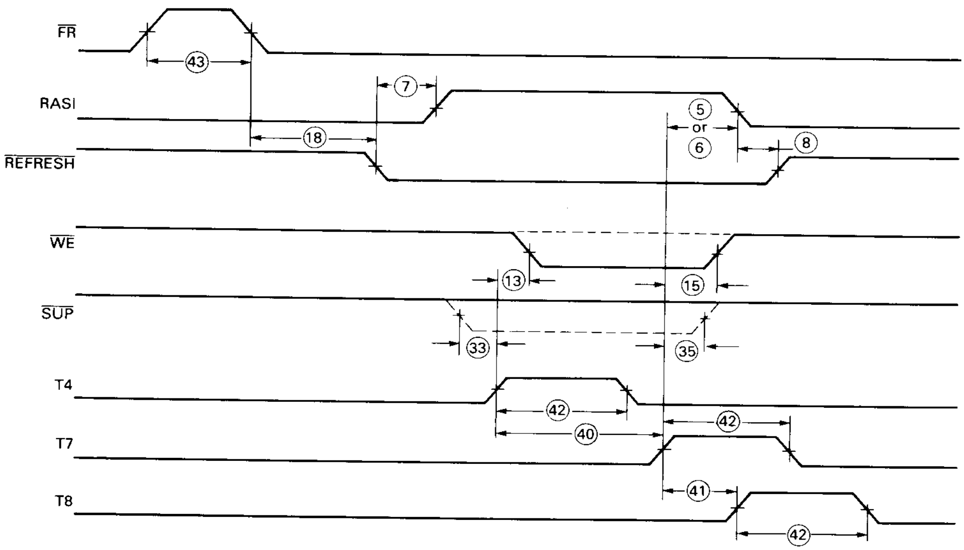


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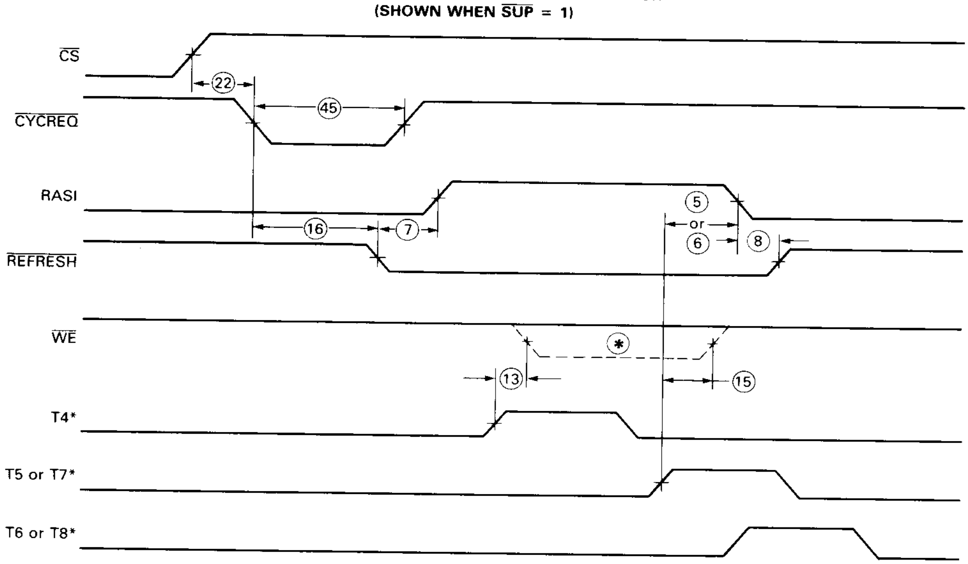
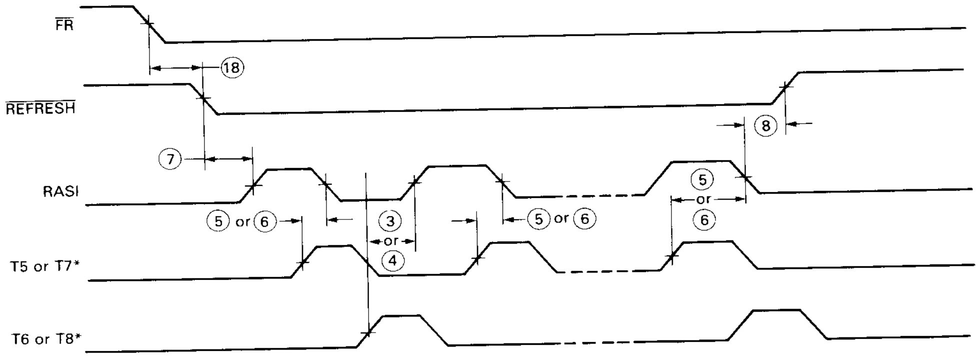
FIGURE 9 — ASYNCHRONOUS HIDDEN REFRESH
(SHOWN WHEN $\overline{SUP}$ = 1)



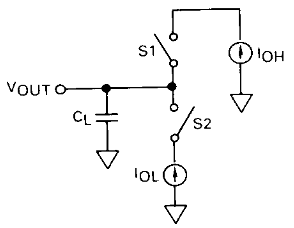
*Active when $\overline{RMWCYCLE}$ = 0

FIGURE 10 — ASYNCHRONOUS BURST REFRESH

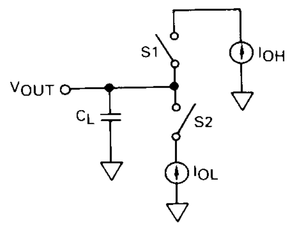


*Active when $\overline{RMWCYCLE}$ = 0

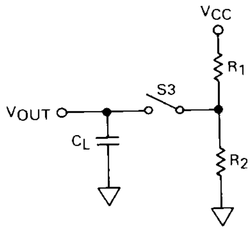
SWITCHING TEST CIRCUITS



A. RASI & $\overline{REFRESH}$ Outputs



B. $\overline{WE}$ Output



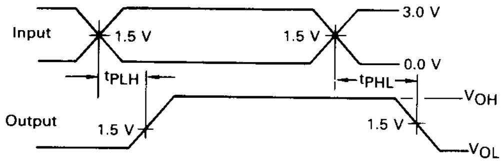
C. $\overline{DTACK}$ Output (Open Collector)

TEST OUTPUT LOADS

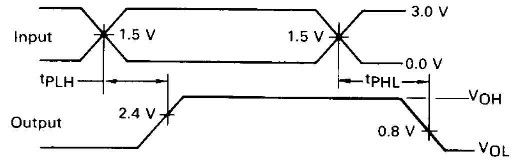
Test Circuit	R_1 (ohm)	R_2 (ohm)	C_L (pF)	I_{OH} (mA)	I_{OL} (mA)
A			50	−1.0	8.0
B			50, 150, 500	−1.0	12
C	680	1600	50		

Notes: 1. C_L, the load capacitance, includes scope, probe, wiring, and stray capacitance without the device in the test fixture.
2. S_1, S_2, and S_3 are open during all dc and functional testing.
3. During ac testing, switches are set as follows:
   1) S_3 is closed
   2) For $V_{OUT} > 1.5$ V, S_1 is closed and S_2 open
   3) For $V_{OUT} < 1.5$ V, S_1 is open and S_2 closed
4. $\overline{DTACK}$ Load:
   V_{CC} = 4.5, 5.0, and 5.5 V
   R_1 is selected to give I_{OL} (Max) with V_{CC} = 5.5 V
   R_2 is selected to give V_{OUT} (dc) = 0.7 V_{CC} when the output $\overline{DTACK}$ is off

SWITCHING TEST WAVEFORMS

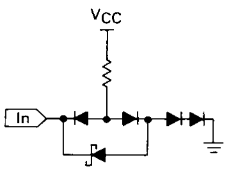


RASI, $\overline{\text{REFRESH}}$, and $\overline{\text{DTACK}}$ Outputs

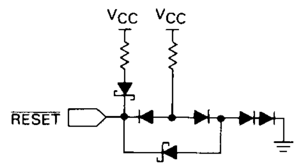


$\overline{\text{WE}}$ Output

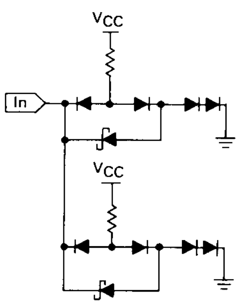
INPUT/OUTPUT CURRENT INTERFACE DIAGRAMS



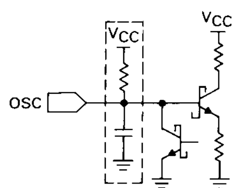
Typical Input



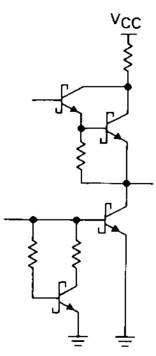
$\overline{\text{RESET}}$ Input



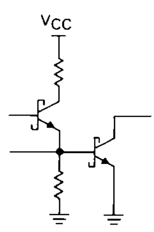
T_1, T_2, R/W, SUP, CS Inputs



OSC Input



Typical Output



$\overline{\text{DTACK}}$ Output