

SN74S262N ✓ ROW OUTPUT CHARACTER GENERATOR

features

- Static operation
- 5760 bit capacity
- 128 characters of 45 bits (5x9)
- 7 input character decoder
- 4 input row decoder
- Character format chosen to allow rounding on all characters
- High speed — 280ns character access time
- Lower power — 250mW
- Single + 5V supply
- 2 enable inputs for system expansion
- 20 pin DIL N-pack
- Compatible with most TTL and DTL logic circuits

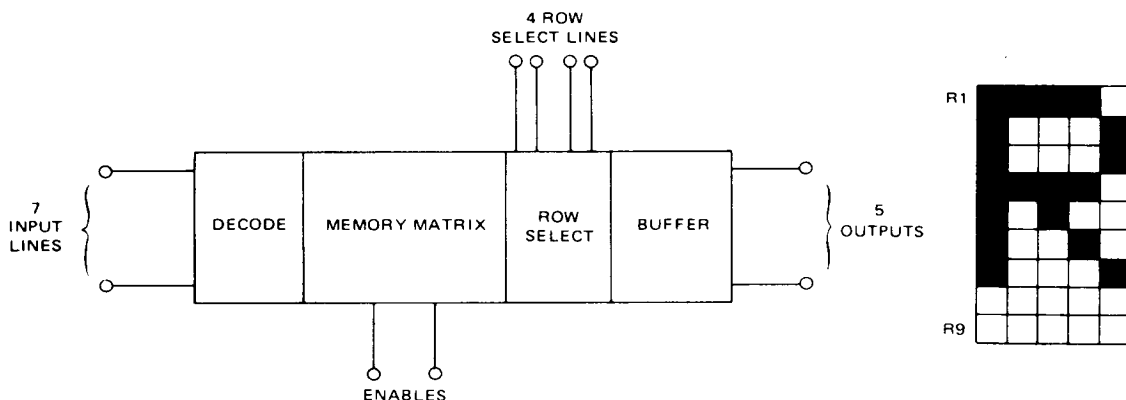
description

The SN74S262N Character Generator ROM is a fast, low power, dedicated IC developed by Texas Instruments Limited as part of the TIFAX Teletext decoder module, XM-11. The memory data is permanently stored by programming a single mask during manufacture, hence, other patterns can be provided.

The outputs are open collector, totempole or tri-state mask programmeable. The ROM is also mask programmable to inhibit outputs for invalid row addresses.

The SN74S262N specifically meets the needs of scanned video display systems. It can also be used in other ROM usages where it capacity, speed and low power features are of advantage.

functional diagram



operation

The SN74S262N series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip enable) remains unchanged.

Access time is defined as the time required for all outputs to reach the minimum level, or maximum 0 level, with the correct data. This time is measured from the point at which all address inputs and chip enable inputs are valid.

TEXAS INSTRUMENTS
LIMITED

SN74S262N CHARACTER GENERATOR

character scanning

The output character appears as a 9-word sequence on each of the 5 output lines. The sequence is controlled by the 4 row-select lines. The five outputs represent a row in a 5 x 9 character matrix. The row address can remain fixed while the character address changes (scanned display), or the character address may remain fixed while the row address changes (x - y or character scan).

ROW SELECT TRUTH TABLE

ROW SELECT				SELECTS ROW
R _d	R _c	R _b	R _a	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	
to				
1	1	1	1	

} Data Outputs Forced to Logical '0'

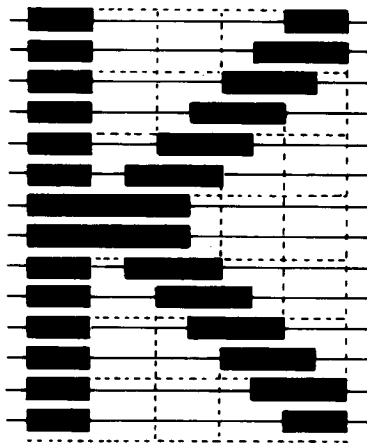
character rounding

In scanned display systems using line interlacing, economy of design requires a repetition of the displayed ROM pattern on alternate lines. This results in coarsely stepped diagonals which appear fainter than verticals or horizontals. A system which looks at the preceding or succeeding character row and interpolates intermediate extensions to the display, by reducing the coarseness of diagonals, makes the display visually more acceptable.

Methods requiring the reading of a character row and its preceding or succeeding row in one character display period, greatly reduce circuit complexity and component cost.

Teletext reception requires a 40 character display on a 625 line/50Hz system. This requires the ROM row access time to be better than about 400ns. The exact requirement is related to the speed and complexity of the associated logic.

Even with 80 characters/row, 625/525 line, 50/60Hz scanned VDU display systems, SN74S262N ROM is usable, especially since an improvement of its row access time specification is planned.



output buffers

The Teletext ROM, SN74S262N, has tri-state outputs.

SN74S262N ROM CHARACTER FORMAT

	1	1	1	1	0	0	0	0	3	2	1	0
	1	1	1	1	0	0	0	0	3	2	1	0
	1	1	1	1	0	0	0	0	3	2	1	0
									0	0	0	0
									1	0	0	0
									0	1	0	0
									1	1	0	0
									0	0	1	0
									1	0	1	0
									0	1	1	0
									1	1	1	0
									0	0	0	1
									1	0	0	1
									0	1	0	1
									1	1	0	1
									1	1	1	1

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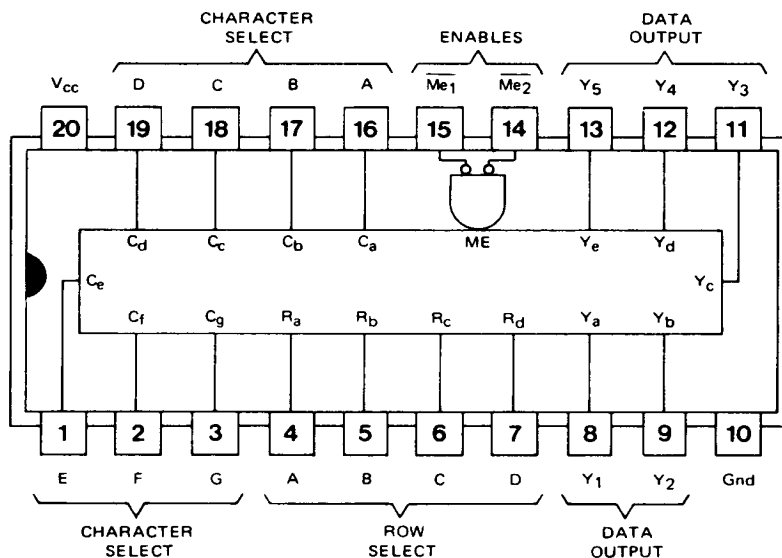
chip enable

Both chip enable inputs need to be at logic 0 to enable the SN74S262N. The facility of two chip enables provides for the selection of one out of four ROMs. The mask programmable option of open collector or tri-state outputs makes it possible to wire OR the outputs of several ROMs.

logic definition

Positive logic is assumed on the inputs.

An output blank is defined as a logic 0. An output dot is defined as a logic 1 output level.



absolute maximum ratings over operating free-air temperature

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
Operating free air temperature	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
High Level Output Current I_{OH}			-1	mA
Low Level 'Output' Current I_{OL}			4	mA
Operating Free Air Temperature (T_A)	0		70	$^{\circ}C$

electrical characteristics over recommended free air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH} High level input voltage		2			V
V_{IL} Low level input voltage				0.8	V
V_{OH} High level output voltage	$V_{IH} = 2V$ $I_{OH} = -0.2mA$ $V_{CC} = MIN$ $V_{IL} = 0.8V$	2.7	3.4		V
V_{OL} Low level output voltage	$V_{IH} = 2V$ $I_{OL} = 4mA$ $V_{CC} = MIN$ $V_{IL} = 0.8V$			0.5	V
I_{IH} High level input current	$V_{CC} = MAX$ $V_I = 2.7V$			20	μA
I_{IL} Low level input current	$V_{CC} = MAX$ $V_I = 0.4V$			-360	μA
Output leakage	$V_O = 2.7V$ $V_{IL} = 0.8V$ $V_{IH} = 2V$		20		μA
I_{CC} Supply current	$V_{CC} = 5.0V$		50		mA
Access time	Worst path		200	280	ns