Multistandard Programmable Analog CMOS Transmission IC

PCA1070

FEATURES

- Line interface with:
  - Voltage regulator with programmable DC voltage drop
  - Programmable set impedance
  - Output to control an external switching MOS transistor for pulse dialling
  - Programmable DC voltage during pulse dialling
  - Circuitry for short DC settling time
- Interface to peripheral circuits with:
  - Supply for microcontroller and DTMF diallers
  - Input to sense supply voltage of microcontroller and output for reset of microcontroller
  - I²C-bus (programming of parameters, control of all logic signals)
  - High impedance DTMF signal input
  - Input for external oscillator signal with on-chip DC blocking
  - Power-down via I²C-bus
  - Stabilized supply for electret microphone
- Microphone and DTMF amplifiers:
  - Low-noise microphone preamplifier suitable for various types of microphones
  - Symmetrical high impedance microphone preamplifier inputs
  - Programmable gain for microphone and DTMF channels
  - Sending mute via I²C-bus to disable microphone amplifier and enable DTMF amplifier
  - Sending mute also to be used as privacy switch
  - Dynamic limiting (speech controlled) to prevent distortion of line signal and sidetone; programmable maximum sending level
- Receive amplifier:
  - Suitable for various types of earpieces (including piezo)
  - Programmable gain and hearing protection level
  - Receive mute via I²C-bus to disable receive amplifier and enable DTMF confidence tone
  - On-chip anti-sidetone circuit with programmable sidetone balance
  - Confidence tone in the earpiece during DTMF dialling
- Facility to regulate parameters with line current:
  - Value of DC line current (bit code) readable via I²C-bus
  - Line loss compensation with fully software programmable characteristics (control range, stop current) of microphone/earpiece/DTMF amplifiers
  - Fully software programmable control of sidetone balance and DC voltage drop as a function of line length.

APPLICATIONS

- Wired telephony (basic till feature phones)
- Combi-terminals (e.g. telephone and answering machine or FAX)
- Modems and base units of cordless telephones.

GENERAL DESCRIPTION

The PCA1070 is a CMOS integrated circuit performing all speech and line interface functions in fully electronic telephone sets. The device requires a minimum of external components. The transmission parameters are programmable via the I²C-bus. This makes the IC adaptable to nearly all worldwide country requirements and to a various range of speech transducers, without changing the (few) external components.

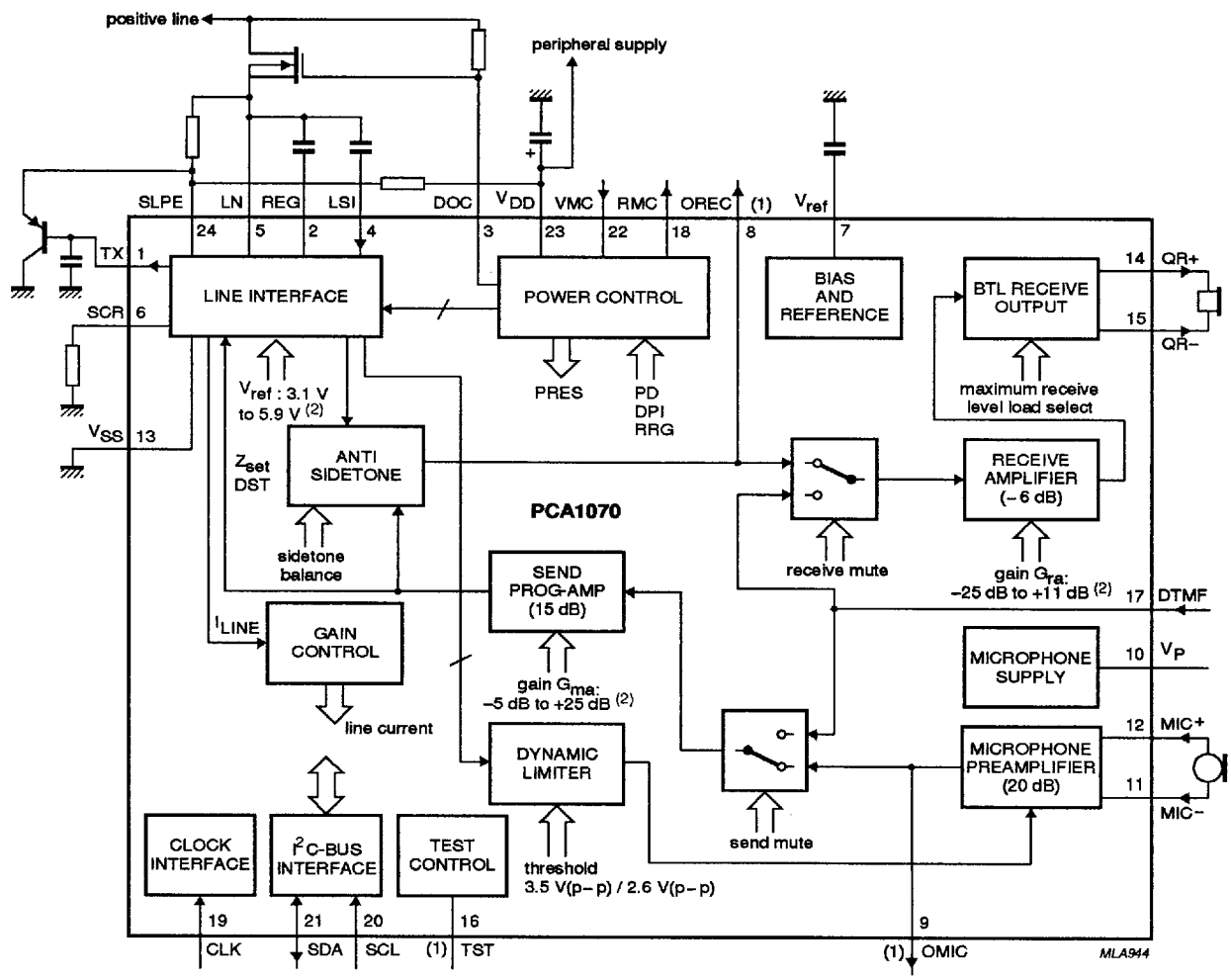
The parameters are stored in the EEPROM of a microcontroller and are loaded into the PCA1070 during the start-up phase of the transmission IC after hook-off.

The PCA1070 also allows adaptation to the connected telephone line by reading the line current via the I²C-bus and processing it in the microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA1070P	DIP24	plastic dual in-line package; 24 leads (600 mil)	SOT101
PCA1070T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137A

BLOCK DIAGRAM



(1) Test pins.
(2) Default value.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TX	1	drive output
REG	2	voltage regulator decoupling
DOC	3	dial output connection
LSI	4	line signal input
LN	5	positive line terminal
SCR	6	sending current resistor
V_{ref}	7	voltage reference decoupling
OREC	8	output receive preamplifier; to be left open-circuit in application
OMIC	9	output microphone preamplifier; to be left open-circuit in application
V_P	10	supply for electret microphones
MIC–	11	inverting input microphone preamplifier
MIC+	12	non-inverting input microphone preamplifier
V_{SS}	13	negative line terminal
QR+	14	non-inverting output for receiving output amplifier
QR–	15	inverting output for receiving output amplifier
TST	16	test pin; to be connected to V_{SS} in application
DTMF	17	dual tone multi-frequency input
RMC	18	reset output for microcontroller
CLK	19	clock signal input
SCL	20	serial clock line input; I^2C-bus
SDA	21	serial data line input/output; I^2C-bus
VMC	22	input to sense supply voltage microcontroller
V_{DD}	23	positive supply decoupling
SLPE	24	slope (DC resistance) adjustment

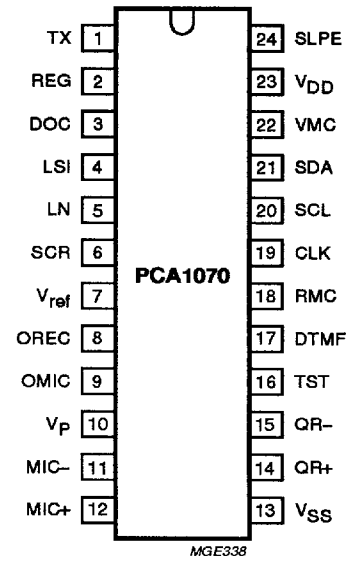


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Line interface

DC VOLTAGE DROP

Power for the PCA1070 and its peripheral circuits is obtained from the telephone line. The IC develops its own supply voltage at V_{DD} and regulates its DC voltage drop between pins SLPE and V_{SS}. The DC voltage V_{SLPE} can be programmed via the I²C-bus interface between 3.1 to 5.9 V and is default at 4.7 V (see Table 1).

The DC line voltage at pin LN can be calculated using the following equation:

$$V_{LN} = V_{SLPE} + (I_{line} - I_{LN}) \times R_{LN\text{-}SLPE}$$

where

I_{LN} = DC bias current flowing into pin LN (≈ 3 mA if I_{line} > 17 mA)

$R_{LN\text{-}SLPE}$ = external 20 Ω resistor between LN and SLPE.

At line currents below 6 mA (typ.) the DC voltage V_{SLPE} is automatically adjusted to a lower value. This means that the operation of more sets, connected in parallel, is possible with reduced sending and receiving levels and relaxed performance. At line currents below 16 mA (typ.) (17 mA max.) the DC bias current I_{LN} is reduced from ≈ 3 mA to a lower value to ensure maximum possible transmit level capability under all line current conditions.

SET IMPEDANCE

In normal conditions $I_{line} \geq I_{LN}$ and the static behaviour is equivalent to a voltage regulator diode with a series resistor $R_{LN\text{-}SLPE}$ (fixed value 20 Ω). In the audio frequency range the dynamic impedance Z_{LN} is determined mainly by internal components $Z_S = R_a + (R_b // C)$. The equivalent impedance Z_{LN} is shown in Fig.3. The values of R_a, R_b and C can be programmed via the I²C-bus interface (see Tables 9, 10 and 11).

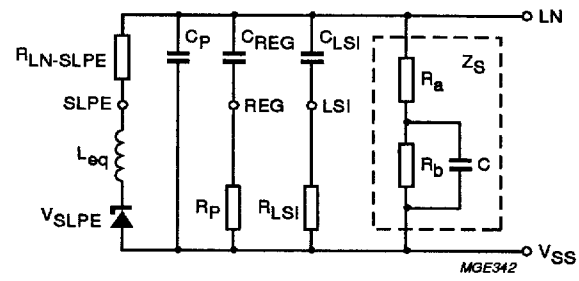


Fig.3 Equivalent impedance Z_{LN}.

Where:

R_P = internal resistor [1075 kΩ (typ.) with V_{SLPE} = 4.7 V]

R_{LSI} = internal resistor (240 kΩ typ.)

C_{REG} = capacitor at pin REG (470 nF)

$L_{eq} = R_P \times R_{LN\text{-}SLPE} \times C_{REG}$ = 10.1 H (typ.) with V_{SLPE} = 4.7 V (artificial inductor)

C_{LSI} = capacitor at pin LSI (100 nF)

C_P = internal capacitor (12 nF typ.).

SUPPLY FOR PERIPHERAL CIRCUITS

The supply voltage V_{DD} can be used for peripheral circuitry. The supply capabilities depend on the programmed DC voltage drop V_{SLPE} and on several other parameters as given in the following equation:

$$V_{DD} = V_{SLPE} - (I_{DD} + I_p + I_{VP}) \times R_{SLPE\text{-}VDD}$$

where

I_{DD} = internal current consumption PCA1070 (2.3 mA typ.)

I_p = current to peripheral circuitry

I_{VP} = current taken from V_P for electret microphone

$R_{SLPE\text{-}VDD}$ = external resistor between SLPE and V_{DD} (250 Ω).

DC STARTING AND SETTLING TIME

The IC is equipped with circuitry for fast DC start-up. This circuit is automatically activated as soon as V_{DD} reaches 3 V (typ.) after hook-off, and is deactivated when V_{SLPE} drops below 5.9 V (typ.). This ensures that only a relatively short time is needed to reach the default DC setting (V_{SLPE}) of the circuit and that V_{DD} will not exceed the maximum permitted voltage of 6 V.

The start-up circuit can also be activated under software control by setting bit code DST to logic 1 via the I²C-bus. The start-up time can be optimized by programming the bit code DST to logic 1 during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational. The DST bit can also be used to quickly restore the DC settings (V_{SLPE}) after long line breaks or during reprogramming of the DC voltage drop V_{SLPE}.

It should be noted that the AC impedance into pin LN is reduced considerably when DST = 1.

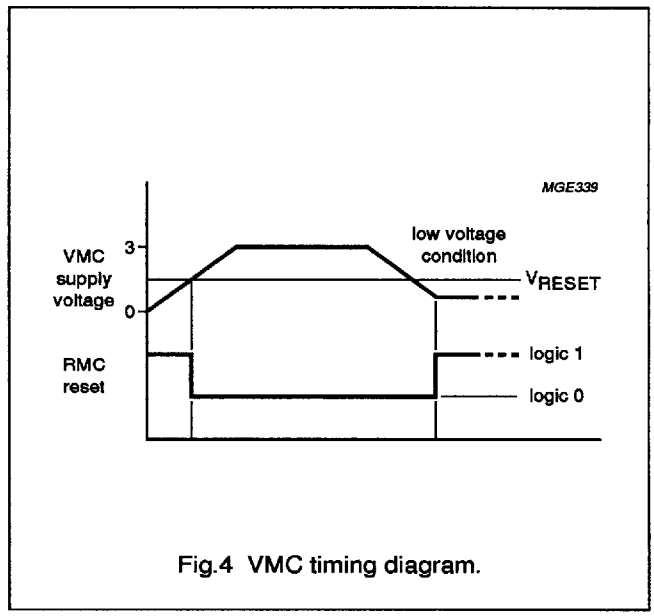


Fig.4 VMC timing diagram.

Power control

INTERNAL RESET PCA1070

The PCA1070 has an internal reset circuit that monitors the supply voltage V_{DD}. If V_{DD} is below the threshold level (V_{DD} = 1.2 V ±0.2 V) then the circuit is in reset-mode. In the reset mode the current consumption is low and the internal reset is active and writes the default values into all registers. The status bit PRES will also be set to logic 1. The microcontroller can read this bit via the I²C-bus interface; once read it will be set to logic 0 again.

When V_{DD} passes the threshold (increasing V_{DD}), the circuit becomes partly active and the internal ring/speech detector will be activated (see Section "Start-up and switch-off behaviour").

RESET OUTPUT FOR MICROCONTROLLER

The voltage at pin VMC (microcontroller supply voltage) is monitored by a reset circuit. If VMC is below the threshold level the output RMC is set to logic 1.

The threshold level in the normal operating mode and in the power-down mode is 2 V ±0.2 V (2.1 V ±0.3 V in standby mode).

POWER-DOWN/STANDBY MODES

The circuit can be set in power-down mode or in standby mode. These modes are intended for use with pulse dialling, during long line breaks, and applications with memory retention.

With control bits PDx = 01, the circuit is in the power-down mode; the current consumption at pin V_{DD} is reduced from I_{DD} = 2.3 mA (typ.) to <100 µA (typ.); the current consumption at pin VMC is 4 µA (typ.)(<10 µA). When PDx = 11 the circuit goes into the standby mode and I_{DD} = < 5 µA, I_{VMC} is reduced from 4 µA (typ.) to 2 µA (typ.)(< 5 µA). In both conditions (power-down and standby) the voltage stabilizer will be disabled.

START-UP AND SWITCH-OFF BEHAVIOUR

This description refers to the basic application where V_{DD} and VMC are connected together and one supply capacitor is used (see Fig.8).

Speech condition

After hook-off, line current will be applied to the line input LN. The supply capacitor connected to V_{DD} and VMC will be charged.

The internal reset signal will change from logic 1 to logic 0 when V_{DD} passes the threshold level (1.2 V ±0.2 V) and the circuit becomes partly active [the line interface part is kept in power-down mode, so that all of the line current is available to charge the supply capacitor(s)];

PCA1070 can receive data via the I²C-bus (standard I²C specifications are fulfilled for $V_{DD} \geq 2.5$ V; for V_{DD} = 1.8 to 2.5 V relaxed performance).

When VMC passes the microcontroller reset level 2 V ±0.2 V (2.1 V ±0.3 V in standby mode) the output RMC changes from logic 1 to logic 0 and the circuit is switched to the normal operating mode.

Hook-on

By decreasing VMC the output RMC will change from logic 0 to logic 1 when VMC passes the threshold level 2 V ±0.2 V (2.1 V ±0.3 V in standby mode), however the PCA1070 will stay in the normal operating mode until the internal reset takes place.

By decreasing V_{DD} the internal reset signal will change from logic 0 to logic 1 when V_{DD} passes the threshold (1.2 V ±0.2 V) and the circuit will go into the reset mode (line interface part in power-down and all programmable parameters are reset to default values).

Ringer condition

In this condition the supply capacitor connected to V_{DD} and VMC is charged by the ringer signal; no line current is applied to pin LN.

V_{DD} and VMC are increasing and when V_{DD} passes the internal reset threshold (1.2 V ±0.2 V), the internal ring/speech-detector will be activated and the circuit will switch to the standby condition (I_{DD} < 5 µA; I_{VMC} < 5 µA) before the voltage at VMC reaches the threshold level for microcontroller reset. When VMC passes this threshold level (2.1 V ±0.3 V) output RMC changes from logic 1 to logic 0 and the circuit will stay in the stand-by mode until line current is applied to pin LN. By setting the 'Reset RinG' control bit (RRG) to logic 1 via the I²C-bus interface, the ring/speech detector will be disabled.

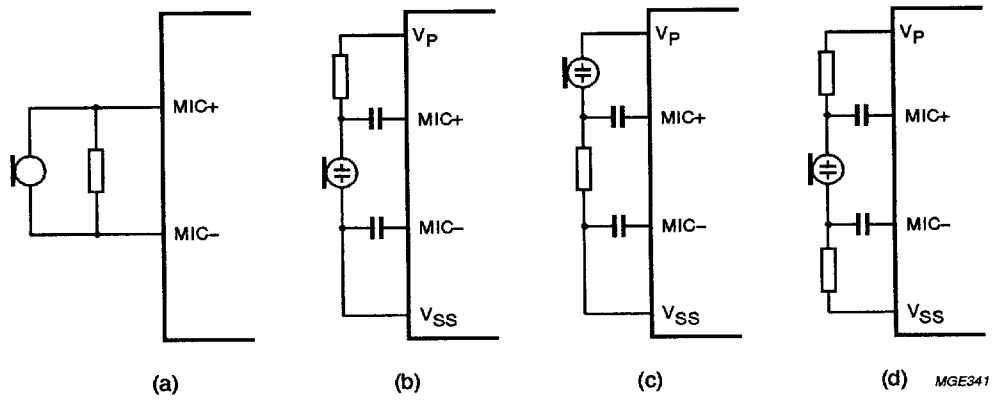
DIAL PULSE INPUT

The DPI bit controls output DOC (open-drain) that drives the gate of an external MOS interrupter transistor. DPI is controlled via the I²C-bus interface.

If DPI is set to logic 1, pin DOC will be pulled down to switch off the MOSFET to generate a line break. If DPI = 0 pin DOC is HIGH and the interrupter transistor will conduct the line current.

Microphone channel

The PCA1070 has symmetrical microphone inputs and accepts input signals of maximum 70 mV (peak) for THD = 2% ($V_{DD} \geq 2.5$ V). Its input impedance is 100 kΩ and its voltage gain is default 41 dB (typ.). Dynamic, magnetic, piezoelectric and electret (with built-in FET source follower) microphones can be used. Some possible microphone arrangements are shown in Fig.5.



(a) Dynamic or piezo.
(b) Low impedance electret with built-in pre-amplifier.
(c) High impedance electret with built-in pre-amplifier.
(d) Symmetrical connection of electret.

Fig.5 Microphone arrangements.

The gain of the microphone channel can be programmed between 30 dB and 51 dB in 1 dB steps using bit code GMAx (6 bits). The gain of the microphone preamplifier is fixed at 20 dB and GMAx sets the gain of the "send prog-amp" (allowed range G_{ma} = 4 to 25 dB, see Fig.1). The gain of the line interface is 6 dB.

The total gain of the microphone channel (G_M) is as follows:

$G_M = 20 + G_{ma} + 6$ (dB)

Default: $G_M = 20 + 15 + 6 = 41$ (dB)

where G_{ma} = Gain "send prog-amp"

Programming for the gain G_{ma} of the "send prog-amp" is given in Table 14.

Dynamic limiter

To prevent distortion of the transmitted speech signal, the gain of the microphone amplifier is reduced rapidly when signal peaks on the line exceed an internally determined threshold level. The time in which gain reduction is affected (attack time) is very short. The circuit stays in the gain-reduced condition until the peaks of the sending signal remain below the threshold level. The sending gain then returns to normal after a time determined on the chip (release time). The threshold level of the AC peak-to-peak line voltage on pin LN is default at 3.5 V (p-p). A lower level [2.6 V (p-p)] can be programmed by setting bit code DLT to logic 1.

The internal threshold is lowered automatically if the DC voltage setting of the circuit (V_{SLPE}) is not high enough to reach the programmed level. When the DC current in the transmit output stage is also insufficient to drive the line load, the internal threshold level is lowered automatically.

Dynamic limiting considerably improves sidetone performance in over-drive conditions (less distortion and limited sidetone level).

Program amplifier

A programmable amplifier called "prog-amp" is used both in the sending channel and in the receiving channel. The bit codes GMAx and GRAx are given in Tables 13 and 14 The permitted adjustment range differs for the two amplifiers. This is indicated in the corresponding sections.

DTMF channel

The PCA1070 has an asymmetrical DTMF input. Its input impedance is 200 kΩ//45 pF (typ.) and its voltage gain is default to 21 dB (typ.).

DTMF signals can be sent to the line by setting control bit SM (send mute) to logic 1 (default SM = 0); by setting the receive mute (RM) also to logic 1 (default RM = 0), the dialling tones are also sent to the receive output to generate a confidence tone in the earpiece.

The gain between the DTMF input and the line LN can be programmed between 1 dB and 21 dB in 1 dB steps using bit code GMAx (6 bits). The confidence tone gain (between DTMF input and earpiece outputs QR) can be programmed between –40 dB and –19 dB (symmetrical drive of earpiece) using bit code GRAx (6 bits). GMAx sets the gain of the "send prog-amp" (recommended range in DTMF mode for G_{ma} = –5 to 15 dB; see Fig.1) and GRAx sets the gain of the "rec prog-amp" (allowed range G_{ra} = –25 to 0 dB; see Fig.1).

The total gain of the DTMF channel between the DTMF input and the line LN is as follows:

$G_{DTMF} = G_{ma} + 6$ (dB]

Default $G_{DTMF} = 15 + 6 = 21$ (dB)

The confidence tone gain (DTMF to QR outputs) is:

With symmetrical drive of earpiece $G_{CTs} = G_{ra} - 19$ (dB)

Default $G_{CTs} = -6 - 19 = -25$ (dB)

At low gain settings ($G_{ra} < -10$ dB), the confidence tone gain will be slightly higher than the calculated value. This is caused by a residual signal.

Programming the gain of the "send prog-amp" and the "rec prog-amp" is given in Table 13.

Receive channel

The PCA1070 has an on-chip anti-sidetone circuit. The gain of the receive channel is defined between the line connection LN and the earpiece outputs QR+ and QR–. Its voltage gain is default to –6 dB (typ.) (differential drive). The LN terminal accepts receive signals up to 1 V (RMS) (typ.) for THD = 2%. The outputs may be used to connect dynamic, magnetic or piezoelectric earpieces with single-ended or differential drive. The load select bit RFC is default to logic 1 to guarantee stable operation in the event of a capacitive load (piezoelectric earpiece). With a resistive load (dynamic capsule) RFC should be set to logic 0 via the I^2C-bus interface to obtain optimum performance with respect to distortion and bandwidth. Two levels for hearing protection can be selected via the I^2C-bus interface with control bit HPL.

The earpiece arrangements are illustrated in Fig.6.

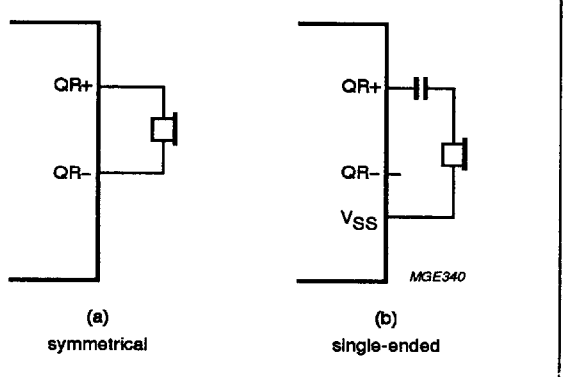


Fig.6 Earpiece arrangements.

The gain of the receive channel can be programmed between −19 dB and +11 dB (symmetrical drive) in 1 dB steps using bit code GRAx (6 bits).

GRAx sets the gain of the "rec prog-amp" (allowed range G_{ra} = −19 dB to +11 dB; default G_{ra} = −6 dB).

The total gain of the receiving channel is as follows:

Symmetrical drive $G_{rs} = G_{ra}$ (dB)

Default G_{rs} = −6 (dB)

Asymmetrical or single-ended drive $G_{ra} = G_{ra} - 6$ (dB)

Default G_{ra} = −6 − 6 (dB) = −12 (dB)

Programming the gain G_{ra} of the "rec prog-amp" is given in Table 13.

Sidetone balance

The PCA1070 has an on-chip anti-sidetone circuit. An internal balance impedance Z_{oss} can be programmed via the I²C-bus interface to match the external line impedance Z_{line} to give optimum sidetone suppression.

$$Z_{oss} = R_{sa} + (R_s // C_s);\ f_{ps} = \frac{1}{(2\pi \times R_s \times C_s)}.$$

Programming for the sidetone balance is given in Tables 15, 16 and 17.

Line current control

The DC line current can be read via the I²C-bus interface. This gives information about the line current and can be used to change several parameters with line current (for example line loss compensation, sidetone balance and DC characteristics).

The bit code LCx as a function of line current is given in Table 18.

I²C-BUS PROGRAMMING

Table 1 Programmable parameters

The following parameters (see Fig.1) can be programmed by means of a bit code via the I²C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
VDCx	V_{ref}	line interface	3	DC voltage SLPE-V_{SS}
ZSAx	Z_{set}	line interface	3	AC set impedance R_a
ZSBx	Z_{set}	line interface	3	AC set impedance R_b
ZSPx	Z_{set}	line interface	4	AC set impedance f_p (pole frequency)
DST	DST	line interface	1	DC Start Time
PDx	PD	power control	2	Power-Down
DPI	DPI	power control	1	Dial Pulse Input
RRG	RRG	power control	1	Reset RinG detector
HPL	maximum receive level	BTL receive output	1	Hearing Protection Level
RFC	load select	BTL receive output	1	Resistive/Capacitive load
ZOSAx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone R_{sa}
ZOSBx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone R_{sb}
ZOSPx	sidetone balance	anti-sidetone	4	Z Optimum Sidetone C_s
RM	receive mute	receive mute	1	Receive Mute
GRAx	gain G_{ra}	receive prog-amp	6	Gain Receive prog-amp
GMAx	gain G_{ma}	send prog-amp	6	Gain send prog-amp
SM	send mute	send mute	1	Send Mute
DLT	threshold	dynamic limiter	1	Dynamic Limiter Threshold

Table 2 Readable parameters

The following parameters (see also Fig.1) can be read as a bit code via the I²C-bus:

SYMBOL	PARAMETER	BLOCK	BITS	DESCRIPTION
PRES	PRES	power control	1	PCA1070 Reset
LCx	line current	gain control	5	Line Current

I²C interface

The I²C-bus interface (see *"The I²C-bus and how to use it"* 12NC: 9398 393 40011) is used to program the transmission parameters and control functions.

Table 3 Device address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
0	1	0	0	0	1	0	X

All functions can be accessed by writing an 8-bit word to the PCA1070. In order to set up the PCA1070, a control message consisting of the device address, a R/$\overline{W}$ bit, a subaddress byte and one or more data bytes must be written to the PCA1070. If more than one data byte follows the subaddress, these bytes are stored in the successive registers by the automatic increment feature.

Table 4 The control word format for the slave receiver

	DEVICE ADDRESS									SUB ADDRESS									DATA/CONTROL BYTE									
S	0	1	0	0	0	1	0	0[1]	A	I7	I6	I5	I4	I3	I2	I1	I0	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. This bit is R/$\overline{W}$.

Table 5 Bit arrangement of each data byte used in the control word: PCA1070 receiver (see note 1)

FUNCTION	SUB ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
DC voltage	H00		VDC2	VDC1	VDC0				DST
Sidetone and set impedance	H01	ZOSB3	ZOSB2	ZOSB1	ZOSB0	ZOSA3	ZOSA2	ZOSA1	ZOSA0
	H02	ZOSP3	ZOSP2	ZOSP1	ZOSP0		ZSA2	ZSA1	ZSA0
	H03		ZSB2	ZSB1	ZSB0	ZSP3	ZSP2	ZSP1	ZSP0
Send channel	H04	DLT		GMA5	GMA4	GMA3	GMA2	GMA1	GMA0
Receive channel	H05	RFC	HPL	GRA5	GRA4	GRA3	GRA2	GRA1	GRA0
Control	H06	PD1	PD0		RRG	RM	SM		DPI

Note

1. The bits that are not indicated must be set to logic 0.

Table 6 The control word format for the slave transmitter

	DEVICE ADDRESS									DATA/STATUS BYTE									
S	0	1	0	0	0	1	0	1[1]	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P

Note

1. Change in direction of R/$\overline{W}$ bit.

Table 7 PCA1070 send bits

FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
PCA1070 status	PRES[1]	–	–	LC4[2]	LC3[2]	LC2[2]	LC1[2]	LC0[2]

Notes

1. Indicates if PCA1070 has received internal reset; PRES will be set to logic 1 with internal reset and is set to logic 0 after reading the register via the I²C-bus.
2. Information about value of line current.

WRITE AND READ TABLES

DC voltages

Table 8 DC voltage at pin SLPE

VDC2	VDC1	VDC0	V_{SLPE}	REMARK
0	0	0	3.1	
0	0	1	3.5	
0	1	0	3.9	
0	1	1	4.3	
1	**0**	**0**	**4.7**	**default**
1	0	1	5.1	
1	1	0	5.5	
1	1	1	5.9	

Set impedance

Programming the impedance in the audio frequency range seen at pin LN: $R_a + (R_b//C)$ where the pole frequency

$$f_p = \left(\frac{1}{(2\pi \times R_b \times C)}\right)$$

Table 9 Programming R_a

ZSA2	ZSA1	ZSA0	R_a (Ω)	REMARK
0	0	0	0	
0	0	1	100	
0	**1**	**0**	**200**	**default**
0	1	1	300	
1	0	0	400	
1	0	1	500	note 1
1	1	X	600	notes 1 and 2

Notes

1. For Z_s combinations where $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions.
2. X = don't care.

Table 10 Programming R_b

ZSB2	ZSB1	ZSB0	R_b (Ω)	REMARK
0	0	0	0	note 1
0	0	1	600	
0	1	0	700	
0	**1**	**1**	**800**	**default**
1	X	0	900	note 2
1	X	1	1000	note 2

Notes

1. For Z_s combinations where $R_a \geq 500\ \Omega$ it is obligatory that $R_b = 0$. This is to safeguard stable operation of the line interface under all practical conditions.
2. X = don't care.

Table 11 Programming pole frequency:

ZSP3	ZSP2	ZSP1	ZSP0	f_p (Hz)	C (nF)					REMARK
					R_b = 600 (Ω)	R_b = 700 (Ω)	R_b = 800 (Ω)	R_b = 900 (Ω)	R_b = 1000 (Ω)	
0	0	0	0	828	320	275	240	214	192	
0	0	0	1	1095	242	207	182	161	145	
0	0	1	0	1448	183	157	137	122	110	
0	**0**	**1**	**1**	**1915**	**139**	**119**	**104**	**92**	**83**	**default**
0	1	0	0	2533	105	90	79	70	63	
0	1	0	1	3350	79	68	59	53	48	
0	1	1	0	4430	60	51	45	40	36	
0	1	1	1	5859	45	39	34	30	27	
1	X	X	X	12000	22	19	17	15	13	note 1

Note

1. X = don't care.

Reset functions

Monitoring of internal reset PCA1070.

Table 12 Status bit PRES

PRES	DESCRIPTION
1	internal reset has occurred; default values in all registers
0	register has been read via the I^2C-bus interface

Programmable amplifier (prog-amp)

A programmable amplifier called "prog-amp" is used both in the sending channel and in the receiving channel. The bit codes GMAx and GRAx are given in Tables 13 and 14. The permitted adjustment range differs for the two amplifiers and is different for the DTMF mode and the speech mode. This is indicated in the corresponding sections.

Table 13 Bit code of rec prog-amp

GAIN (dB)	INPUT CODE					
	MSB					LSB
−25	1	1	1	0	0	1
−24	1	1	1	0	0	0
−23	1	1	0	1	1	1
−22	1	1	0	1	1	0
−21	1	1	0	1	0	1
−20	1	1	0	1	0	0
−19	1	1	0	0	1	1
−18	1	1	0	0	1	0
−17	1	1	0	0	0	1
−16	1	1	0	0	0	0
−15	1	0	1	1	1	1
−14	1	0	1	1	1	0
−13	1	0	1	1	0	1
−12	1	0	1	1	0	0
−11	1	0	1	0	1	1
−10	1	0	1	0	1	0
−9	1	0	1	0	0	1
−8	1	0	1	0	0	0
−7	1	0	0	1	1	1
−6[1]	**1**	**0**	**0**	**1**	**1**	**0**
−5	1	0	0	1	0	1
−4	1	0	0	1	0	0
−3	1	0	0	0	1	1
−2	1	0	0	0	1	0
−1	1	0	0	0	0	1
−0	1	0	0	0	0	0

Notes

1. Default value "rec prog-amp" GRAx.

Table 14 Bit code of send prog-amp

GAIN (dB)	INPUT CODE					
	MSB					LSB
+25	0	1	1	0	0	1
+24	0	1	1	0	0	0
+23	0	1	0	1	1	1
+22	0	1	0	1	1	0
+21	0	1	0	1	0	1
+20	0	1	0	1	0	0
+19	0	1	0	0	1	1
+18	0	1	0	0	1	0
+17	0	1	0	0	0	1
+16	0	1	0	0	0	0
+15[1]	**0**	**0**	**1**	**1**	**1**	**1**
+14	0	0	1	1	1	0
+13	0	0	1	1	0	1
+12	0	0	1	1	0	0
+11	0	0	1	0	1	1
+10	0	0	1	0	1	0
+9	0	0	1	0	0	1
+8	0	0	1	0	0	0
+7	0	0	0	1	1	1
+6	0	0	0	1	1	0
+5	0	0	0	1	0	1
+4	0	0	0	1	0	0
+3	0	0	0	0	1	1
+2	0	0	0	0	1	0
+1	0	0	0	0	0	1
+0	0	0	0	0	0	0

Notes

1. Default value "send prog-amp" GMAx.

Sidetone balance

Internal balance impedance Z_{oss} to match the external line impedance Z_{line} to give optimum sidetone suppression.

$$Z_{oss} = R_{sa} + (R_{sb}//C_s);\ f_{ps} = \frac{1}{(2\pi \times R_{sb} \times C_s)}$$

Table 15 Programming R_{sa}

ZOSA				R_{sa} (Ω)
MSB			LSB	
0	0	0	0	134
0	0	0	1	153
0	0	1	0	193
0	0	1	1	221
0	1	0	0	246
0	1	0	1	277
0	1	1	0	295
0	1	1	1	341
1	0	0	0	369
1	0	0	1	443
1	**0**	**1**	**0**	**492**(1)
1	0	1	1	–
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. default value.

Table 16 Programming R_{sb}

ZOSB				R_{sb} (Ω)
MSB			LSB	
0	0	0	0	465
0	0	0	1	637
0	0	1	0	710
0	0	1	1	803
0	1	0	0	893
0	1	0	1	1003
0	**1**	**1**	**0**	**1259**(1)
0	1	1	1	1410
1	0	0	0	1572
1	0	0	1	1773
1	0	1	0	1978
1	0	1	1	2216
1	1	0	0	–
1	1	0	1	–
1	1	1	0	–
1	1	1	1	–

Note

1. default value.

Table 17 Programming C_s

ZOSP				C_s (nf)
MSB			LSB	
0	0	0	0	5
0	0	0	1	55
0	0	1	0	58
0	0	1	1	69
0	1	0	0	76
0	1	0	1	85
0	1	1	0	96
0	1	1	1	105
1	0	0	0	121
1	**0**	**0**	**1**	**134**(1)
1	0	1	0	145
1	0	1	1	166
1	1	0	0	186
1	1	0	1	207
1	1	1	0	232
1	1	1	1	259

Note

1. default value.

The optimum setting of R_{sa} depends on the value of the set impedance. To safeguard stable operation of the anti-sidetone circuit under all practical conditions, the following condition must be fulfilled: $R_{sa} \geq 0.5R_a$.

Line current control

Table 18 Bit code LCx and DC line current

BIT CODE LCx					I_{line} (typ.) (mA)
LC4	LC3	LC2	LC1	LC0	
0	0	0	0	0	<12.5
0	0	0	0	1	15.0
0	0	0	1	0	17.5
0	0	0	1	1	20.0
0	0	1	0	0	22.5
0	0	1	0	1	25.0
0	0	1	1	0	27.5
0	0	1	1	1	30.0
0	1	0	0	0	32.5
0	1	0	0	1	35.0
0	1	0	1	0	37.5
0	1	0	1	1	40.0
0	1	1	0	0	42.5
0	1	1	0	1	45.0
0	1	1	1	0	47.5
0	1	1	1	1	50.0
1	0	0	0	0	52.5
1	0	0	0	1	55.0
1	0	0	1	0	58.0
1	0	0	1	1	61.0
1	0	1	0	0	64.0
1	0	1	0	1	66.5
1	0	1	1	0	69.0
1	0	1	1	1	71.5
1	1	0	0	0	74.0
1	1	0	0	1	77.5
1	1	0	1	0	80.0
1	1	0	1	1	82.5
1	1	1	0	0	85.0
1	1	1	0	1	88.0
1	1	1	1	0	91.0
1	1	1	1	1	>94.0

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{LN}	positive line voltage at pin LN	−0.8	12	V
V_i	input voltage on pins SLPE, DOC, REG, TX and LSI	−0.8	12	V
V_{DD}	supply voltage	−0.8	+7.0	V
V_n	voltage on all other pins	−0.8	+7.0	V
I_i	input current	−	±10	mA
P_{tot}	total power dissipation	−	250	mW
T_{stg}	storage temperature	−40	+125	°C
T_{amb}	operating ambient temperature	−10	+60	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		K/W

CHARACTERISTICS

I_{line} = 20 mA; V_{SS} = 0 V; f = 1000 Hz; I_p = 0 mA; I_{VP} = 0 mA; f_{clk} = 3.579545 MHz; T_{amb} = 25 °C; all programmable parameters at default values; control bits set at default: DST = 0; DLT = 0; PDx = 00; RRG = 0; HPL = 0; RM = 0; SM = 0; DPI = 0; control bit not set at default: RFC = 0; AC load impedance at pin LN is Z_{line} = 220 Ω + (820 Ω//115 nF); load impedance at earpiece output R_t = 150 Ω; source impedance at microphone input R_m = 150 Ω; measured in test circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC line interface: LN, TX, SLPE and REG						
I_{line}	line current operating range	normal operation	17	–	140	mA
		reduced sending level	12	–	17	mA
V_{SLPE}	reference DC voltage at SLPE, DST = 0 with or without clock	VDCx = 100 default	4.3	4.7	5.1	V
$V_{SLPE(min)}$	minimum selectable value	VDCx = 000; note 1	2.8	3.1	3.4	V
$V_{SLPE(max)}$	maximum selectable value	VDCx = 111; note 1	5.4	5.9	6.4	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
V_{SLPE}	reference DC voltage at SLPE, DST = 1 with or without clock	VDCx = 100 default	–	4.7	–	V
$V_{SLPE(min)}$	minimum selectable value	VDCx = 000; note 1	–	3.1	–	V
$V_{SLPE(max)}$	maximum selectable value	VDCx = 111; note 1	–	5.9	–	V
$V_{SLPE(step)}$	step resolution		–	0.4	–	V
ΔV_{SLPE}	reference DC voltage at SLPE variation with temperature	at −10°C and +60 °C with respect to T_{amb} = 25 °C; DST = 0	–	±20	–	mV
V_{LN}	DC line voltage at LN (slope = 20 Ω); with or without clock at default	VDCx = 100; DST = 0; I_{line} = 12 mA	–	4.83	–	V
		VDCx = 100; DST = 0; I_{line} = 20 mA	4.6	5.0	5.4	V
		VDCx = 100; DST = 0; I_{line} = 120 mA	6.5	7.0	7.5	V
V_{LN}	DC line voltage at LN at low line current with or without clock	DST = 0; I_{line} = 0.25 mA	–	1	–	V
		DST = 0; I_{line} = 2 mA	–	1.9	–	V
		DST = 0; I_{line} = 4 mA	–	3.4	–	V
		DST = 0; I_{line} = 7 mA	–	4.73	5.2	V
t_{DC}	DC start-up time	C_{VDD} = 470 µF; I_{line} = 20 mA; (no clock; V_{clk} = 0); note 2	–	145	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TX: DRIVE OUTPUT (EXTERNAL pnp)						
V_{TX}	output drive voltage with TX disconnected from external pnp	V_{SLPE} = 2 V; V_{REG} = 1.5 V; V_{DD} = VMC = 2.5 V; I_{TX} = 0 mA	–	1.45	–	V
		V_{SLPE} = 3 V; V_{REG} = 2.5 V; V_{DD} = VMC = 2.5 V; I_{TX} = 1.6 mA	–	2.2	–	V
t_{SW}	switching time DC voltage at SLPE	V_{SLPE} = 5.9 V to 3.1 V; DST = 0; note 3	–	65	–	ms
		V_{SLPE} = 3.1 V to 5.9 V; DST = 0; note 3	–	65	–	ms
		V_{SLPE} = 5.9 V to 3.1 V; DST = 1; note 3	–	1	–	ms
		V_{SLPE} = 3.1 V to 5.9 V; DST = 1; note 3	–	0.5	–	ms
Supplies: V_{DD}, VMC, V_P and SLPE						
V_{DD}	operating supply voltage	normal operation; note 4	2.5	–	6	V
		relaxed performance; note 5	1.8	–	2.5	V
V_{DD}; SUPPLY PIN						
I_{DD}	current consumption	PDx = 00 default; V_{DD} = 2.5 V; normal operation	–	2.3	–	mA
$I_{DD(int)}$	internal current in power-down or standby mode; I²C-bus in idle mode	power-down; PDx = 01; SCL = 1; SDA = 1	–	30	100	µA
		standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	µA
V_{DD}: PERIPHERAL SUPPLY						
I_p	current available for peripheral circuitry	V_{DD} = 2.9 V; SM = 1; RM = 1; V_{SLPE} = 4.7 V (default); $R_{SLPE-VDD}$ = 250 Ω external	–	4.9	–	mA
		V_{DD} = 2.5 V; SM = 1; RM = 1; V_{SLPE} = 4.7 V (default); $R_{SLPE-VDD}$ = 250 Ω external	–	6.5	–	mA
VMC; SENSE INPUT MICROCONTROLLER SUPPLY VOLTAGE						
I_{VMC}	input current	VMC = 2.5 V in normal operation; PDx = 00 default	–	4	10	µA
I_{VMC}	input current in power-down or standby mode; I²C-bus in idle mode	VMC = 2.5 V in power-down; PDx = 01; SCL = 1; SDA = 1	–	4	10	µA
		VMC = 2.5 V in standby; PDx = 11; SCL = 1; SDA = 1	–	2	5	µA
V_P; SUPPLY OUTPUT FOR ELECTRET MICROPHONE						
V_P	voltage available	I_{VP} = 500 µA	1.6	1.9	–	V
Z_o	output impedance	f = 300 Hz	–	40	–	Ω
PSR	power supply rejection	f = 300 Hz; note 6	–	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset functions: V_{DD}, VMC and RMC						
INTERNAL RESET PCA1070: note 7						
$V_{DD(SW)}$	switching level of V_{DD} below which internal reset is active	T_{amb} = −10 to +60 °C	1.0	1.2	1.4	V
RMC: RESET OUTPUT FOR MICROCONTROLLER						
$V_{VMC(SW)}$	voltage switching level at pin VMC where RMC changes state	normal operation; PDx = 00; T_{amb} = 25 °C; note 8	1.8	2.0	2.2	V
		power-down; PDx = 01; T_{amb} = 25 °C; note 8	1.8	2.0	2.2	V
		standby; PDx = 11; T_{amb} = 25 °C; note 8	1.8	2.1	2.4	V
$\Delta V_{VMC}/T$	sense voltage variation with temperature	normal operation; PDx = 00; T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		power-down; PDx = 01; T_{amb} = −10 to +60 °C	–	0	–	mV/°C
		standby; PDx = 11; T_{amb} = −10 to +60 °C	–	3	–	mV/°C
Sending channel: MIC+, MIC−, DTMF, OMIC, LN, SCR, REG and LSI						
MIC+, MIC−: MICROPHONE INPUTS						
Z_i	input impedance	differential	60	100	–	kΩ
		single-ended	30	50	–	kΩ
CMRR	common mode rejection ratio	f = 1000 Hz; note 9	–	72	–	dB
$V_{i(peak)}$	allowed input signal voltage level (peak value)		–	–	70	mV
$G_{v(MIC)}$	voltage gain MIC+/MIC− to LN	GMAx = 001111 default	39.5	41	42.5	dB
$G_{v(min)}$	minimum selectable voltage gain	GMAx = 000100; note 1	28.5	30	31.5	dB
$G_{v(max)}$	maximum selectable voltage gain	GMAx = 011001; note 1	49.5	51	52.5	dB
G_{step}	step resolution		–	1	–	dB
ΔG_v	frequency response	gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	+0.3/−0.7	dB
ΔG_v	voltage gain variation with temperature	at −10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	at 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
t_{AC}	AC start-up time (with clock V_{clk})	C_{VDD} = 470 µF; I_{line} = 20 mA; note 11	–	150	–	ms
Send mute/privacy switch						
ΔG_v	voltage gain reduction from MIC+/MIC− to LN	SM = 1; note 1	–	100	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF: dual tone multi-frequency input						
Z_{IRp}	input impedance $R_p//C_p$	single-ended	100	200	–	kΩ
Z_{ICp}	input impedance $R_p//C_p$	single-ended	–	45	–	pF
$G_{v(LN)}$	voltage gain from DTMF to LN	SM = 1 default; GMAx = 001111	20	21	22	dB
$G_{v(min)}$	minimum selectable voltage gain	SM = 1 default; GMAx = 100101; note 1	0	1	2	dB
$G_{v(max)}$	maximum selectable voltage gain	SM = 1 default; GMAx = 001111; note 1	20	21	22	dB
G_{step}	step resolution		–	1	–	dB
ΔG_v	frequency response	SM = 1; gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	+0.3/–0.7	dB
ΔG_v	voltage gain variation with temperature	SM = 1; at –10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	SM = 1; at 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
Confidence tone; note 12						
$G_{v(QR)}$	voltage gain from DTMF to QR+ or QR–	GRAx = 100110 default; SM = 1; RM = 1; differential load RT = 150 Ω	–	–25	–	dB
$G_{v(min)}$	minimum selectable voltage gain	GRAx = 111001; SM = 1; RM = 1; differential load RT = 150 Ω; note 1	–	–40	–	dB
$G_{v(max)}$	maximum selectable voltage gain	GRAx = 100000; SM = 1; RM = 1; differential load RT = 150 Ω; note 1	–	–19	–	dB
G_{step}	step resolution		–	0.5 to 1	–	dB
LN: sending channel output						
Z_{LN}	impedance between LN and V_{SS}; $f_p = 1/(2\pi \times R_b \times C)$ $Z_{LN} \approx Z_s = R_a + (R_b//C)$;	ZSAx = 010 default; no Z_{line}; notes 13 and 14	–	200	–	Ω
		ZSBx = 011 default; no Z_{line}; notes 13 and 14	–	800	–	Ω
		ZSPx = 0011 default; no Z_{line}; notes 13 and 14	–	1915	–	Hz
BRL	balance return loss Z_{LN} with respect to Z_{ref}; Z_{ref} = 220 Ω + (820 Ω//115 nF)	Z_s = default; f = 300 Hz; note 15	20	37	–	dB
		Z_s = default; f = 1 kHz; note 15	20	35	–	dB
		Z_s = default; f = 3.4 kHz; note 15	20	27	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SELECTABLE VALUES FOR Z_S; note 1						
$R_{a(min)}$	minimum selectable value for R_a	R_b = 0; f_p = 12 kHz; ZSAx = (001); note 16	–	100	–	Ω
$R_{a(max)}$	maximum selectable value for R_a	R_b = 0; f_p = 12 kHz; ZSAx = (11x); note 16	–	600	–	Ω
$R_{a(step)}$	step resolution for R_a		–	100	–	Ω
$R_{b(min)}$	minimum selectable value for R_b	R_a = 0; f_p = 12 kHz; ZSBx = (001); note 16	–	600	–	Ω
$R_{b(max)}$	maximum selectable value for R_b	R_a = 0; f_p = 12 kHz; ZSBx = (1x1); note 16	–	1000	–	Ω
$R_{b(step)}$	step resolution for R_b		–	100	–	Ω
$f_{p(min)}$	minimum selectable pole frequency	R_a = 0; R_b = 1 kΩ; ZSPx = (0000); note 17	–	828	–	Hz
$f_{p(max)}$	maximum selectable pole frequency	R_a = 0; R_b = 1 kΩ; ZSPx = (0111); note 17	–	5859	–	Hz
n	multiplication factor for pole frequency	$f_p(x + 1) = n \times [f_p(x)]$	–	1.322	–	
$V_{no(rms)}$	noise output voltage (RMS value)	150 Ω between MIC+ and MIC-; psophometrically weighted (O41 curve)	–	−76	–	dBmp
Dynamic limiter; note 1						
$V_{LN(p-p)}$	voltage threshold level at which dynamic limiter reduces send gain (peak-to-peak value)	V_{SLPE} = default (4.7 V ±0.4 V); DLT = 0 default	3.1	3.5	3.9	V
		V_{SLPE} = default (4.7 V ±0.4 V); DLT = 1 default	2.2	2.6	3.0	V
THD	total harmonic distortion	V_i = 12 mV (RMS) + 10 dB	–	2.5	5.0	%
Dynamic behaviour of limiter; note 18						
t_{att}	attack time	V_i jumps from 12 to 38 mV (RMS)	–	1.5	–	ms
t_{rel}	release time	V_i jumps from 38 to 12 mV (RMS)	–	90	–	ms
$V_{LN(p-p)}$	voltage threshold level at which dynamic limiter reduces send gain	low voltage conditions; DLT = 0; V_{SLPE} = 3.1 V; I_{line} = 20 mA	–	2.4	–	V
		low current conditions; DLT = 0; V_{SLPE} = 4.7 V; I_{line} = 9 mA	–	2.6	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCR: pin for sending current resistor						
V_{SCR}	voltage at pin SCR	I_{line} = 20 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.28	–	V
		I_{line} = 20 mA; GMAx = 000100; G_M = 30 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.26	–	V
		I_{line} = 12 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.22	–	V
		I_{line} = 7 mA; GMAx = 001111; G_M = 41 dB; $R_{SCR-VSS}$ = 100 Ω	–	0.13	–	V
Receive channel: LN, LSI, OREC, QR+ and QR–						
QR+, QR–: RECEIVING AMPLIFIER OUTPUTS						
Z_o	output impedance	single-ended	–	4	–	Ω
$G_{v(rec)}$	voltage gain from LN to QR	RFC = 0 default; R_t = 150 Ω; GRAx = 100110; single-ended	–13.5	–12	–10.5	dB
		RFC = 0 default; R_t = 150 Ω; GRAx = 100110; differential	–7.5	–6	–4.5	dB
$G_{v(min)}$	minimum selectable voltage gain	GRAx = 110011; R_t = 150 Ω; single-ended	–26.5	–25	–23.5	dB
		GRAx = 110011; R_t = 150 Ω; differential	–20.5	–19	–17.5	dB
$G_{v(max)}$	maximum selectable voltage gain	GRAx = 001011; R_t = 150 Ω; single-ended	3.5	5.0	6.5	dB
		GRAx = 001011; R_t = 150 Ω; differential	9.5	11.0	12.5	dB
$G_{v(step)}$	voltage gain step resolution		–	1	–	dB
ΔG_v	frequency response	R_t = 150 W; RFC = 0; gain variation at f = 300 Hz and 3400 Hz with respect to 1 kHz; note 10	–	–	±0.5	dB
ΔG_v	voltage gain variation with temperature	R_t = 150 Ω; RFC = 0 at –10 to +60 °C with respect to T_{amb} = 25 °C	–	±0.2	–	dB
ΔG_v	voltage gain variation with line current	R_t = 150 Ω; RFC = 0; 100 mA with respect to 20 mA; note 10	–	0	±0.5	dB
t_{ACsu}	AC start-up time (with clock V_{clk})	C_{VDD} = 470 µF; I_{line} = 20 mA; note 11	–	140	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(p-p)}$	hearing protection output voltage swing (peak-to-peak value)	V_{DD} = 5 V; receive gain set to +11 dB differential; $R_l = \infty\ \Omega$; RFC = 1; V_{LN} = 2 V (RMS); HPL = 0 default	–	2.3	–	V
		V_{DD} = 5 V; receive gain set to +11 dB differential; $R_l = \infty\ \Omega$; RFC = 1; V_{LN} = 2 V (RMS); switchable HPL = 1; note 1	–	5.9	–	V
$V_{o(rms)}$	output voltage (RMS value); THD = 2%	single-ended; RFC = 0; HPL = 1; Z_l = 150 Ω + 100 µF at QR; (+3 dB receiver gain); GRAx = 001001; note 19	0.45	–	–	V
		differential; RFC = 0; HPL = 1; R_l = 150 Ω; (+3 dB receiver gain); GRAx = 000011; note 19	0.45	–	–	V
		differential; RFC = 0; HPL = 1; R_l = 450 Ω; (+3 dB receiver gain); GRAx = 000011; note 19	0.84	–	–	V
		differential; RFC = 1; C_l = 80 nF; f = 3.4 kHz; (+3 dB receiver gain); GRAx = 000011; note 19	0.9	–	–	V
$V_{no(rms)}$	noise output voltage (RMS value); Z_{line} = 220 Ω + (820 Ω//115 nF)	differential; 150 Ω between MIC+ and MIC–; R_l = 150 Ω; psophometrically weighted (O41 curve); (–6 dB receiver gain); GRAx = 100110	–	–82	–	dBmp
V_{DCos}	DC offset voltage between QR+/QR–	(–6 dB receiver gain); GRAx = 100110	–	–	±100	mV
Sidetone balance adjustment						
Z_{oss}	internal balance impedance Z_{oss} to match the external load impedance at pin LN ($Z_{line} = Z_{oss}$) for optimum sidetone suppression; $Z_{oss} = R_{sa} + (R_{sb}//C_s)$; [$f_{ps} = 1/(2\pi \times R_{sb} \times C_s)$]	ZOSAx = 1010 default; note 20	–	492	–	Ω
		ZOSBx = 0110 default; note 20	–	1259	–	Ω
		ZOSPx = 1001 default; note 20	–	134	–	nF
$R_{sa(min)}$	minimum selectable value Z_{oss} for range R_{sa}	ZOSAx = 0000; notes 1 and 21	–	134	–	Ω
$R_{sa(max)}$	maximum selectable value Z_{oss} for range R_{sa}	ZOSAx = 1010; notes 1 and 21	–	492	–	Ω
$R_{sb(min)}$	minimum selectable value Z_{oss} for range R_{sb}	ZOSBx = 0000; notes 1 and 21	–	465	–	Ω
$R_{sb(max)}$	maximum selectable value Z_{oss} for range R_{sb}	ZOSBx = 1011; notes 1 and 21	–	2216	–	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{s(min)}$	minimum selectable value Z_{oss} for range C_s	ZOSPx = 0000; note 22	–	55	–	nF
$C_{s(max)}$	maximum selectable value Z_{oss} for range C_s	ZOSPx = 1111; note 22	–	259	–	nF
Sidetone suppression						
$G_{v(st)}$	voltage gain from MIC+/MIC– to QR outputs; Z_{line} = 492 Ω + (1259 Ω//134 nF)	differential output; R_l = 150 Ω; f = 300 Hz; Z_{oss} = default; note 23	–	11	15	dB
		differential output; R_l = 150 Ω; f = 1 kHz; Z_{oss} = default; note 23	–	5	10	dB
		differential output; R_l = 150 Ω; f = 3.4 kHz; Z_{oss} = default; note 23	–	9	15	dB
Dial output connection: DOC (open-drain output)						
$I_{DOCsink}$	output sink current	V_{DOC} = 12 V; DPI = 0	–	0	100	nA
		V_{DOC} = 0.4 V; V_{DD} = 2.5 V; DPI = 1	200	400	–	µA
Line current control: LN and SLPE						
$I_{line(min)}$	typical minimum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 00001; note 1	–	15	–	mA
$I_{line(max)}$	typical maximum value of DC line current that can be read as a bit code via the I²C-bus	LCx = 11110; note 1	–	91	–	mA
$I_{line(step)}$	DC line current step resolution	note 24	–	≈2.5	–	mA
I²C-bus inputs/outputs: SDA and SCL						
	in accordance with standard	note 25				
Clock input: CLK						
$V_{clk(p-p)}$	input signal voltage level (peak-to-peak value)	f_i = 3.579545 MHz	200	–	VMC–V_{SS}	mV
Δf/f	input frequency tolerance with respect to f_i = 3.579545 MHz	note 26	–	–	±0.5	%
R_i	input resistance		–	800	–	Ω
C_i	input capacitance		–	4	–	pF

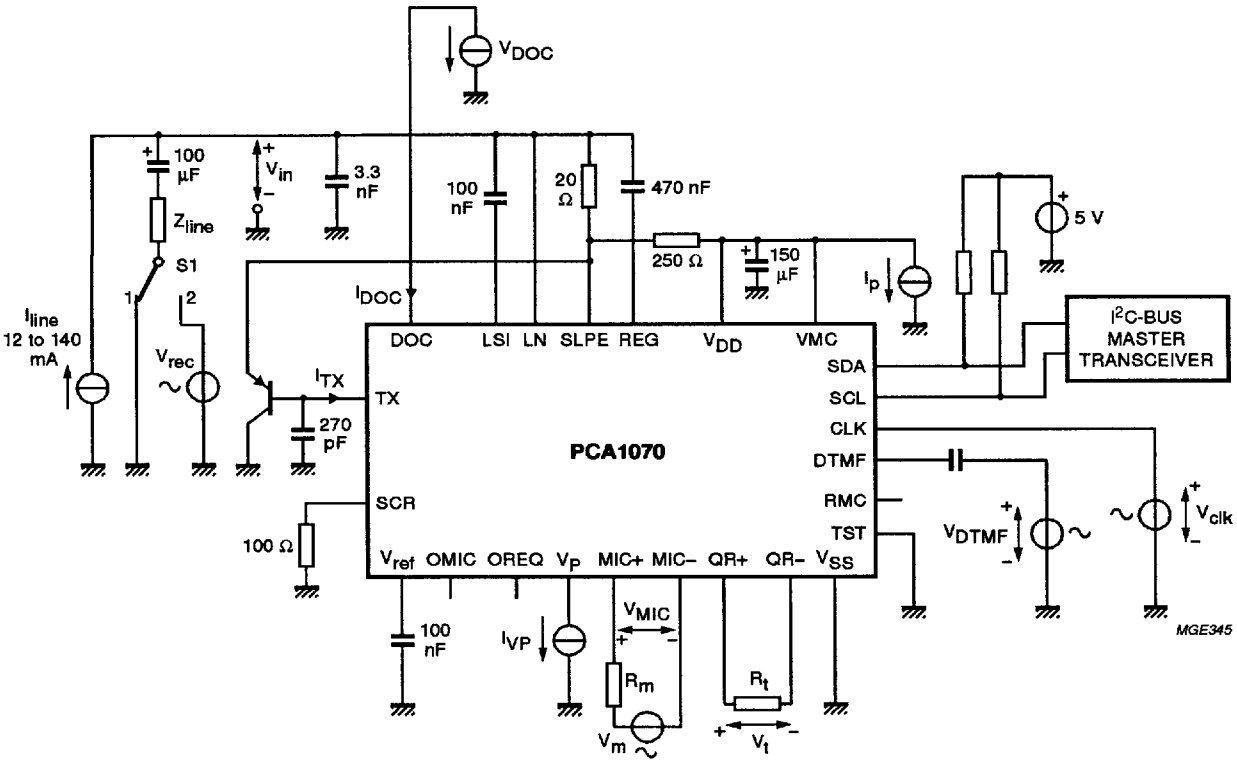
Notes to the characteristics

1. Programmable via the I²C-bus; bit codes are given in Chapter "I²C-BUS PROGRAMMING".
2. Time needed to reach default DC reference voltage V_{SLPE} (±10% from final value);
   a) Time depends strongly on the value of the capacitor(s) at V_{DD} and VMC; with a lower value of C_{VDD} the DC start-up time decreases.
   b) The start-up time can be reduced considerably by programming the bit code DST = 1 during the start-up procedure. In practice this is possible as soon as the microcontroller has become operational.
3. Time needed to reach DC reference voltage V_{SLPE} (±10% from final value).
4. The supply voltage V_{DD} is determined by the regulated DC voltage at pin SLPE and by the voltage drop between pin SLPE and V_{DD}; see Chapter "Functional description".
5. Relaxed performance means: parameters can deviate from their specified values.
6. Rejection between supply pin V_{DD} and V_P. Rejection between pin LN and V_P can be calculated by adding the attenuation of the first-order low-pass filter (R = 250 Ω, C = 150 µF) between SLPE and V_{DD}.
7. Switching level of V_{DD} below which the internal reset is active. If V_{DD} is above this level, the default values have been loaded into the internal registers.
8. RMC changes from logic 1 to logic 0 when voltage on pin VMC is increasing; RMC changes from logic 0 to logic 1 when voltage on pin VMC is decreasing; see Fig.4.
9. Common mode signal is applied via 2 × 470 Ω external resistors connected to pins MIC+ and MIC–.
10. Not tested, guaranteed by design.
11. Time needed to reach default gain settings (± 3 dB value).
12. At low gain settings the confidence tone gain will be slightly higher than the calculated value.
13. The set impedance between pin LN and V_{SS} consists of $R_a + (R_b//C)$ in parallel with an artificial inductor L_{eq} and internal resistors R_p and R_{LSI} and internal capacitor C_p. See Chapter "Functional description".
14. Without clock the set impedance is automatically set to Z_s = 600 Ω (typ.).
15. Balance Return Loss indicates the deviation of an impedance with respect to a reference impedance.
    BRL = 20 log|$(Z_{LN} + Z_{ref})/(Z_{LN} - Z_{ref})$| where $Z_{LN} \approx R_a + (R_b//C)$ is the impedance seen into pin LN
    $Z_{ref} = R_{a(ref)} + (R_{b(ref)}//C_{ref})$ is the reference impedance.
16. Value '0' can also be programmed.
17. Value f_p = 12 kHz can also be programmed.
18. Attack and release times are also valid under low current and low voltage conditions.
19. The maximum possible output swing depends on the DC conditions (the programmed voltage V_{SLPE} and the load on the supply pin V_{DD}) and on the gain setting of the receive channel.
20. Without clock the sidetone balance impedance is automatically set to Z_{oss} = 600 Ω (typ.).
21. Exact values can be found in Tables 15, 16 and 17.
22. value C_s = 5 nF can also be programmed.
23. Gain microphone channel G_M = default (typ. 41 dB); gain receive channel G_{rec} = default (typ. –6 dB); sidetone gain G_{st} minimum sidetone suppression at f = 300 Hz and 3400 Hz is: $G_M + G_R - G_{st(max)} = 41 - 6 - 15 = 20$ dB.
24. Indication only; exact values can be found in Table 17.
25. Standard I²C specifications are valid for $V_{DD} \geq 2.5$ V. Relaxed specifications for V_{DD} = 1.8 to 2.5 V.
26. Recommended accuracy of input frequency; a higher tolerance will cause parameters to deviate from their specified values; note that all parameters are specified with the reference input clock frequency f_{clk} = 3.579545 MHz.

TEST AND APPLICATION INFORMATION

The test circuit is illustrated in Fig.7. The basic application circuit is illustrated in Fig.8. An interrupter with an N-channel depletion MOS transistor (e.g. BSD254A or BSP124) is shown. It is intended for applications where a low DC line voltage is required. An interrupter with an N-channel enhancement MOS transistor (e.g. BSN304A or BSP130) can be used for applications where a relatively high DC line voltage is allowed.

An application circuit for applications where a low DC line voltage and long line interrupts are required, is illustrated in Fig.9 (interrupter with an N-channel depletion MOS transistor).



Definitions:

Gain microphone channel $G_M = 20 \log(V_{LN}/V_M)$ with S1 in position 1; $V_{DTMF} = 0$.

Gain DTMF amplifier $G_{DTMF} = 20 \log(V_{LN}/V_{DTMF})$ with S1 in position 1; $V_m = 0$.

Gain receive channel $G_{rec} = 20 \log(V_T/V_{LN})$ with S1 in position 2; $V_m = 0$.

Sidetone gain $G_{st} = 20 \log(V_T/V_M)$ with S1 in position 1; $V_{DTMF} = 0$.

Fig.7 Test circuit of the PCA1070.

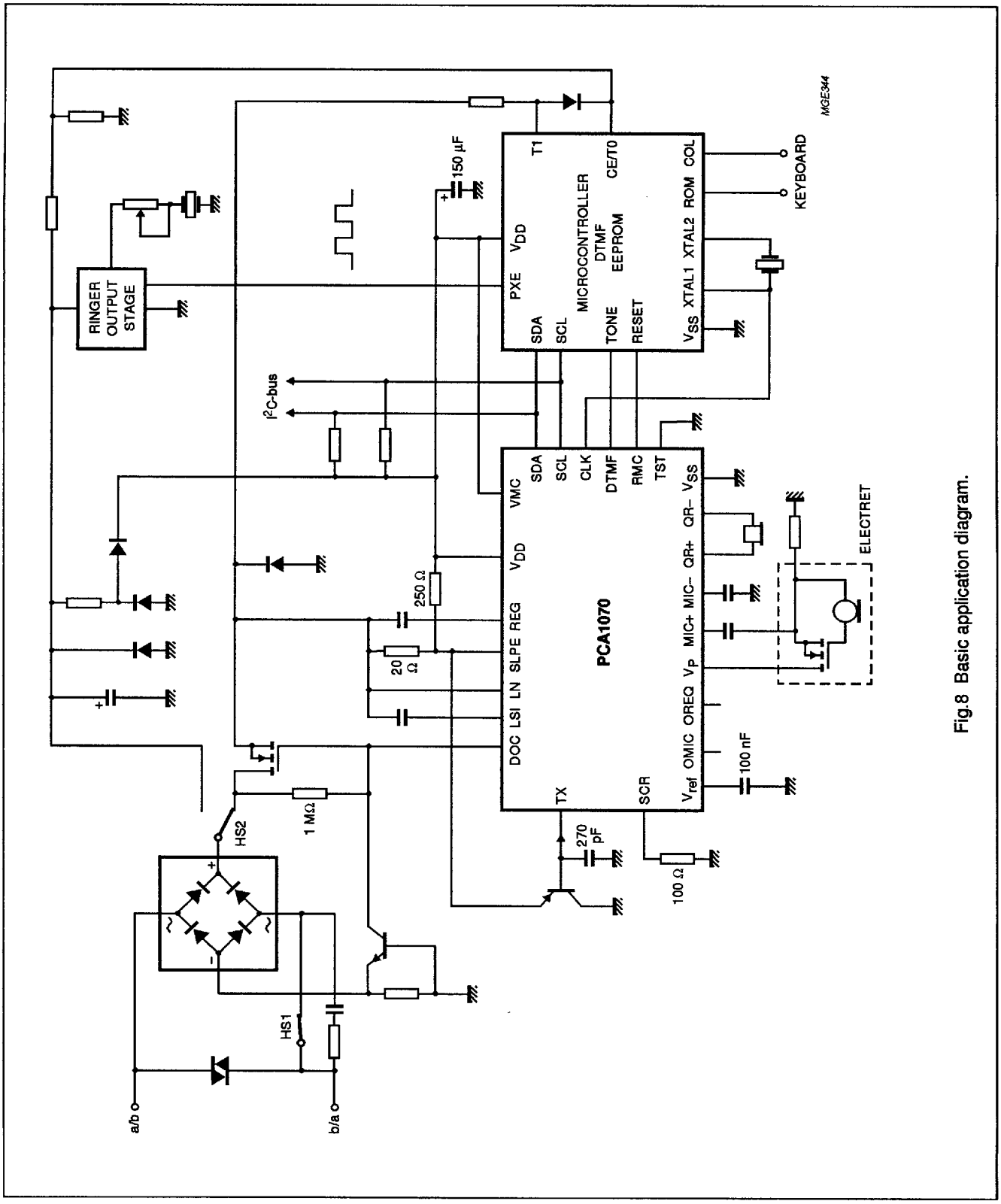


Fig.8 Basic application diagram.

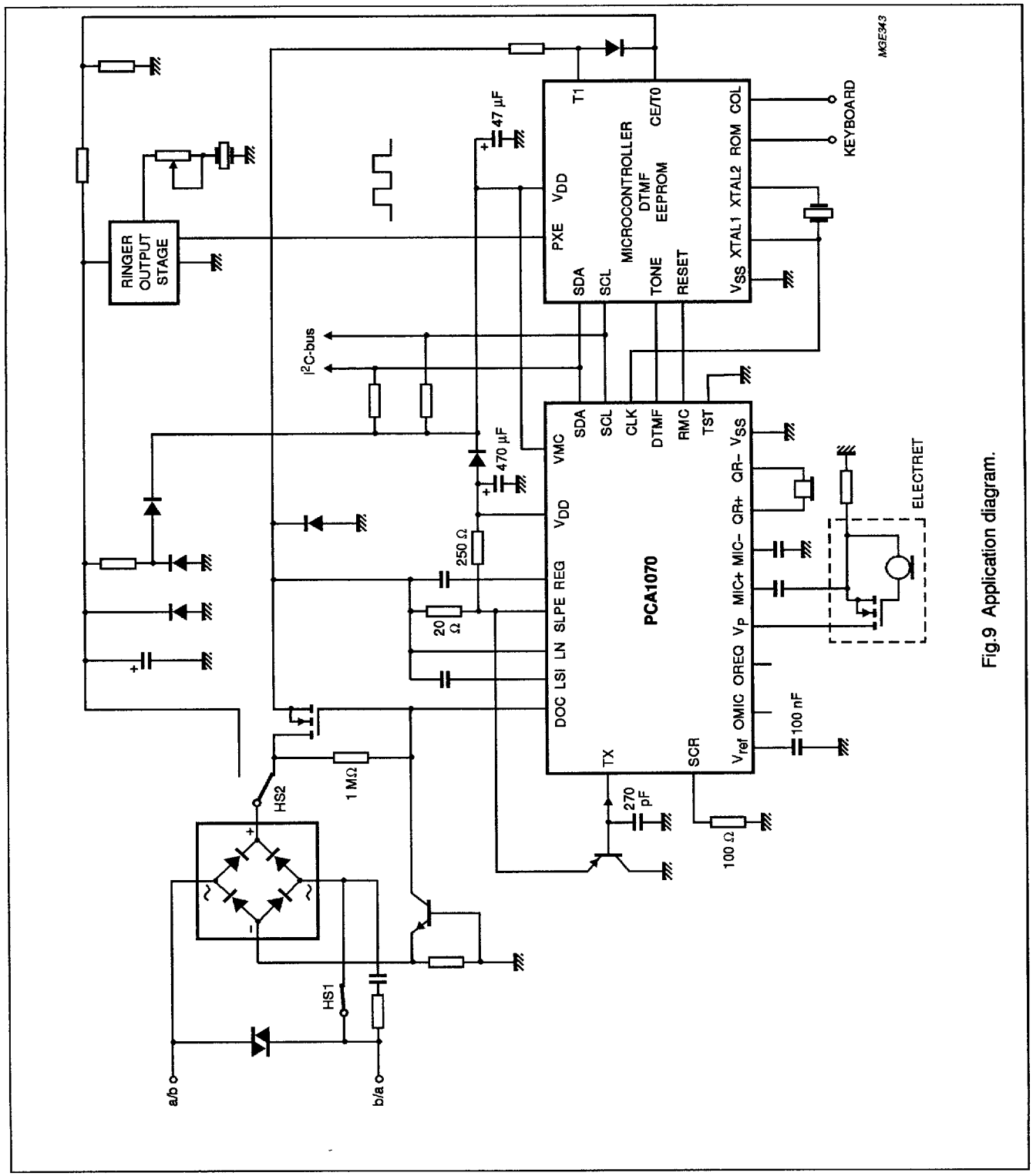
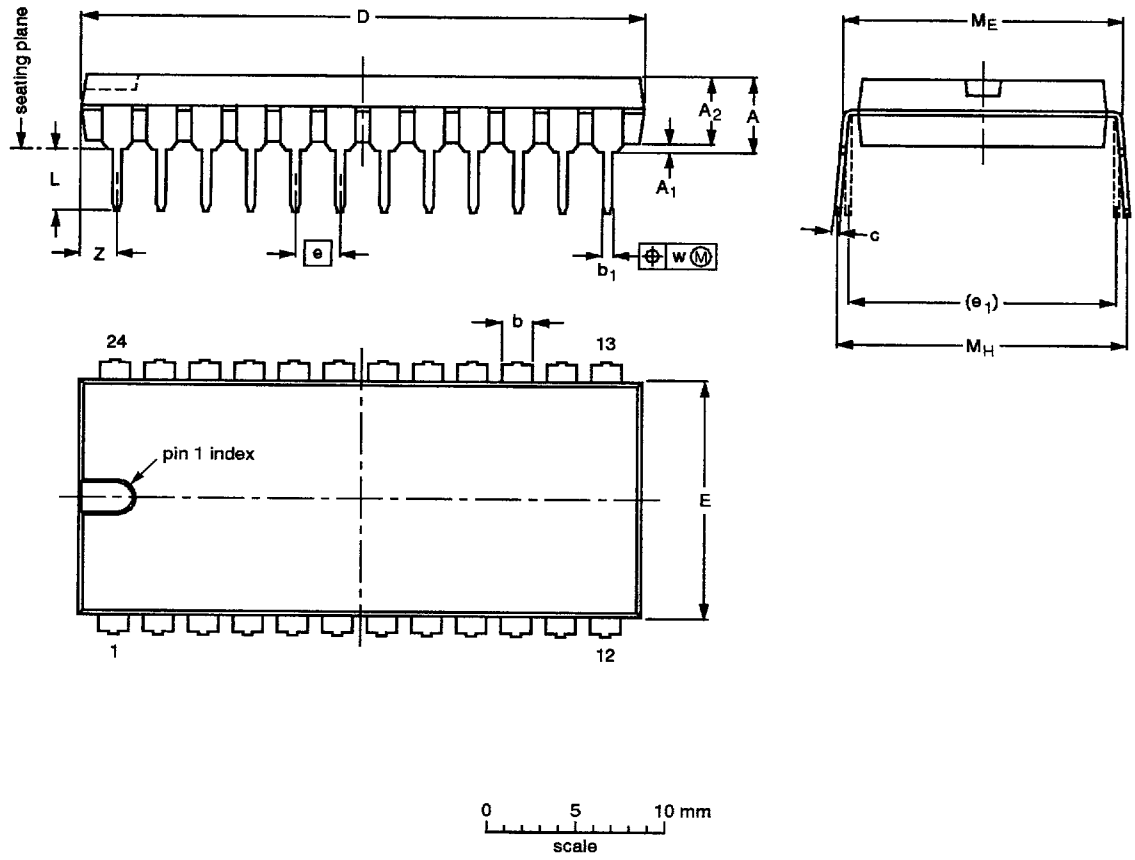


Fig.9 Application diagram.

PACKAGE OUTLINE

DIP24: plastic dual in-line package; 24 leads (600 mil) **SOT101-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

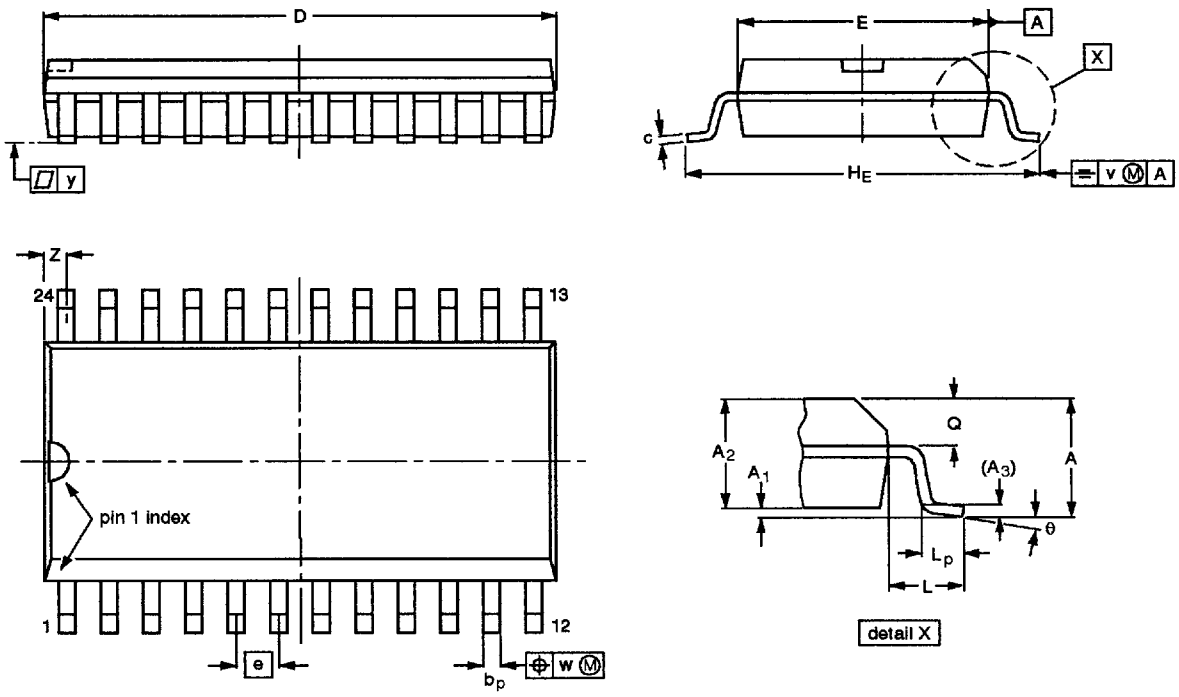
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

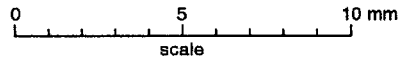
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT101-1	051G02	MO-015AD				~~92-11-17~~ 95-01-23

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used
- The longitudinal axis of the package footprint must be parallel to the solder flow
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.