Signetics

2964B
Dynamic Memory Controller

Product Specification

Logic Products

FEATURES

- **Operating Options — controls 16K or 64K DRAMs**
- **8-Bit Refresh Counter — refresh address generation, clear input, and selectable terminal count (128 or 256) output**
- **Row Address Decoder — four Active *R*ow *A*ddress *S*elect (RAS) outputs during refresh**
- **On-Chip Latches — dual 8-bit address latches and RAS decoder latches**
- **User-Selectable Refresh Modes — burst, distributed or transparent**
- **3-port, 8-bit address multiplexer with Schottky speed**
- **Non-inverting address for RAS and CAS signal paths**

PRODUCT DESCRIPTION

The Signetics 2964B **D**ynamic **M**emory **C**ontroller (DMC) provides address multiplexing, refresh address generation, and RAS/CAS control for dynamic RAMs of any data width. The eight-bit address path is designed for 64K DRAMs but can be used equally well with 16K DRAMs. Sixteen address input latches and two row address select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K DRAMs) by using the internal RAS decoder to select from one-of-four banks of DRAMs.

FUNCTIONAL OPERATION

The Signetics 2964B Dynamic Memory Controller (Figure 1) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the DRAM address lines.

The 2964B also includes a special RAS decoder and CAS buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The RAS Decoder allows upper addresses to select one-of-four banks of DRAM by determining which bank receives an RAS input. During refresh (RFSH = LOW), the decoder mode is changed to four-of-four and all banks of

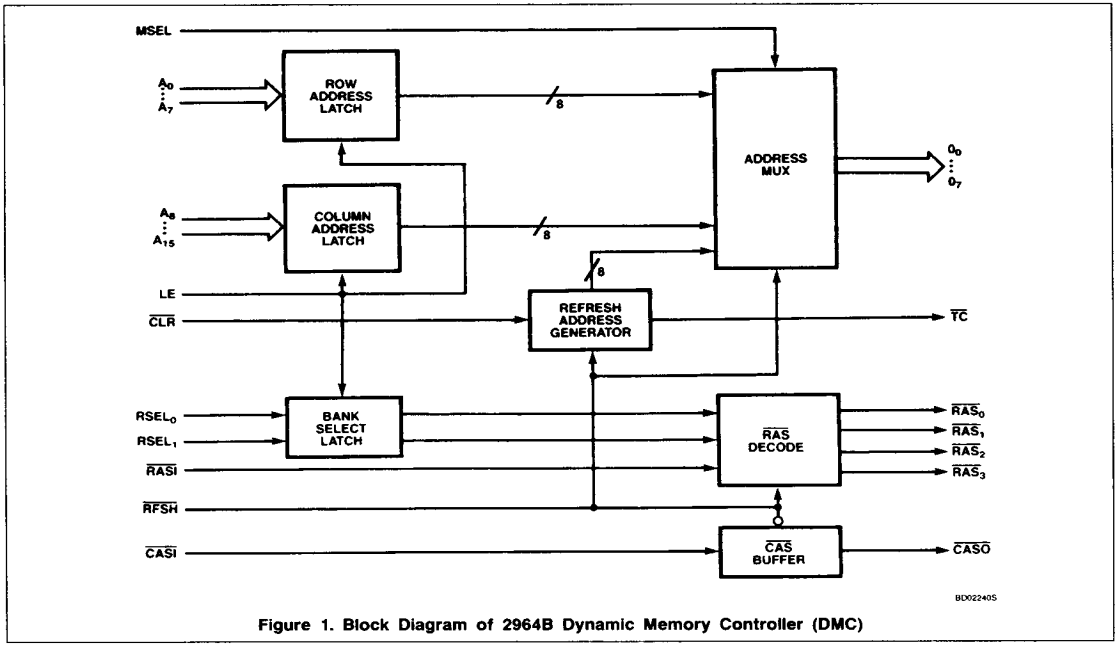

Figure 1. Block Diagram of 2964B Dynamic Memory Controller (DMC)

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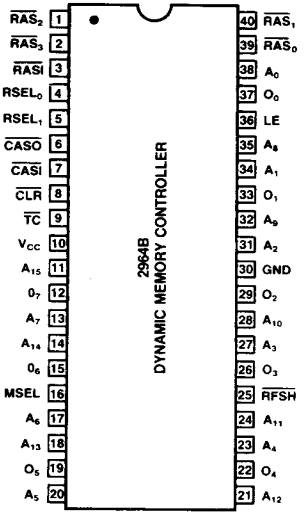
2964B PACKAGE/PIN DESIGNATIONS



PIN NO.	IDENTIFIER	FUNCTION
1, 2, 39 and 40	$\overline{RAS}_2$, $\overline{RAS}_3$ $\overline{RAS}_0$, $\overline{RAS}_1$	Row Address Strobe outputs ($\overline{RAS}_i$). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active LOW. All $\overline{RAS}_{0\text{-}3}$ outputs go active low in response to $\overline{RASI}$ when $\overline{RFSH}$ goes LOW.
3	$\overline{RASI}$	The Row Address Strobe input. During normal memory cycles, the selected $\overline{RAS}$ Decoder output, $\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$ or $\overline{RAS}_3$, will go active LOW in response to an active LOW input at $\overline{RASI}$. During refresh (RFSH = LOW), all $\overline{RAS}$ outputs go LOW in response to $\overline{RASI}$ = LOW.
4 and 5	$RSEL_0$ and $RSEL_1$	The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs (normally higher-order addresses) is decoded by the $\overline{RAS}$ Decoder to "$\overline{RAS}$ Select" one of four banks of memory with $\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$ or $\overline{RAS}_3$.
6	$\overline{CASO}$	The Column Address Strobe output. The active LOW $\overline{CASO}$ output strobes the Column Address into the dynamic RAM. $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = LOW).
7	$\overline{CASI}$	The Column Address Strobe. An active LOW input at $\overline{CASI}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = LOW).
8	$\overline{CLR}$	The refresh counter Clear input. An active LOW input at $\overline{CLR}$ resets the refresh counter to all LOW (refresh address output to all HIGH).
9	$\overline{TC}$	The Terminal Count output. A LOW output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15}. The $\overline{TC}$ output remains active LOW until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.
10	V_{CC}	+5V power supply
11, 14, 18, 21, 24, 28, 32 and 35	$A_{15} - A_8$	The high-order Address inputs are used to latch eight Column Address inputs for the DRAM. These inputs drive the outputs $O_0 - O_7$ when MSEL is LOW — see next paragraph. A_{15} is a dual input. With normal TTL level inputs. A_{15} acts as an address input for 64K DRAMs. If A_{15} is pulled up to +12V through a 1K resistor, the terminal count output $\overline{TC}$ will go LOW every 128 counts (for 16K DRAMs) instead of every 256 counts.
12, 15, 19, 22, 26, 29, 33 and 37	$O_7 - O_0$	The DRAM address outputs. The eight-bit width is designed for DRAMs up to 64K.
13, 17, 20, 23, 27, 31, 34 and 38	$A_7 - A_0$	The low-order Address inputs are used to latch eight Row Address inputs for the DRAM. These inputs drive the outputs $O_0 - O_7$ when MSEL is HIGH.
16	MSEL	The Multiplexer-SELect input determines whether low-order or high-order address inputs appear at the multiplexer outputs $O_0 - O_7$. When MSEL is HIGH, the low-order address latches ($A_0 - A_7$) are connected to the outputs. When MSEL is LOW, the high-order address latches are connected to the outputs.

2964B PACKAGE/PIN DESIGNATIONS (Continued)

PIN NO.	IDENTIFIER	FUNCTION
25	$\overline{RFSH}$	The Refresh control input. When active LOW, the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{RFSH}$ LOW also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS}_0$, $\overline{RAS}_1$, $\overline{RAS}_2$ and $\overline{RAS}_3$, go LOW in response to a LOW input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each cycle by the LOW-to-HIGH transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh. $\overline{RFSH}$ may be held LOW and refresh accompanied by toggling $\overline{RASI}$.
30	GND	Ground.
36	LE	The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.

memory receive an RAS input for refresh in response to an RASI active LOW input. CAS is inhibited during refresh.

Burst mode refresh is accomplished by holding RFSH low and toggling RASI.

A_{15} is a dual function input which controls the refresh counter's range. For 64K DRAMs, it is an address input. For 16K DRAMs, it can be pulled to +12V through 1K to terminate the refresh count at 128 instead of 256.

TRUTH TABLES:
$\overline{RAS}$ OUTPUT FUNCTIONS

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RESEL_0$	$\overline{RAS}_0$	$\overline{RAS}_1$	$\overline{RAS}_2$	$\overline{RAS}_3$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ FUNCTION

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTIONS

MSEL	$\overline{RFSH}$	$0_0 - 0_7$
H	H	$A_0 - A_7$
L	H	$A_8 - A_{15}$
X	L	Refresh Address

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REFRESH ADDRESS COUNTER FUNCTION

A_{15}	CLR	$\overline{RFSH}$	$\overline{RASI}$	$\overline{TC}$	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF_H	Clear counter
X	H		X	X	NC	Output refresh address no change for counter
X	H		L	X	Count – 1	Return to memory cycle mode and decrement counter
X	H	L		X	NC	Output all RASI to RAM no change for counter
X	H	L		X	Count – 1	Return RAS_i to HIGH and decrement counter
L or H	H	X	X	L	00_H	Terminal count for 256 line refresh
+12V*	H	X	X	L	00_H and 80_H	Terminal count for 128 line refresh

*Through 1KΩ resistor.

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage temperature	–65 to +150°C
Temperature (ambient) under bias	–55 to +125°C
Supply voltage to ground potential	–0.5 to +7.0V
DC voltage applied to outputs for high output state	+0.5V to $+V_{CC}$ MAX
DC input voltage	–0.5 to 5.5V
DC output current, into outputs	30mA
DC input current	–30 to +5.0mA

DC ELECTRICAL CHARACTERISTICS Commercial: $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V$ ($\pm 5\%$), (Min = 4.75V), (Max = 5.25V)

DESCRIPTION		TEST CONDITIONS[1]		2964B			UNIT
				Min	Typ[2]	Max	
V_{OH}	Output HIGH voltage	V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL}, $I_{OH} = -1mA$	$\overline{TC}$	2.5			V
			Others	3.0			V
V_{OH}	Output HIGH voltage	V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL}, $I_{OH} = -15mA$	All outputs except $\overline{TC}$	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = MIN, $V_{IN} = V_{IH}$ or I_{IL}	All outputs except $\overline{TC}$, $I_{OL} = 16mA$			0.5	V
			$\overline{TC}$, $I_{OL} = 8mA$			0.5	V
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, $I_{IN} = -18mA$				-1.5	V
I_{IL}	Input LOW current	V_{CC} = MAX, $V_{IN} = 0.4V$	$\overline{RASI}$			-3.2	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			-1.6	mA
			$A_0 - A_{15}$, $\overline{CLR}$, $RSEL_{0,1}$, LE			-0.4	mA
I_{IH}	Input HIGH current	V_{CC} = MAX, $V_{IN} = 2.7V$	$\overline{RASI}$			100	μA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			50	μA
			$A_0 - A_{15}$, $\overline{CLR}$, $RSEL_{0,1}$, LE			20	μA
I_I	Input HIGH current	V_{CC} = MAX, $V_{IN} = -5.5V$	$\overline{RASI}$			2.0	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			1.0	mA
		V_{CC} = MAX, $V_{IN} = 5.5V$	$A_0 - A_{15}$, $\overline{CLR}$, $RSEL_{0,1}$, LE			0.1	mA
I_{SC}	Output short circuit current	V_{CC} = MAX (note 3)		-40		-100	mA
I_{CC}	Power supply current (note 4)	25°C, 5V	Com'l		122		mA
		0 to 70°C				173	mA
		70°C				165	mA
I_T	A_{15} Enable current	A_{15} connected to +12V through 1KΩ ±10%				5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under DC Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), $\overline{RASI}$ and $\overline{CASI}$ are HIGH and all other inputs are LOW.

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AC ELECTRICAL CHARACTERISTICS

Tables 1 and 2 specify performance characteristics of the Signetics 2964B over the operating range for capacitive loads of 50 and 150 picofarads, respectively. Note that the minimum specified limits for t_{PW}, t_S, and t_H are for minimum system operating requirements and that limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device. All AC parameters are specified at 1.5 volts.

Table 1. Performance Characteristics for Capacitive Loading of 50 Picofarads

PARAMETER — See Figure 2.	DESCRIPTION	$T_A = +25°C$ $V_{CC} = 5.0V$	COMMERCIAL $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$		UNIT
		Typ	Min	Max	
1 t_{PD}	A_i to O_i Delay	14		19	ns
2 t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	14		20	ns
3 t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	14		20	ns
4 t_{PD}	MSEL to O_i	17	9		ns
5 t_{PD}	MSEL to O_i	17		21	ns
6 t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	12		17	ns
7 t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	15		20	ns
8 t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	30		40	ns
9 t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	25		35	ns
10 t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		ns
11 t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		ns
12 t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	17		21	ns
13 t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	19		26	ns
14 t_{PW}	$\overline{CLR}$ = L	10	30		ns
15 t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 1)	16		21	ns
16 t_{PD}	LE to O_i	25		35	ns
17 t_{PHL}	LE to $\overline{RAS_i}$	30		40	ns
18 t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	35		45	ns
19 t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	31		44	ns
20 t_S	A_i to LE Set-up time	0	5		ns
21 t_H	A_i to LE Hold time	5	12		ns
22 t_S	$RSEL_i$ to LE Set-up time	0	5		ns
23 t_H	$RSEL_i$ to LE Hold time	10	17		ns
24 t_S	$\overline{CLR}$ Recovery time	10	16		ns
25 t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 2)	2		5	ns
26 t_{SKEW}	O_i to $\overline{CASO}$ (Note 2)	6		8	ns
27 t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 3)	6		8	ns
28 t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = Z, Note 4)	1		5	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Table 2. Performance Characteristics for Capacitive Loading of 150 Picofarads

PARAMETER — See Figure 2.	DESCRIPTION	$T_A = +25°C$ $V_{CC} = 5.0V$	COMMERCIAL $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$		UNIT
		Typ	Min	Max	
1 t_{PD}	A_i to O_i Delay	20		25	ns
2 t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	18		24	ns
3 t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	18		24	ns
4 t_{PD}	MSEL to O_i	23	12		ns
5 t_{PD}	MSEL to O_i	23		27	ns
6 t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	17		24	ns
7 t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	19		27	ns
8 t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	34		45	ns
9 t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	32		45	ns
10 t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		ns
11 t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		ns
12 t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	21		27	ns
13 t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	25		33	ns
14 t_{PW}	$\overline{CLR}$ = L	10	30		ns
15 t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 1)	21		27	ns
16 t_{PD}	LE to O_i	30		40	ns
17 t_{PHL}	LE to $\overline{RAS_i}$	34		45	ns
18 t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	39		55	ns
19 t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	38		50	ns
20 t_S	A_i to LE Set-up time	0	5		ns
21 t_H	A_i to LE Hold time	5	12		ns
22 t_S	$RSEL_i$ to LE Set-up time	0	5		ns
23 t_H	$RSEL_i$ to LE Hold time	10	17		ns
24 t_S	$\overline{CLR}$ Recovery time	10	16		ns
25 t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 2)	3		6	ns
26 t_{SKEW}	O_i to $\overline{CASO}$ (note 2)	6		8	ns
27 t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 3)	6		9	ns
28 t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL ⌝⌞, Note 4)	1		5	ns

NOTES:
1. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
2. O_i to $\overline{RAS_i}$, ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
3. O_i to $\overline{RAS_i}$, ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
4. O_i to $\overline{RAS_i}$ (MSEL ⌝⌞) skew is guaranteed maximum difference between fastest MSEL ⌝⌞ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

TIMING DIAGRAM

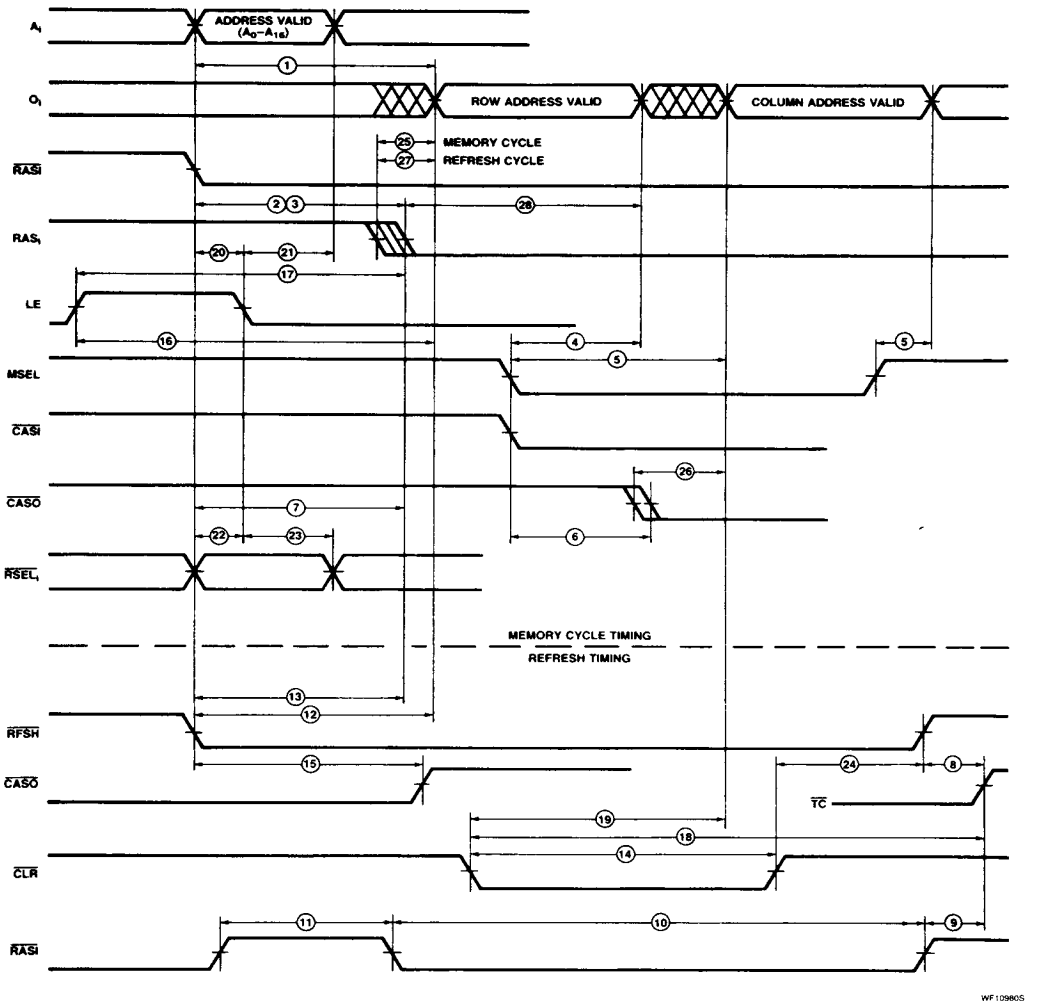


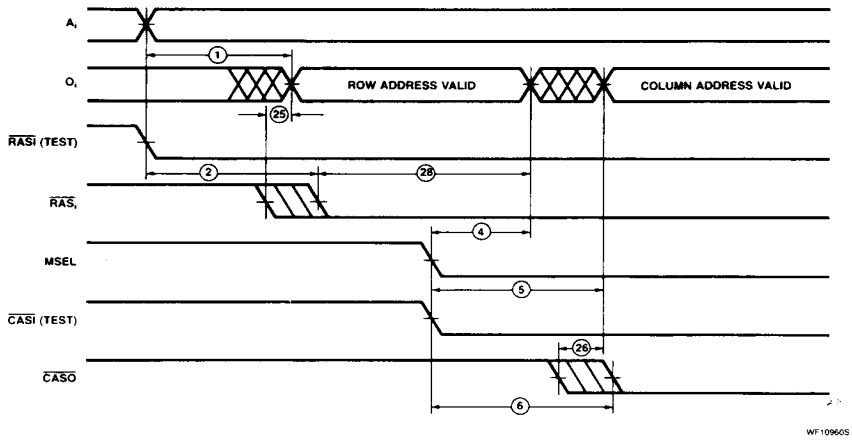
Figure 2. Dynamic Memory Controller Timing

MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1, T_2, and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that DRAM timing requirements are met and that maximum system performance is achieved.

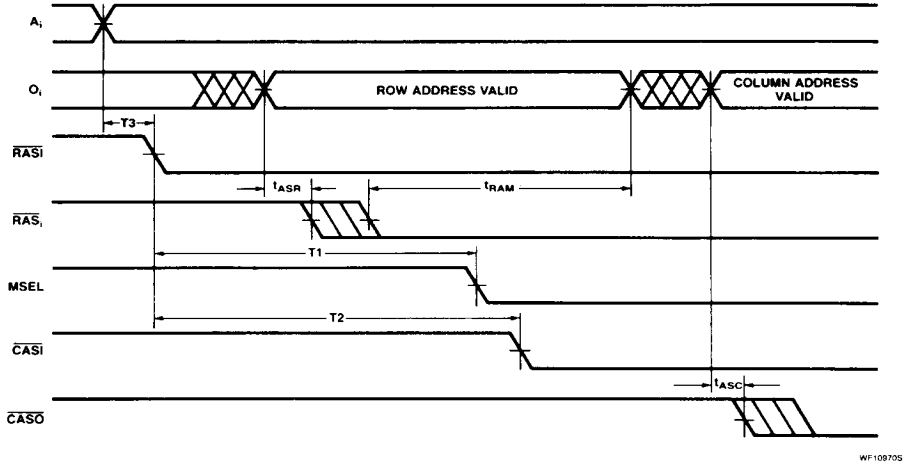
The minimum requirements for T_1, T_2, and T_3 are as follows:

$T_1MIN = t_{RAH} + t_{28}$
$T_2MIN = t_1 + t_{26} + t_{ASC}$
$T_3MIN = t_{ASR} + t_{25}$ where,
t_{RAH} = Row Address Hold Time
t_{ASC} = Column Address Set-up Time
t_{ASR} = Row Address Set-up Time



Legend
㉕ = Guaranteed maximum difference between fastest $\overline{RASI}_1$ to $\overline{RAS}$ delay and the slowest A_1 to O_1 delay on any single device.
㉖ = Guaranteed maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and the slowest MSEL to 0_1 delay on any single device.
㉘ = Guaranteed maximum difference between fastest MSEL to O_i delay and the slowest RASI to RAS_i delay on any single device.

a. Specifications Applicable to Memory Cycle Timing



b. Desired System Timing

Figure 3. Memory Cycle Timing

REFRESH CYCLE TIMING

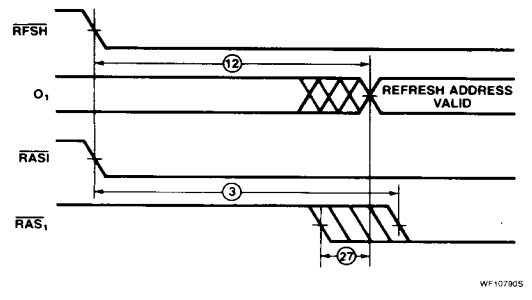
The timing relationships for refresh are shown in Figure 4.

T_4 minimum is calculated as follows:

$$T_4 = t_{ASR} + t_{27}$$

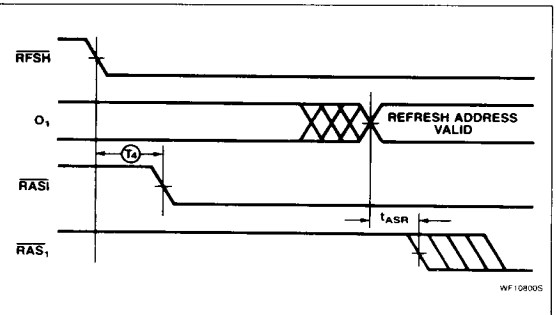
Burst refresh timing is shown in Figure 5.

AC WAVEFORMS



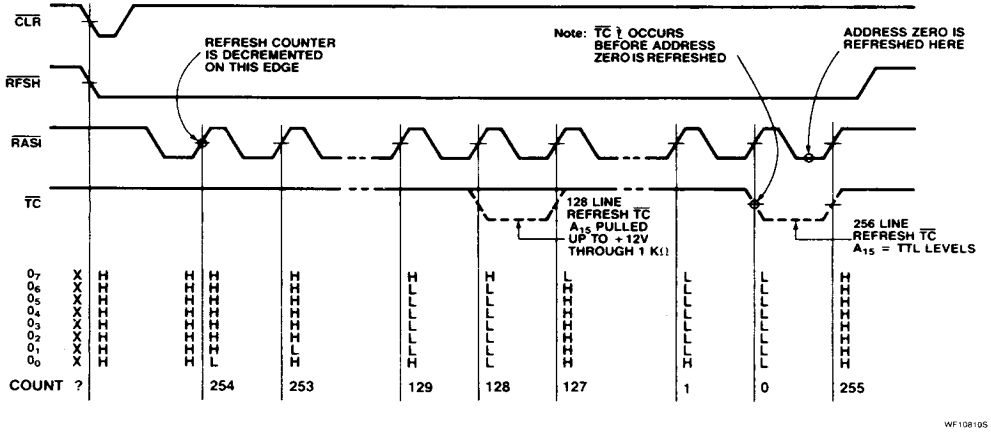
㉗ = Guaranteed maximum difference between fastest $\overline{RASi}_1$ to $\overline{RAS}$ delay and the slowest $\overline{RFSH}$ to O_1 delay on any single device.

Figure 4a. Refresh Timing — Test Waveforms



㉗ = Guaranteed maximum difference between fastest $\overline{RASi}_1$ to $\overline{RAS}$ delay and the slowest $\overline{RFSH}$ to O_1 delay on any single device.

Figure 4b. Refresh Timing — Desired System Timing



NOTE:
The timing shown assumes that burst mode applications may power-down the 2964B with the RAM. Therefore, the counter is cleared prior to executing the refresh sequence

Figure 5. Burst Refresh Timing

ORDERING INFORMATION

Commercial:
N2964BN (Plastic)
N2964BI (Ceramic)

PACKAGE DATA

Type: Plastic or Ceramic
Configuration: DIP
Width: 0.6 in.
Length: 2.0 in.
Pin Centers: 0.1 in.

APPLICATIONS

Speed with Minimum Skew

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, RAS and CAS paths is minimized (and specified) by placing these functions on the same chip. The inclusion of the CAS buffer allows matching of its propagation delay, and also provides the CAS inhibit function during RAS — only refresh.

Input Latches

The eighteen input latches are transparent when LE is HIGH and latch the input data, meeting the set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

Refresh Counter

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of RFSH (or RASI). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by CLR. This actually causes all output to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting.)

Refresh Terminal Count

The refresh counter also provides a Terminal Count output for burst mode refresh applications. TC normally occurs at count 255 (00_7 to 0_7 all LOW when RFSH is LOW). TC can be made to occur at count 127 for 128 line burst mode refresh by pulling A_{15} up to +12V through a 1KΩ ±10% resistor. The counter actually cycles through 256 with TC determined by A_{15}. Otherwise A_{15} functions as an address input when driven at normal TTL levels.

Three-Input 8-Bit Address Multiplexer

The address MUX is 8-bits wide (for 64K DRAMs) and has three data sources, the lower address input latch (A_0 to A_7), the upper address input latch (A_8 to A_{15}), and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source — the refresh counter is selected when RFSH is LOW and overrides MSEL.

When RFSH goes LOW, the MUX selects the refresh counter address and CASO is inhibited. Also, the RAS Decoder function is changed from one-of-four to four-of-four so all RAS outputs $RAS_0 - RAS_3$ go low to refresh all banks of memory when RASI goes LOW. When RFSH is HIGH, only one RAS output goes low, determined by the RAS Select inputs, $RSEL_0$ and $RSEL_1$. In either case the RAS Decoder output timing is controlled by RASI to make sure the refresh count appears at $00_0 - 0_7$ before $RAS_0 - RAS_3$ goes LOW. This assures meeting Row address Set-up time requirement of the DRAM (t_{ASR}).

Maximum Performance System

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 6. Delay lines provide the most accurate timing and are recommended for RAS, MSEL, and CAS timing in this type of system.

Controlling 16K RAMS or Smaller Systems

16K DRAMs require seven address inputs and 128 line refresh. Also A_0 is often used to designate upper or lower byte transactions in 16-bit systems. These modifications are shown in Figure 7.

7

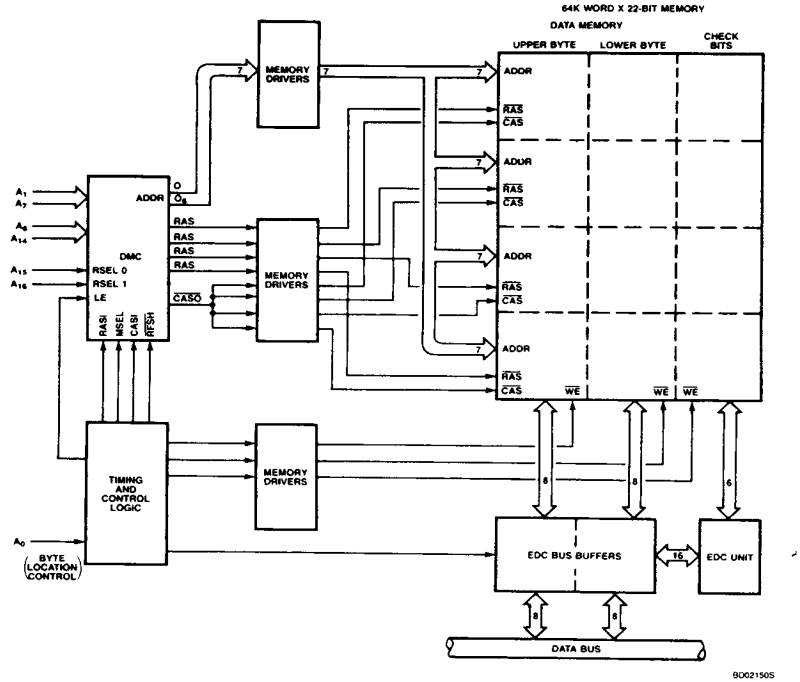
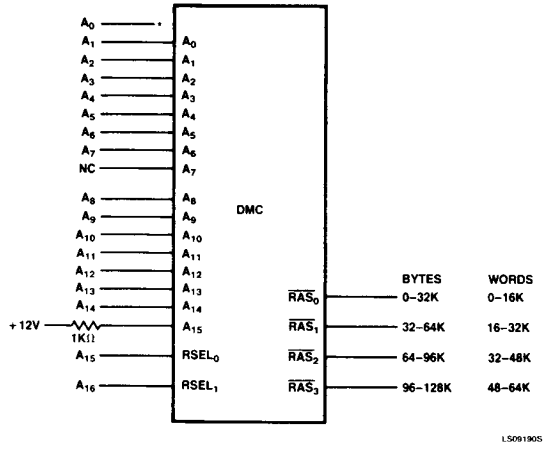


Figure 6. Dynamic Memory Control with Error Detection and Correction



*A_0 controls byte select logic.

Figure 7. Word Organized Memory Using 16K RAMs