**MC54/74HC7793**

*Product Preview*

# Octal 3-State Noninverting Transparent Latch with Readback

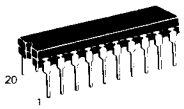
## High-Performance Silicon-Gate CMOS

The MC54/74HC7793 consists of eight noninverting transparent latches with readback. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

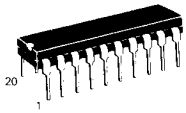
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable and Output Enable are low. Data meeting the setup and hold time is latched when either Latch Enable or Output Enable is high.

The HC7793 can enable its output data back onto its input bus via the I/O port configuration. Output Enable and Latch Enable determine how pins D0/Q0-D7/Q7 are configured. When Output Enable is high and Latch Enable is low, the outputs of the latches are enabled on D0/Q0-D7/Q7, configuring D0/Q0-D7/Q7 as an output bus so that the output data can be read back by the host.

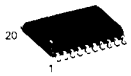
- Output Drive Capability: 10 LSTTL Loads (Q0-Q7)
  15 LSTTL Loads (D0/Q0-D7/Q7)
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 $\mu$A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



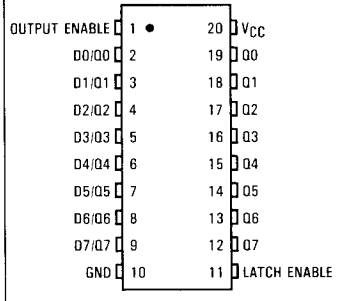
DW SUFFIX
SOIC
CASE 751D

**ORDERING INFORMATION**

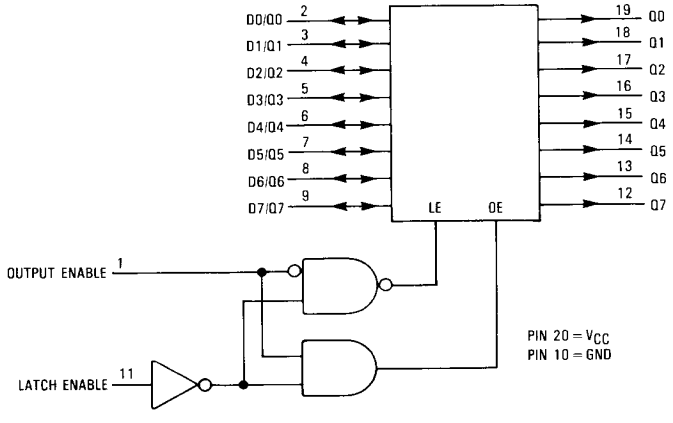
| | |
|---|---|
| MC74HCXXXXN | Plastic |
| MC54HCXXXXJ | Ceramic |
| MC74HCXXXXDW | SOIC |

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

**PIN ASSIGNMENT**




**BLOCK DIAGRAM**




**FUNCTION TABLE**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Output Enable | Latch Enable | D/Q | D/Q | Q |
| L | L | L | Input | L |
| L | L | H | Input | H |
| L | H | X | Input | Q* |
| H | L | Output | Q* | Q* |
| H | H | X | Input | Q* |

*Q represents the previous latched state.

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −1.5 to $V_{CC}$ +1.5 | V |
| $V_{out}$ | DC Input Voltage (Referenced to GND) | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{in}$ | DC Input Current, per Pin (Pins 1, 11) | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin (Pins 12-19) | ±25 | mA |
| $I_{I/O}$ | DC Output Current, per Pin (Pins 2-9) | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic or Ceramic DIP† | 750 | mW |
| | SOIC Package† | 500 | |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | °C |
| | (Plastic DIP or SOIC Package) | 260 | |
| | (Ceramic DIP) | 300 | |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltages higher than the maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either GND or $V_{CC}$). Unused outputs must be left open. I/O pins must be connected to a properly terminated line or bus. See Chapter 4 subject listing on page 4-2.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 2.0 V | 0 | 1000 | ns |
| | (Figure 1) | $V_{CC}$ = 4.5 V | 0 | 500 | |
| | | $V_{CC}$ = 6.0 V | 0 | 400 | |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low-Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | V |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 6.0$ mA<br>Pins 2-9 $\|I_{out}\| \le 7.8$ mA | 4.5<br>6.0 | 3.98<br>5.48 | 3.84<br>5.34 | 3.70<br>5.20 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 4.0$ mA<br>Pins 12-19 $\|I_{out}\| \le 5.2$ mA | 4.5<br>6.0 | 3.98<br>5.48 | 3.84<br>5.34 | 3.70<br>5.20 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 6.0$ mA<br>Pins 2-9 $\|I_{out}\| \le 7.8$ mA | 4.5<br>6.0 | 0.26<br>0.26 | 0.33<br>0.33 | 0.40<br>0.40 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 4.0$ mA<br>Pins 12-19 $\|I_{out}\| \le 5.2$ mA | 4.5<br>6.0 | 0.26<br>0.26 | 0.33<br>0.33 | 0.40<br>0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three-State Leakage Current | Output in High-Impedance State<br>$V_{in}$ = $V_{IL}$ or $V_{IH}$<br>$V_{out}$ = $V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

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**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Input Data to Q (Figures 1 and 5) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Latch Enable or Output Enable to Q (Figures 2 and 5) | 2.0 | 175 | 220 | 265 | ns |
| | | 4.5 | 35 | 44 | 53 | |
| | | 6.0 | 30 | 37 | 45 | |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Latch Enable or Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Latch Enable or Output Enable to D0/Q0-D7/Q7 (Figures 3 and 6) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, D0/Q0-D7/Q7 | 2.0 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Q0-Q7 (Figures 1 and 5) | 2.0 | 75 | 95 | 110 | ns |
| | | 4.5 | 15 | 19 | 22 | |
| | | 6.0 | 13 | 16 | 19 | |
| $C_{in}$ | Maximum Input Capacitance (Pins 1, 11) | — | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum I/O Capacitance (I/O in High-Impedance State) | — | 15 | 15 | 15 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

| | | | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Latch)<br>Used to determine the no-load dynamic power consumption:<br>$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$<br>For load considerations, see Chapter 4 subject listing on page 4-2. | Typical @ 25°C, $V_{CC}$ = 5.0 V<br>TBD | pF |

**TIMING REQUIREMENTS** (Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $t_{su}$ | Minimum Setup Time, Input Data to Latch Enable (Figure 4) | 2.0 | 100 | 125 | 150 | ns |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| $t_h$ | Minimum Hold Time, Latch Enable to Input Data (Figure 4) | 2.0 | 5 | 5 | 5 | ns |
| | | 4.5 | 5 | 5 | 5 | |
| | | 6.0 | 5 | 5 | 5 | |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 1) | 2.0 | 1000 | 1000 | 1000 | ns |
| | | 4.5 | 500 | 500 | 500 | |
| | | 6.0 | 400 | 400 | 400 | |

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

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## SWITCHING WAVEFORMS

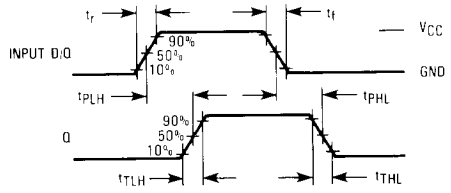



Figure 1

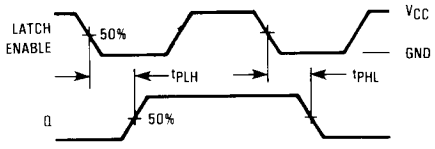



Figure 2

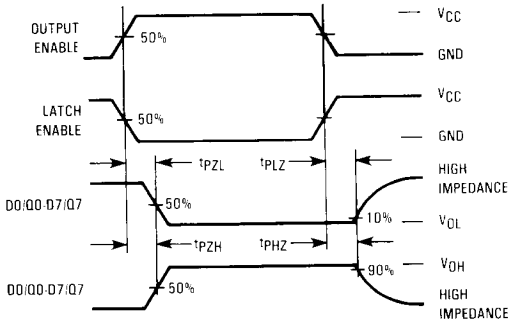



Figure 3

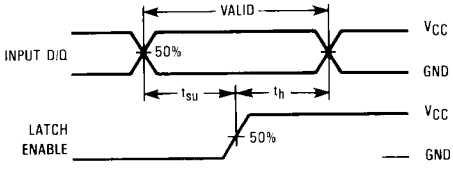
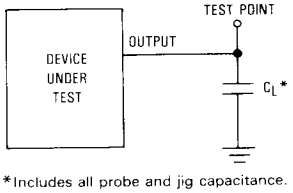
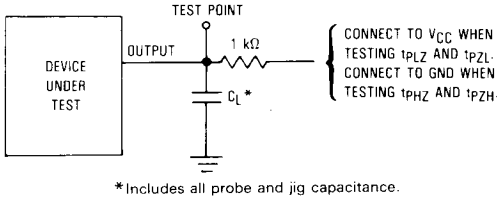



Figure 4




*Includes all probe and jig capacitance.

Figure 5. Test Circuit




*Includes all probe and jig capacitance.

Figure 6. Test Circuit

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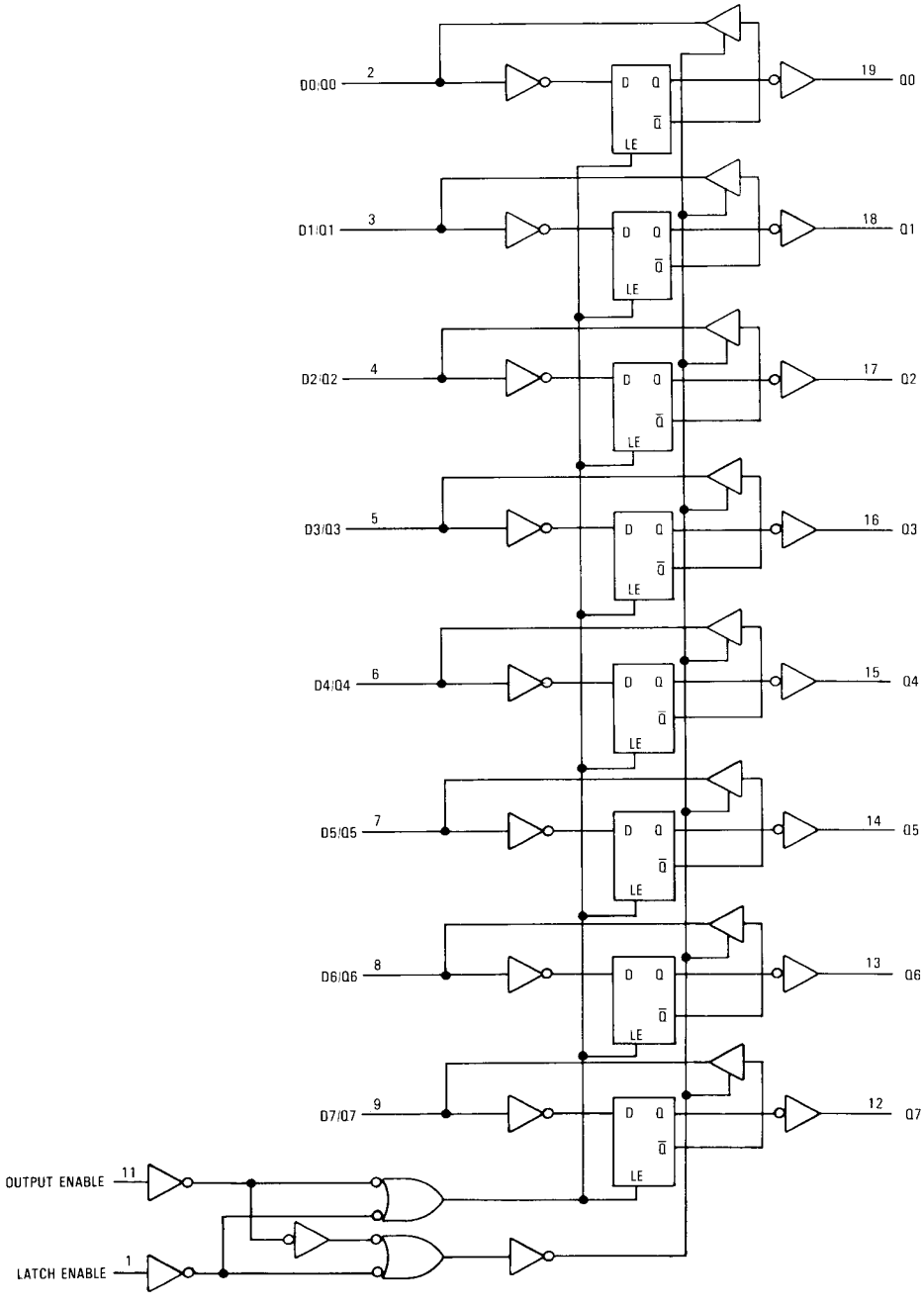
EXPANDED LOGIC DIAGRAM

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