048468

MC54/74HC9000

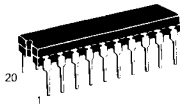
Product Preview

Programmable Timer

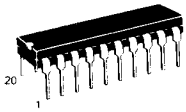
High-Performance Silicon-Gate CMOS

The MC54/74HC9000 is a precision programmable timer that, when used in conjunction with a 32 kHz to 20 MHz crystal, can provide time durations from 4.2 minutes to 100 ns. Using the on-chip oscillator function and external RC components, even longer time durations can be obtained. Both true and complementary outputs are available for use with the edge-sensitive oscillator control and count control. These control pins facilitate several timer and "one-shot" type configurations (see Application Information).

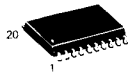
- Has On-Chip Crystal or RC Oscillator Capability; or may be Driven by External Frequency Source
- More Accurate than Monostable Multivibrators when used with a Crystal
- Low Power Consumption Characteristic of CMOS Devices
- Wide Operating Voltage Range: 2.5 to 6 Volts
- OUT and $\overline{OUT}$ Drive Capability: 10 LSTTL Loads
- High Noise Immunity Characteristics of CMOS Devices
- Very Low Power Consumption in Standby Mode
- Double Diode Protection on all Inputs
- Divide Range of 2 to 2^{24}
- Select Inputs (S0, S1, S2, S3, S4) Facilitate Programming and Incoming Inspection
- Mode Inputs (M0, M1, M2) for Functional Versatility
- Chip Complexity: 923 FETs or 231 Equivalent Gates



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



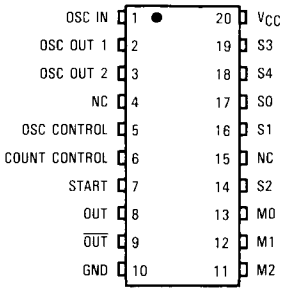
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

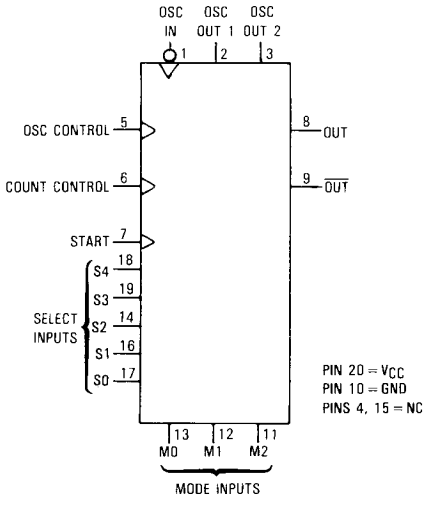
$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



NC = NO CONNECTION

LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	 260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.5*	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	Except OSC IN and START	V_{CC} = 4.5 V	0	500	
	(Figure 1)	V_{CC} = 6.0 V	0	400	
	Input Rise and Fall Time (OSC IN or START)		0	No Limit	

*The oscillator is guaranteed to function at 2.5 V minimum. However, parametrics are tested at 2.0 V by driving Pin 1 with an external clock source.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit 25°C to −55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage (OUT, $\overline{OUT}$)	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage (OUT, $\overline{OUT}$)	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Projected Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
f_{max}	Maximum Clock Frequency (Modes 1-7) (50% Duty Cycle) (Figures 1 and 2)	2.0 4.5 6.0	4.0 20 24	3.2 16 19	2.6 13 15	MHz
f_{max}	Maximum Clock Frequency (Mode 0) (50% Duty Cycle) (Figures 1 and 2)	2.0 4.5 6.0	2.0 10 11.8	1.6 8.0 9.4	1.3 6.7 7.9	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, OSC IN to OUT or $\overline{OUT}$ (One Stage Selected) (Figures 1 and 2)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, START to OUT or $\overline{OUT}$ (One Shot Mode) (Figures 3 and 2)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V_{CC} = 5.0 V TBD	pF

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Projected Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, S0-S4 or M0-M2 to START (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_d	Minimum Delay Time, START to OUT or $\overline{OUT}$ (Figure 3)	2.0 4.5 6.0	500 100 85	625 125 106	750 150 128	ns
t_b	Minimum Burst Time, Count Control (Figure 3)	2.0 4.5 6.0	500 100 85	625 125 106	750 150 128	ns
t_w	Minimum Pulse Width, START (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, OSC IN (Figure 1)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, OUT or $\overline{OUT}$ (One-Shot Mode) (Figure 3)	2.0 4.5 6.0	500 100 85	625 125 106	750 150 128	ns
t_w	Minimum Pulse Width, OUT or $\overline{OUT}$ (Delayed Multiple Pulse Mode) (Figure 3)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_r, t_f	Maximum Input Rise and Fall Times, Except OSC IN or START	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns
t_r, t_f	Maximum Input Rise and Fall Times, OSC IN or START (Figure 1)	—	No Limit			—

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

5

PIN DESCRIPTIONS

OSC IN, OSC OUT 1, OSC OUT 2 (Pins 1, 2, 3)

These pins, used in conjunction with external components, form an on-chip reference oscillator. The frequency of this oscillator and the number of counters selected determines the amount of time-out desired (see Figures 7 and 8). An external generator may be used instead of the internal oscillator. In this case, the signal should swing from ground to V_{CC} and should be fed into OSC IN. OSC OUT 1 and OSC OUT 2 must be left floating (see Figure 9). With the crystal oscillator configuration shown in Figure 7, OSC OUT 2 must be left open-circuited.

OSC CONTROL (Pin 5)

This pin is used to enable or disable the oscillator. A low-to-high transition on this pin resets all counters and shuts down the oscillator. This puts the device into a low-power standby condition.

COUNT CONTROL (Pin 6)

A low-to-high transition on this pin also resets all counters. The oscillator continues to run, but the counters do not increment. This condition eliminates oscillator start-up delay time.

START (Pin 7)

A low-to-high transition on this pin causes the oscillator to start up, if previously disabled, and timing begins. The START input is Schmitt-triggered to allow for slow rise and fall input pulses. When using only one or two stages of delay, it is recommended that an external time base, synchronized with the start pulse, be used. With no synchronization, a start pulse occurring when the clock is high produces a different initial delay than when the start pulse occurs when the clock is low. This effect causes less error as more delay stages are selected.

M0, M1, M2 (Pins 13, 12, 11)

Mode inputs. These pins determine the timer's mode of operation (see Table 1).

S0, S1, S2, S3, S4 (Pins 17, 16, 14, 19, 18)

Select inputs. These pins select the exact divide ratio desired (see Table 2).

OUT (Pin 8)

This pin is the output of the timer. OUT can be fed back to either OSC CONTROL or COUNT CONTROL to inhibit counting.

$\overline{\text{OUT}}$ (Pin 9)

$\overline{\text{OUT}}$ is the complement of OUT. $\overline{\text{OUT}}$ can also be fed back to OSC CONTROL or COUNT CONTROL to inhibit counting.

NC (Pins 4, 15)

No connect pins. These pins are not connected internally.

Table 1. Output Mode Selection Table

Mode	Mode Inputs			Output Pulse Description	Figure
	M2	M1	M0		
0	0	0	0	Delayed Pulse ($t_w = 1/2f$)	11, 13
1	0	0	1	Delayed Pulse ($t_w = 2/f$)	11, 13
2	0	1	0	Delayed Pulse ($t_w = 8/f$)	11, 13
3	0	1	1	Monostable Multivibrator	10
4	1	0	0	Delayed Burst Pulse ($t_w = 1/2f$) $t_{delay} = t_{burst}$	14
5	1	0	1	Delayed Burst Pulse ($t_w = 2/f$) $t_{delay} = t_{burst}$	14
6	1	1	0	Delayed Burst Pulse ($t_w = 8/f$) $t_{delay} = t_{burst}$	14
7	1	1	1	Programmable Counter or Test Mode (50% Output Duty Cycle)	12, 15, 17

5

Table 2. Select Divide Range

Select Inputs					Number of Counter Stages Selected, N ($\div 2^N$)
S4	S3	S2	S1	S0	
0	0	0	0	0	1
0	0	0	0	1	2
0	0	0	1	0	3
0	0	0	1	1	4
0	0	1	0	0	5
0	0	1	0	1	6
0	0	1	1	0	7
0	0	1	1	1	8
0	1	0	0	0	9
0	1	0	0	1	10
0	1	0	1	0	11
0	1	0	1	1	12
0	1	1	0	0	13
0	1	1	0	1	14
0	1	1	1	0	15
0	1	1	1	1	16

Select Inputs					Number of Counter Stages Selected, N ($\div 2^N$)
S4	S3	S2	S1	S0	
1	0	0	0	0	17
1	0	0	0	1	18
1	0	0	1	0	19
1	0	0	1	1	20
1	0	1	0	0	21
1	0	1	0	1	22
1	0	1	1	0	23
1	0	1	1	1	24
1	1	0	0	0	1*
1	1	0	0	1	2*
1	1	0	1	0	3*
1	1	0	1	1	4*
1	1	1	0	0	5*
1	1	1	0	1	6*
1	1	1	1	0	7*
1	1	1	1	1	8*

*Configured internally such that the 24 stage counter is parallel clocked as three 8-bit counters. This allows for shorter incoming inspection testing times.

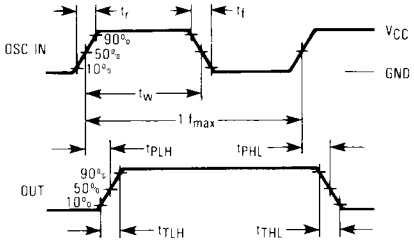


Figure 1. Switching Waveforms

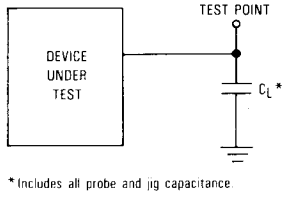


Figure 2. Test Circuit

5

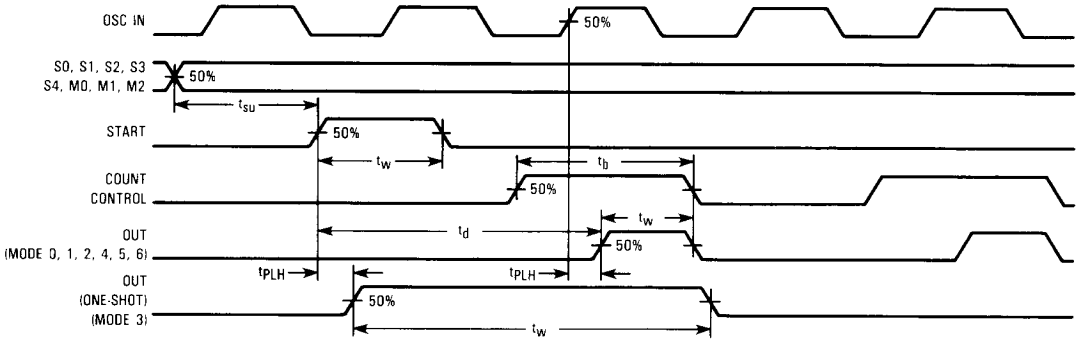
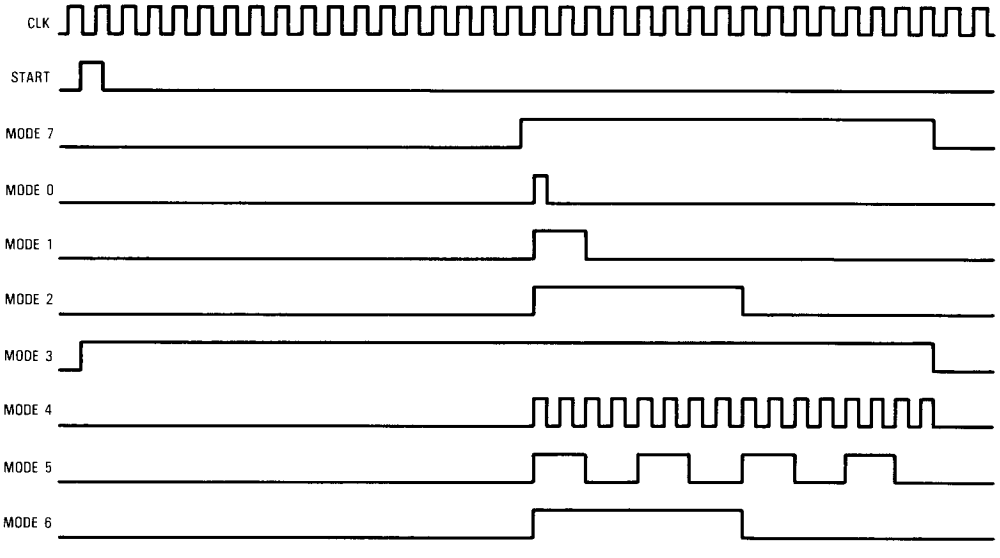


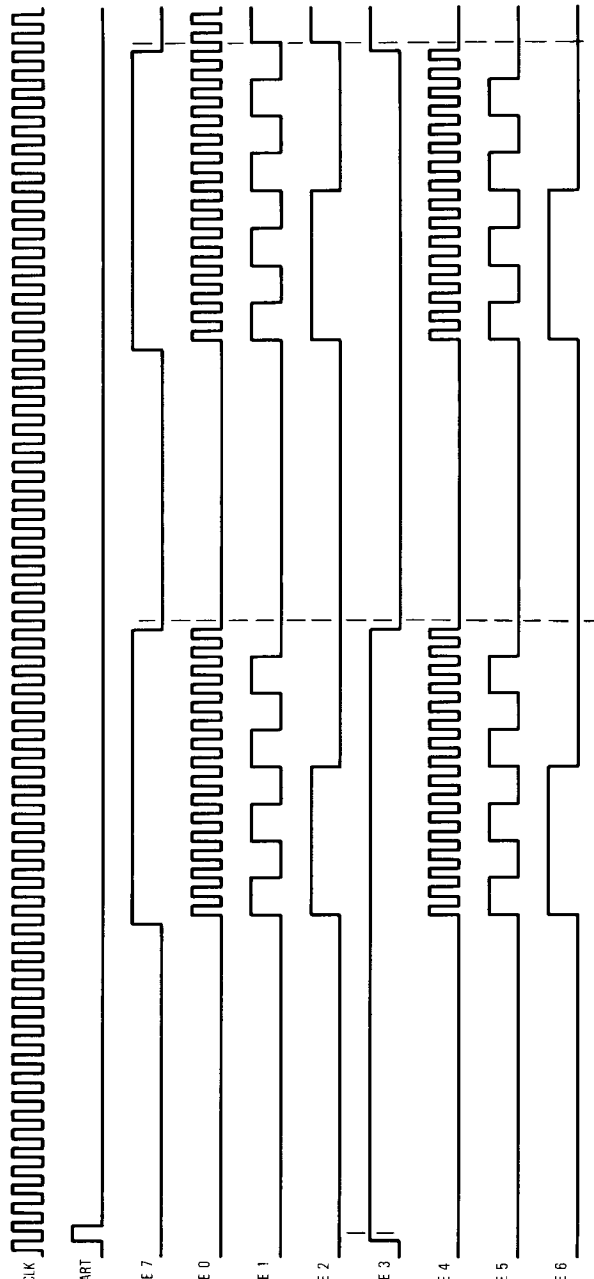
Figure 3. Functional Timing Diagram



NOTE: Five stages of delay counter selected (S4, S3, S2, S1, S0 = 00100).

Figure 4. Timing Diagram Using Feedback

5



NOTE: Five stages of delay counter selected (S4, S3, S2, S1, S0 = 00100).

Figure 5. Timing Diagram Using No Feedback

5

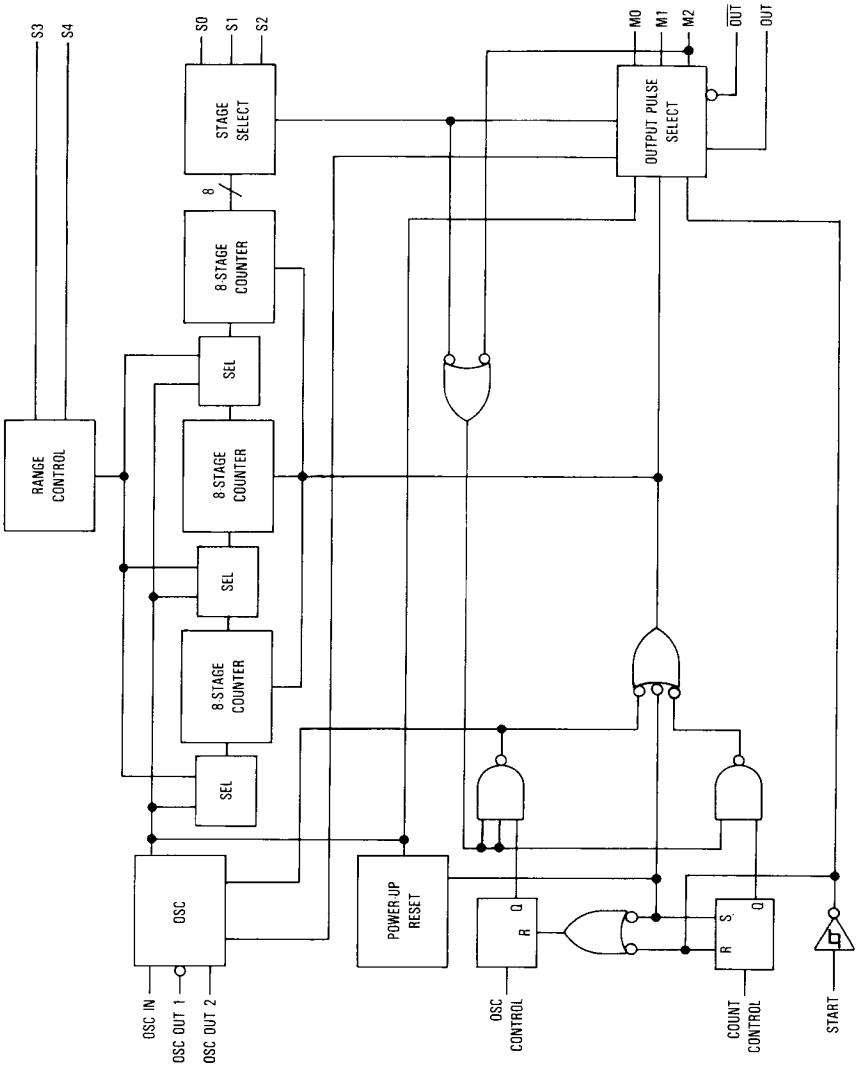


Figure 6. Block Diagram

5

OSCILLATOR DESIGN INFORMATION

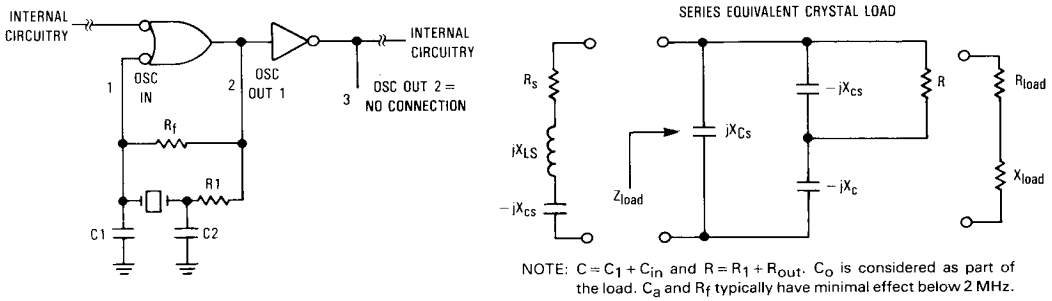
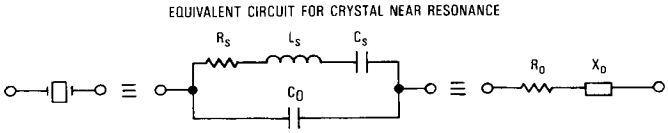
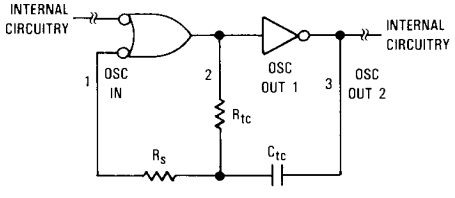


Figure 7. Pierce Oscillator





$10\ R_{tc} > R_S > 2\ R_{tc}$

$400\ Hz \leq f \leq 400\ kHz$:

$$f = \frac{1}{2.3\ R_{tc} C_{tc}}$$ (f in Hz, R_{tc} in ohms, C_{tc} in farads)

The formula may vary for other frequencies.

Figure 8. RC Oscillator

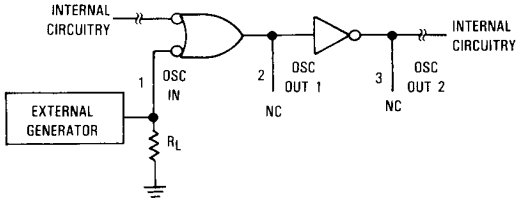


Figure 9. External Generator

DESIGN PROCEDURE

The following procedure applies for oscillators operating below 2 MHz where Z is a resistor R_1. Above 2 MHz, additional impedance elements may be considered: C_{out} and C_a of the amp, feedback resistor R_f, and amplifier phase shift error from 180°.

Step 1: Calculate the equivalent series circuit of the crystal at the frequency of oscillation.

$$Z_e = \frac{-jX_{CO}(R_S + jX_{LS} - jX_{CS})}{-jX_{CO} + R_S + jX_{LS} - jX_{CS}} = R_e + jX_e$$

Reactance jX_e should be positive, indicating that the crystal is operating as an inductive reactance at the oscillation frequency. The maximum R_S for the crystal should be used in the equation.

Step 2: Determine β, the attenuation, of the feedback network. For a closed loop gain of 2, $A_V\beta = 2$, $\beta = 2/A_V$ where A_V is the gain of the HC9000 amplifier.

Step 3: Determine the manufacturer's loading capacitance. For example: a manufacturer may specify an external load capacitance of 32 pF at the required frequency.

Step 4: Determine the required Q of the system, and calculate R_{load}. For example: a manufacturer specifies a crystal Q of 100,000. The desired in-circuit Q is set at 20% below crystal Q or 80,000. Then $R_{load} = (2\pi f_o L_S/Q) - R_S$ where L_S and R_S are crystal parameters.

Step 5: Simultaneously solve, using a computer, equations 1, 2, and 3.

$$\beta = \frac{X_c * X_{c2}}{R * R_e + X_{c2}(X_e - X_c)} \text{ (with feedback phase shift = 180°)} \quad (1)$$

$$X_e = X_{c2} + X_c + \frac{R_e X_{c2}}{R} = X_{cload} \text{ (where the loading capacitor is an external load not including } C_O) \quad (2)$$

$$R_{load} = \frac{RX_{CO}X_{c2}[(X_c + X_{c2})(X_c + X_{CO}) - X_c(X_c + X_{CO} + X_{c2})]}{X_{c2}^2(X_c + X_{CO})^2 + R^2(X_c + X_{CO} + X_{c2})^2} \quad (3)$$

Here $R = R_{out} + R_1$. R_{out} is amp output resistance, R_1 is Z. The C corresponding to X_c is given by $C = C_1 + C_{in}$.

Alternately, pick a value for R_1 (i.e. let $R_1 = R_S$). Solve Equations 1 and 2 for C_1 and C_2. Use Equation 3 and the fact $Q = 2\pi f_o L_S/(R_S + R_{load})$ to find in-circuit Q. If Q is not satisfactory pick another value for R_1 and repeat the procedure.

APPLICATIONS INFORMATION
APPLICATIONS WITH FREE-RUN OSCILLATOR (NO OSCILLATOR START-UP DELAY)

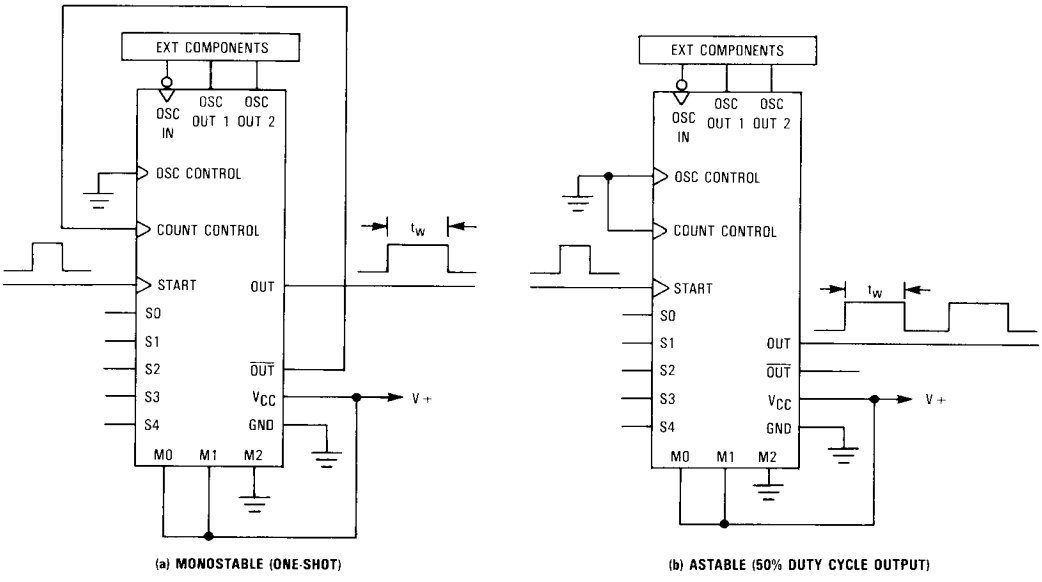
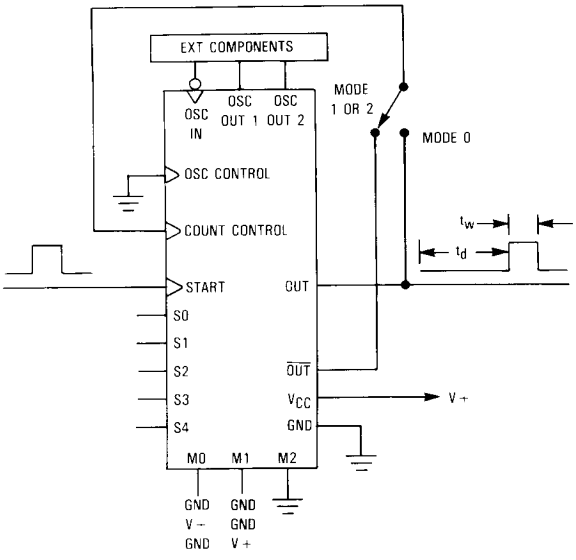
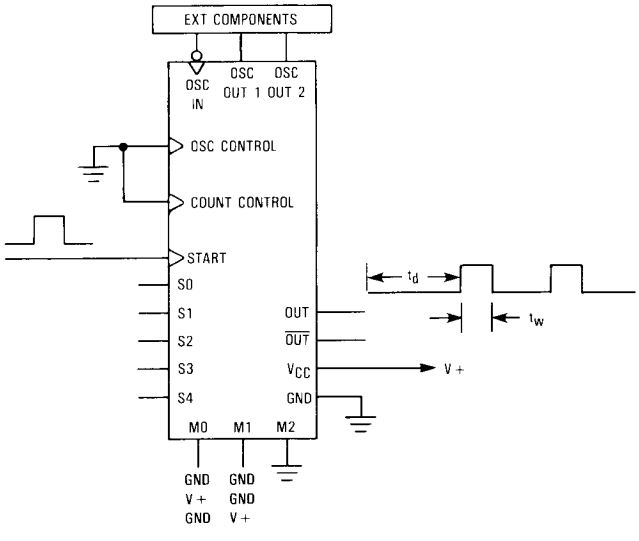


Figure 10. Multivibrator Configurations

5



(a) DELAYED SINGLE PULSE



(b) DELAYED MULTIPLE PULSE

Figure 11. Delayed Pulse Configurations

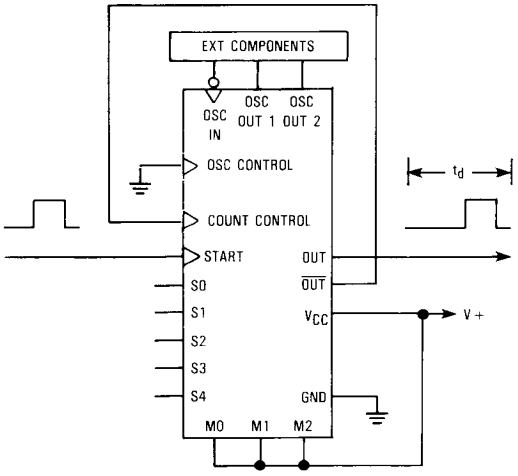
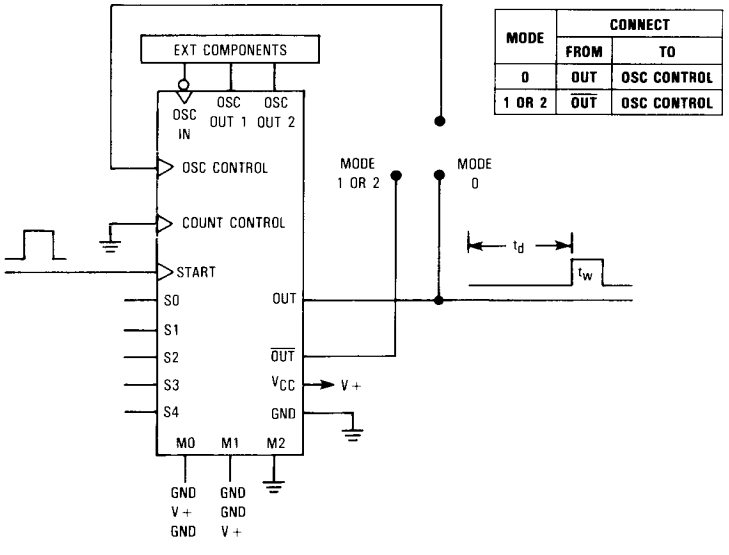


Figure 12. Programmable Timer

LOW STANDBY POWER APPLICATIONS (OSCILLATOR IS STOPPED WHEN IN STANDBY)



MODE	CONNECT	
	FROM	TO
0	OUT	OSC CONTROL
1 OR 2	$\overline{OUT}$	OSC CONTROL

Figure 13. Delayed Single-Pulse Configuration

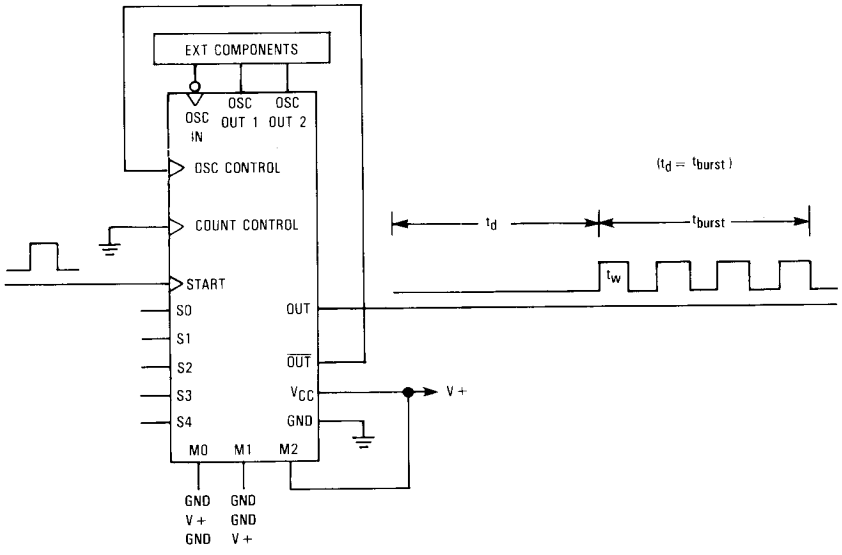


Figure 14. Burst Delayed-Pulse Configuration

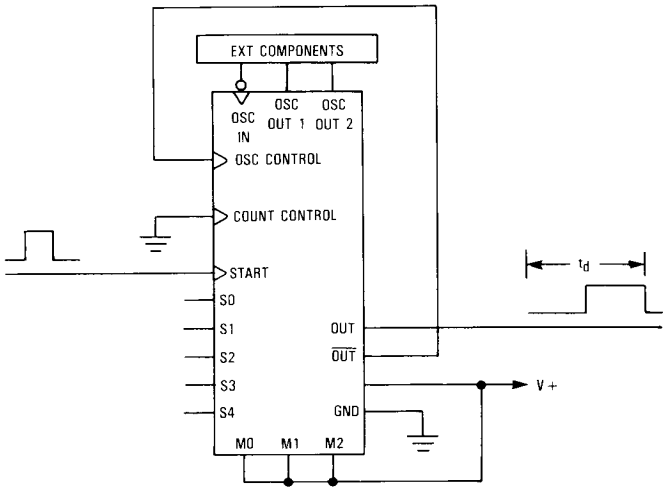


Figure 15. Programmable Timer

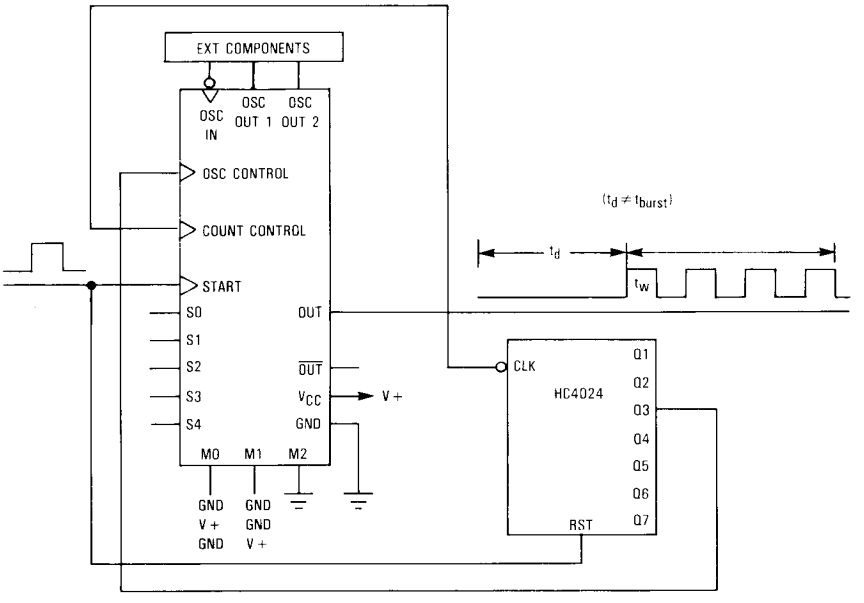


Figure 16. Delayed Multiple Pulse Configuration (4-Pulse Configured)

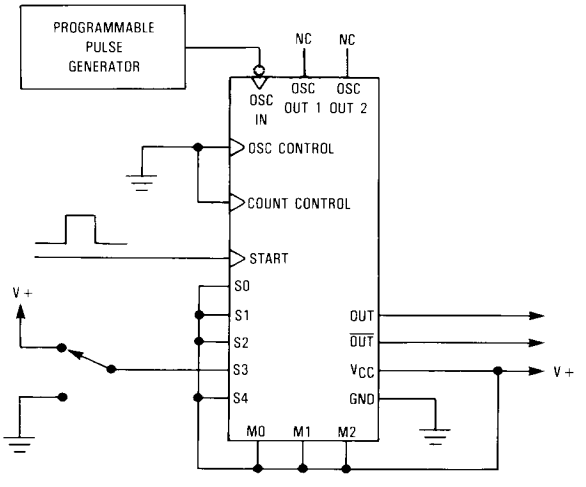


Figure 17. Test Mode (2^8 Divider Configuration)

NOTE

TEST MODE

Setting M0, M1, M2 to a logic level 1 selects the programmable counter option. Setting S3 and S4 to a logic level 1 divides the 2^{24} stage counter into three 8-stage counters. These three 8-stage counters are clocked in parallel. Setting S0, S1, S2, to a logic level 1 sets the counters to divide by 2^8 (256). Applying a start pulse, and then clocking OSC IN 255 times sets all flip flop stages and OUT to a high level. After setting OUT to a high level, S3 is set to a logic level 0 and the counters revert back to 2^{24} operation. Clocking OSC IN one more time causes a 0 to ripple through the counters and OUT goes from a high to a low level (see Figure 17). This method of exercising the delay counter is faster than clocking in 2^{24} clock pulses.