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Product Preview

Nine-Wide Buffers with Open-Drain Outputs

High-Performance Silicon-Gate CMOS

MC54/74HC9134
MC54/74HC9135

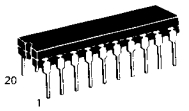
The MC54/74HC9134 consists of nine inverting buffers and the MC54/74HC9135 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

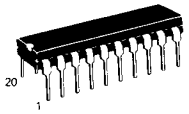
Each of the HC9134 and HC9135 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

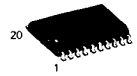
- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 45 FETs or 11.25 Equivalent Gates (HC9134)
  63 FETs or 15.75 Equivalent Gates (HC9135)



J SUFFIX
CERAMIC
CASE 732



N SUFFIX
PLASTIC
CASE 738



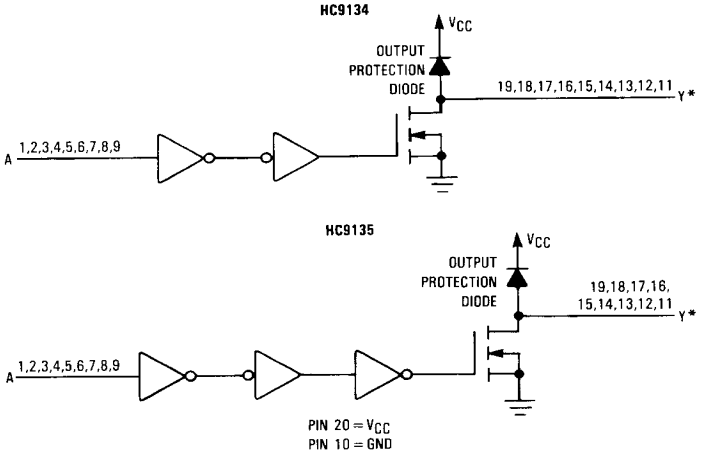
DW SUFFIX
SOIC
CASE 751D

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic
MC74HCXXXXDW	SOIC

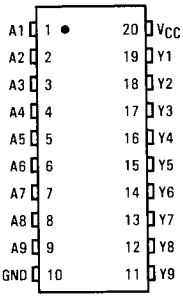
$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

LOGIC DIAGRAMS



*Denotes open-drain outputs.

PIN ASSIGNMENT



FUNCTION TABLE

A Input	Y Outputs	
	HC9134	HC9135
L	Z	L
H	L	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC} +1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1$ V)	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$ (Figure 2 for $V_{out} = V_{CC} - 0.1$ V)	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\ \mu A$	6.0	2	20	40	μA
I_{OZ}	Maximum Output Leakage Current	$A = V_{IH}$ or V_{IL} $V_{out} = V_{CC}$ or GND	6.0	±0.5	±5.0	±10.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter		V_{CC} V	Projected Limit 25°C to −55°C	Projected Limit ≤85°C	Projected Limit ≤125°C	Unit
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9134	2.0	115	145	175	ns
			4.5	23	29	35	
			6.0	20	25	30	
		HC9135	2.0	120	150	180	
			4.5	24	30	36	
			6.0	20	26	31	
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)		2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
C_{in}	Maximum Input Capacitance		—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)		—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, V_{CC} = 5.0 V 15	pF

SWITCHING WAVEFORMS

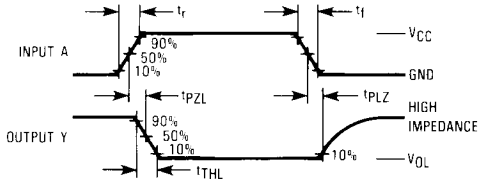


Figure 1A. HC9134

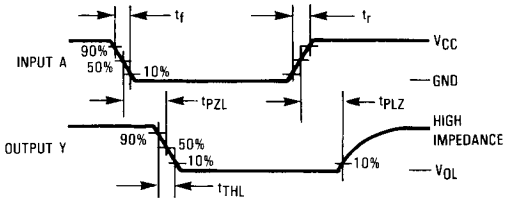
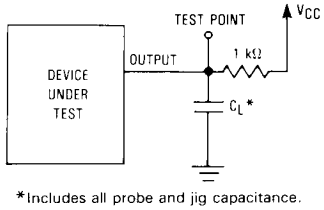
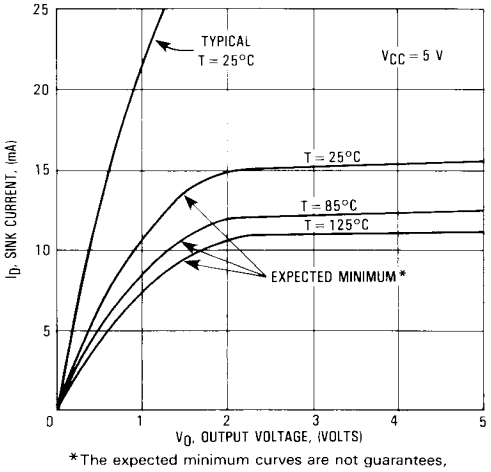


Figure 1B. HC9135



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics