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Product Preview

Nine-Wide Buffers with Open-Drain Outputs
High-Performance Silicon-Gate CMOS

The MC54/74HC9134 consists of nine inverting buffers and the MC54/74HC9135 consists of nine noninverting buffers. Both devices have inputs that are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

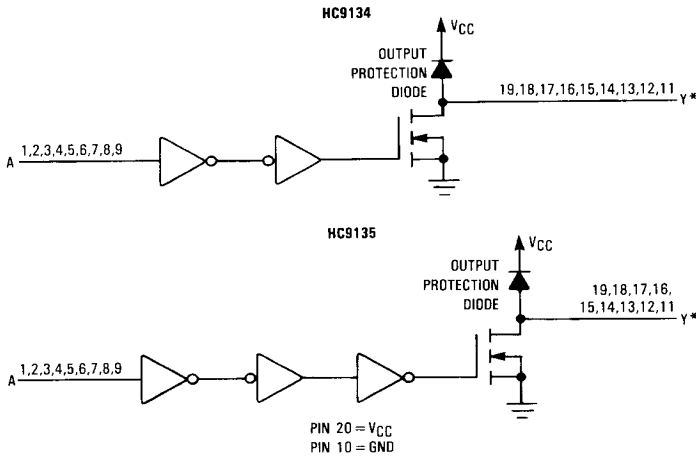
These devices find primary use as interfaces between microprocessors and peripheral hardware such as keyboards, memory arrays, displays, etc. They are especially useful when 8 bits of data are needed and an extra bit is required for parity, control, or handshake.

Each of the HC9134 and HC9135 outputs are fabricated using a high-performance MOS N-channel transistor. Therefore, with a suitable pullup resistor, these gates can be used in wired-AND applications. Using the output characteristic curves given in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

Using 9-Wide buffers, instead of standard hex buffers, decreases component count and increases system reliability.

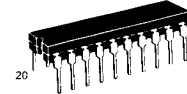
- Output Drive Capability: 10 LSTTL Loads — with Suitable Pullup Resistor
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 45 FETs or 11.25 Equivalent Gates (HC9134)
 63 FETs or 15.75 Equivalent Gates (HC9135)

LOGIC DIAGRAMS

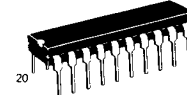


*Denotes open-drain outputs.

MC54/74HC9134
MC54/74HC9135



J SUFFIX
 CERAMIC
 CASE 732



N SUFFIX
 PLASTIC
 CASE 738



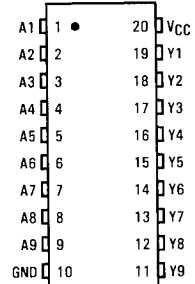
DW SUFFIX
 SOIC
 CASE 751D

ORDERING INFORMATION

- | | |
|--------------|---------|
| MC74HCXXXXN | Plastic |
| MC54HCXXXXJ | Ceramic |
| MC74HCXXXXDW | SOIC |

T_A = -55° to 125°C for all packages.
 Dimensions in Chapter 7.

PIN ASSIGNMENT



FUNCTION TABLE

A Input	Y Outputs	
	HC9134	HC9135
L	Z	L
H	L	Z

Z = high impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 †Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
 Ceramic DIP: - 10 mW/°C from 100° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4 subject listing on page 4-2.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to - 55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA (Figure 2 for V _{out} = V _{CC} - 0.1 V)	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA (Figure 2 for V _{out} = V _{CC} - 0.1 V)	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	4.5	0.26	0.33	0.40	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	2	20	40	μA
I _{OZ}	Maximum Output Leakage Current	A = V _{IH} or V _{IL} V _{out} = V _{CC} or GND	6.0	± 0.5	± 5.0	± 10.0	μA

NOTE: Information on typical parametric values can be found in Chapter 4 subject listing on page 4-2.

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AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	VCC V	Projected Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t_{PLZ} , t_{PZL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	HC9134 2.0 4.5 6.0	115 23 20	145 29 25	175 35 30	ns
		HC9135 2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 4 subject listing on page 4-2.
- Information on typical parametric values can be found in Chapter 4.

CPD	Power Dissipation Capacitance (Per Buffer) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4 subject listing on page 4-2.	Typical @ 25°C, VCC = 5.0 V	pF
		15	

SWITCHING WAVEFORMS

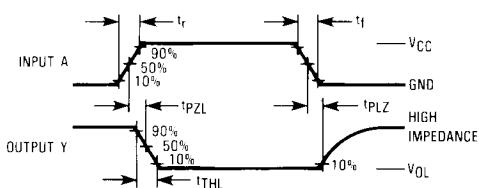


Figure 1A. HC9134

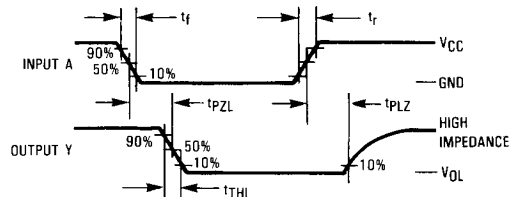
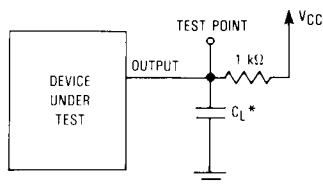
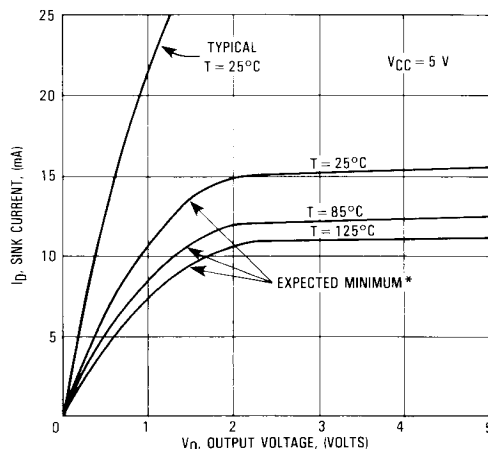


Figure 1B. HC9135



*Includes all probe and jig capacitance.

Figure 2. Test Circuit



*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics

MOTOROLA HIGH-SPEED CMOS LOGIC DATA