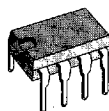


MULTIFUNCTION VERY LOW DROP VOLTAGE REGULATOR

ADVANCE DATA

- OPERATING DC SUPPLY VOLTAGE RANGE 5V - 28V
- TRANSIENT SUPPLY VOLTAGE UP TO 40V
- EXTREMELY LOW QUIESCENT CURRENT IN STANDBY MODE
- HIGH PRECISION STANDBY OUTPUT VOLTAGE $5V \pm 1\%$
- OUTPUT CURRENT CAPABILITY UP TO 100mA
- VERY LOW DROPOUT VOLTAGE LESS THAN 0.4V
- RESET CIRCUIT SENSING THE OUTPUT VOLTAGE
- PROGRAMMABLE RESET PULSE DELAY WITH EXTERNAL CAPACITOR
- VOLTAGE SENSE COMPARATOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS


Minidip

SO-8
ORDERING NUMBERS:

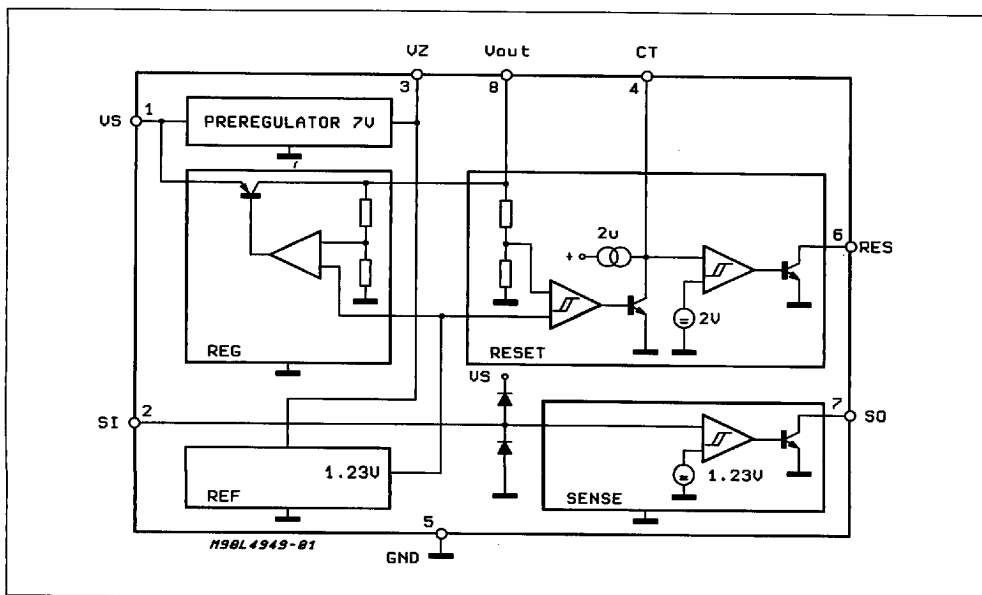
L4949N

L4949DN

DESCRIPTION

The L4949 is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as power-on reset and input voltage sense. It is designed for supplying the micro-computer controlled systems especially in automotive applications.

BLOCK DIAGRAM



February 1992

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This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
VSDC	DC Operating Supply Voltage	28	V
VSTR	Transient Supply Voltage (T < 1s)	40	V
IO	Output Current	Internally Limited	
VO	Output Voltage	20	V
ISI	Sense Input Current	±1	mA
IEN	Enable Input Current	-1	mA
VEN	Enable Input Voltage	VS	
VRES, VSO	Output Voltages	20	V
IRES, ISO	Output Currents	5	mA
VZ	Preregulator Output Voltage	7	V
Iz	Preregulator Output Current	5	mA
TJ	Junction Temperature	-40 to +150	°C
Tslg	Storage Temperature Range	-55 to +150	°C

Note: The circuit is ESD protected according to MIL-STD-883C

THERMAL DATA

Symbol	Description	Minidip	SO-8	Unit
Rth j-amb	Thermal Resistance Junction-ambient	100	200	°C/W
TJSD	Thermal Shutdown Junction temperature	165		°C

ELECTRICAL CHARACTERISTICS (VS = 14V; -40°C < TJ < 125°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VO	Output Voltage	TJ = 25°C; IO = 1mA	4.95	5	5.05	V
VO	Output Voltage	6V < VIN < 28V, 1mA < IO < 50mA	4.90	5	5.10	V
VO	Output Voltage	VIN = 35V; T < 1s 1mA < IO < 50mA			5.50	V
VOP	Dropout Voltage	IO = 10mA		0.1	0.25	V
		IO = 50mA		0.2	0.4	V
		IO = 100mA		0.3	0.5	V
VIO	Input to Output Voltage Difference in Undervoltage Condition	VIN = 4V, IO = 35mA			0.4	V
VOL	Line Regulation	6V < VIN < 28V; IO = 1mA			20	mV
VOLO	Load Regulation	1mA < IO < 100mA			30	mV
IUN	Current Limit	VO = 4.5V VO = 0V (note 1)	105	200 50	400	mA mA
Iose	Quiescent Current	IO = 0.3mA; TJ < 100°C		150	260	µA
IQ	Quiescent Current	IO = 100mA			5	mA

RESET

VRT	Reset Threshold Voltage			VO-0.5V		V
VRTH	Reset Threshold		50	100	200	mV

Note 1: Foldback characteristic

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{RD}	Reset Pulse Delay	$C_T = 100\text{nF}$; $T_R \geq 100\mu\text{s}$	55	100	180	ms
t_{RR}	Reset Reaction Time	$C_T = 100\text{nF}$		5	30	μs
V_{RL}	Reset Output Low Voltage	$R_{RES} = 10\text{K}\Omega$ to V_O ; $V_S \geq 3\text{V}$			0.4	V
I_{RH}	Reset Output High Leakage Current	$V_{RES} = 5\text{V}$			1	μA
V_{CTH}	Delay Comparator Threshold			2		V
$V_{CTH,hy}$	Delay Comparator Threshold Hysteresis			100		mV

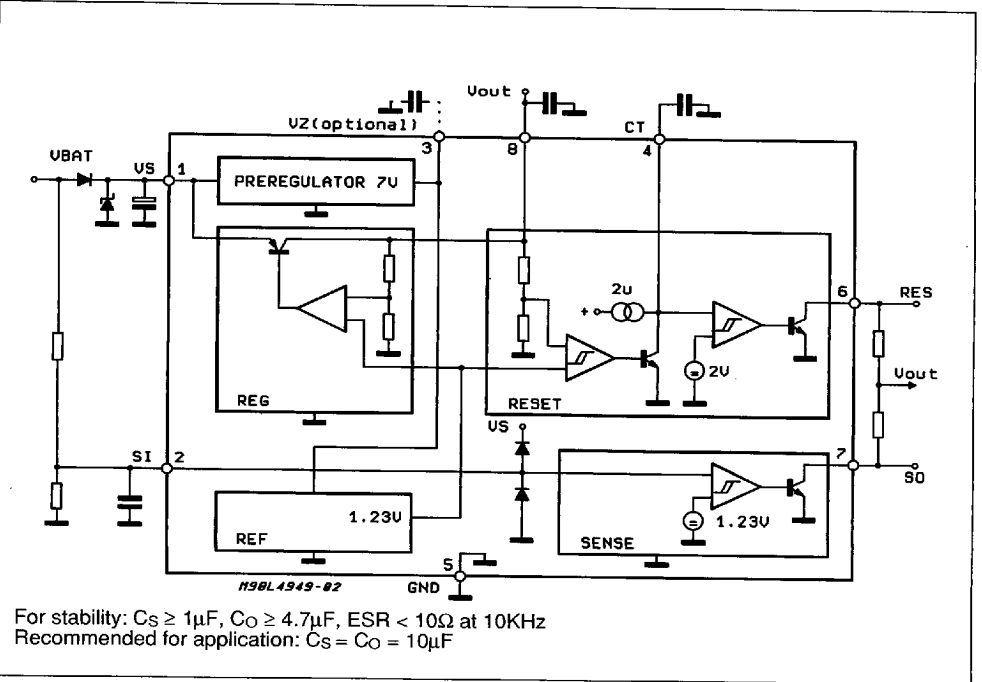
SENSE

V_{st}	Sense Low Threshold		1.16	1.23	1.35	V
V_{sth}	Sense Threshold Hysteresis		20	100	200	mV
V_{SL}	Sense Output Low Voltage	$V_{SI} \leq 1.16\text{V}$; $V_S \geq 3\text{V}$ $R_{SO} = 10\text{K}\Omega$ to V_O			0.4	V
I_{SH}	Sense Output Leakage	$V_{SO} = 5\text{V}$; $V_{SI} \geq 1.5\text{V}$			1	μA
I_{SI}	Sense Input Current		-1	0.1	1	μA

PREREGULATOR

V_Z	Preregulator Output Voltage	$I_Z = 10\mu\text{A}$		7		V
I_Z	Preregulator Output Current				10	μA

APPLICATION CIRCUIT



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APPLICATION INFORMATION

Supply Voltage Transient

High supply voltage transients can cause a reset output signal disturbance.

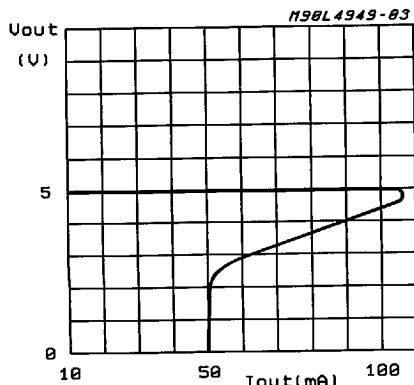
For supply voltages greater than 8V the circuit shows a high immunity of the reset output against supply transients of more than 100V/μs.

For supply voltages less than 8V supply transients of more than 0.4V/μs can cause a reset signal disturbance.

To improve the transient behaviour for supply voltages less than 8V a capacitor at pin 3 can be used.

A capacitor at pin 3 ($C_3 \leq 1\mu\text{F}$) reduces also the output noise.

Figure 1: Foldback Characteristic of V_O



FUNCTIONAL DESCRIPTION

The L4949 is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

Voltage Regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 100mA is obtained. The dropout operation of the standby regulator is maintained down to 3V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35V. With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in Fig. 2.

The current consumption of the device (quiescent current) is less than 200μA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled, the quiescent current as a function of the supply input voltage is shown in Fig. 3.

Preregulator

To improve the transient immunity a preregulator stabilized the internal supply voltage to 7V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small ($\leq 10\mu\text{A}$). This output may be used as an option when a better transient behaviour for supply voltages less than 8V is required (see also application note). In this case a capacitor (100nF - 1μF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Figure 2: Output Voltage vs. Input Voltage

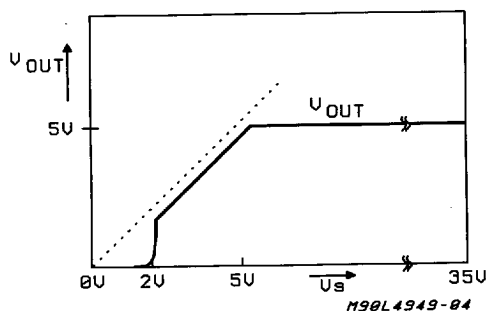
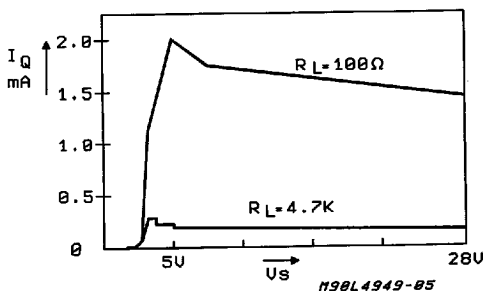


Figure 3: Quiescent Current vs. Supply Voltage



Reset Circuit

The block circuit diagram of the reset circuit is shown in Fig. 4. The reset circuit supervises the output voltage. The reset threshold of 4.5V is defined with the internal reference voltage and standby output divider.

The reset pulse delay time t_{RD} , is defined with the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T .

The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops

below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time. The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50μs.

The typical reset output waveforms are shown in Fig. 5.

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application. It can be used to supervise the input voltage either before or after the protection diode and to give additional informations to the microprocessor like low voltage warnings.

Figure 4

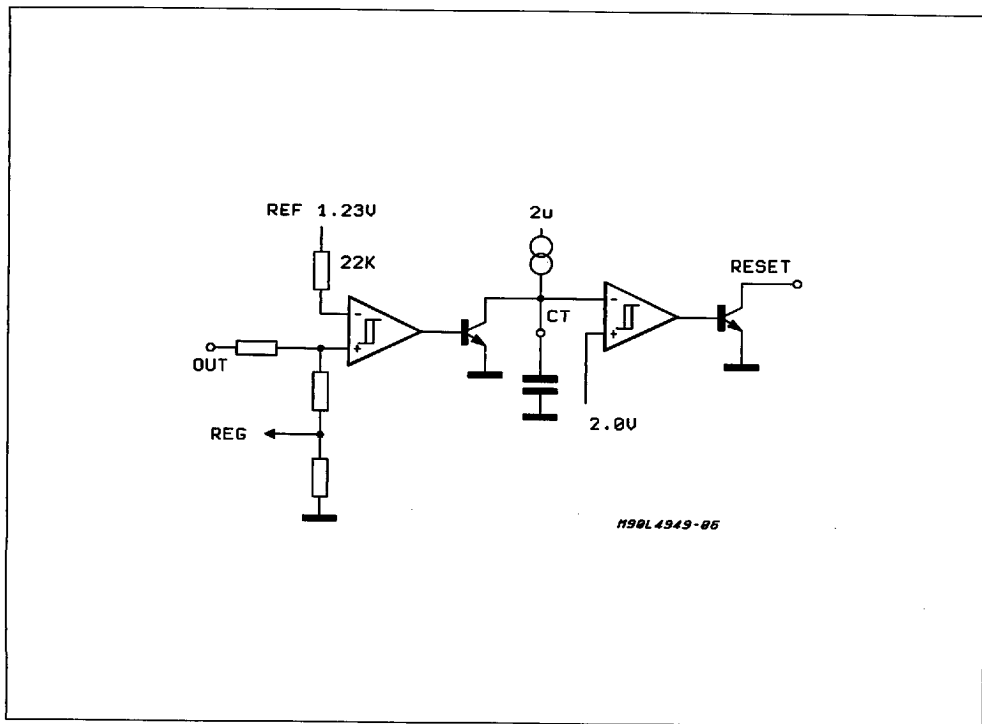


Figure 5

