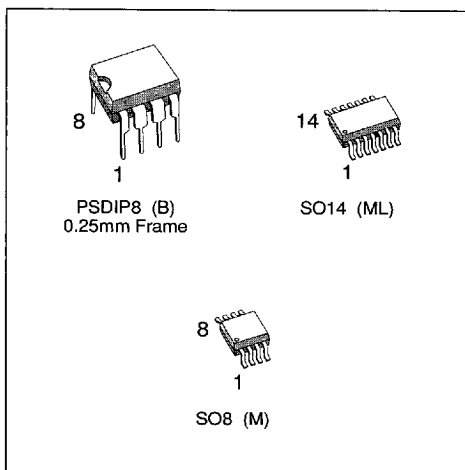


SERIAL ACCESS CMOS 16K (2048 x 8) EEPROMs

ABBREVIATED DATA

- MINIMUM 1 MILLION ERASE/WRITE CYCLES, with OVER 10 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
 - 3V to 5.5V for ST24x16 versions
 - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I²C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



DESCRIPTION

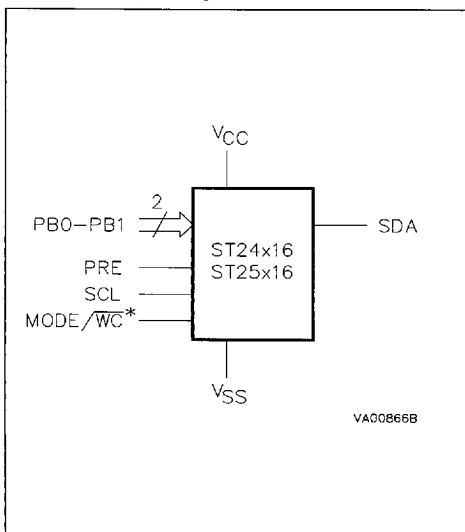
This specification covers a range of 16K bits I²C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured

Figure 1. Logic Diagram

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
W	Write Control (W version)
V _{CC}	Supply Voltage
V _{SS}	Ground



Note: WC signal is only available for ST24/25W16 products.

October 1993

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This is an abbreviated version of the complete document. The full document is available separately.

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Figure 2A. DIP Pin Connections

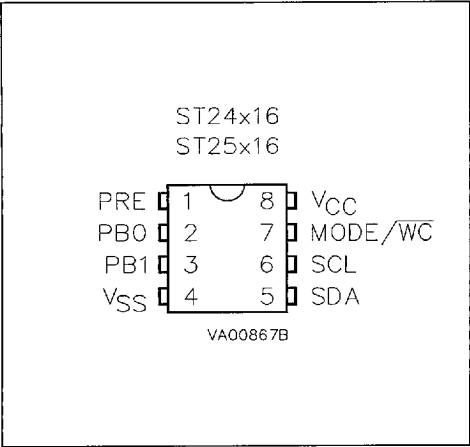
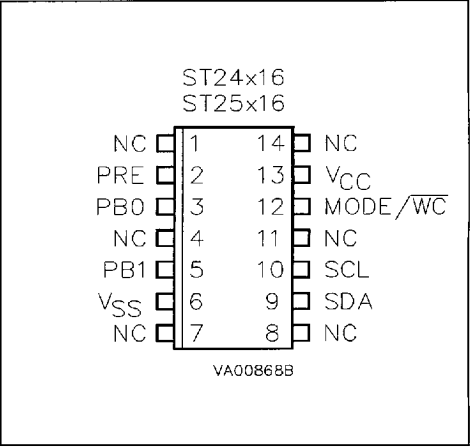
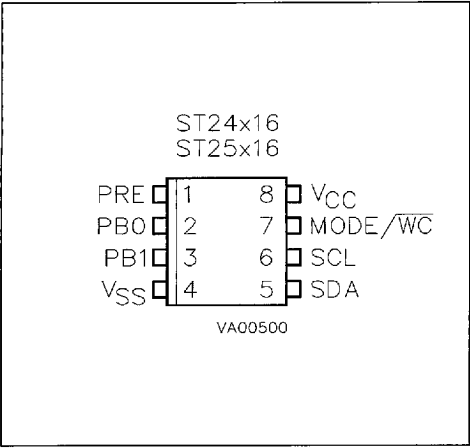


Figure 2B. SO14 Pin Connections



Warning: NC = No Connection

Figure 2C. SO8 Pin Connections



DESCRIPTION (cont'd)

in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of more than one million erase/write cycles with a data retention of over 10 years.

The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I²C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I²C bus definition. The memories behave as slave devices in the I²C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.