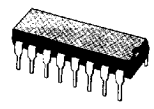
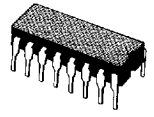
BCD TO 7 SEGMENT LATCH/DECODER DRIVER

- HIGH SPEED
  t_{PD} = 28 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- HIGH SOURCE CURRENT
  $|I_{OH}|$ = 20 mA (MIN.)
- BALANCED PROPAGATION DELAYS
  $t_{PLH} = t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH 4511B



B1R
(Plastic Package)



F1R
(Ceramic Package)

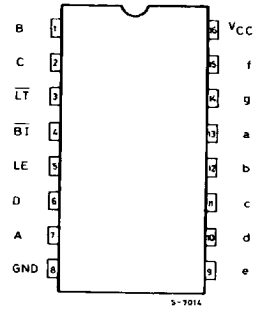
M1R
(Micro Package)

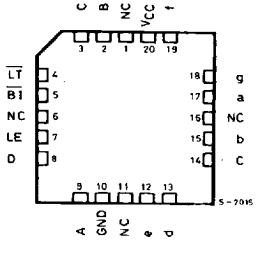
C1R
(Chip Carrier)

ORDER CODES :

M54HC4011F1R M74HC4011M1R
M74HC4011B1R M74HC4011C1R

PIN CONNECTIONS (top view)





NC =
No Internal
Connection

DESCRIPTION

The M54/74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C^2MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

The segment output driver, which is CMOS fabricated in silicon gate C^2MOS technology, has large I_{OH} capability which enables common cathode Leds to be directly driven.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L".

These functions operate regardless of other inputs and are used to test the display.

Input BI is used to pulse-modulate the brightness of the display.

When an error input code (over 10) is applied to the BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

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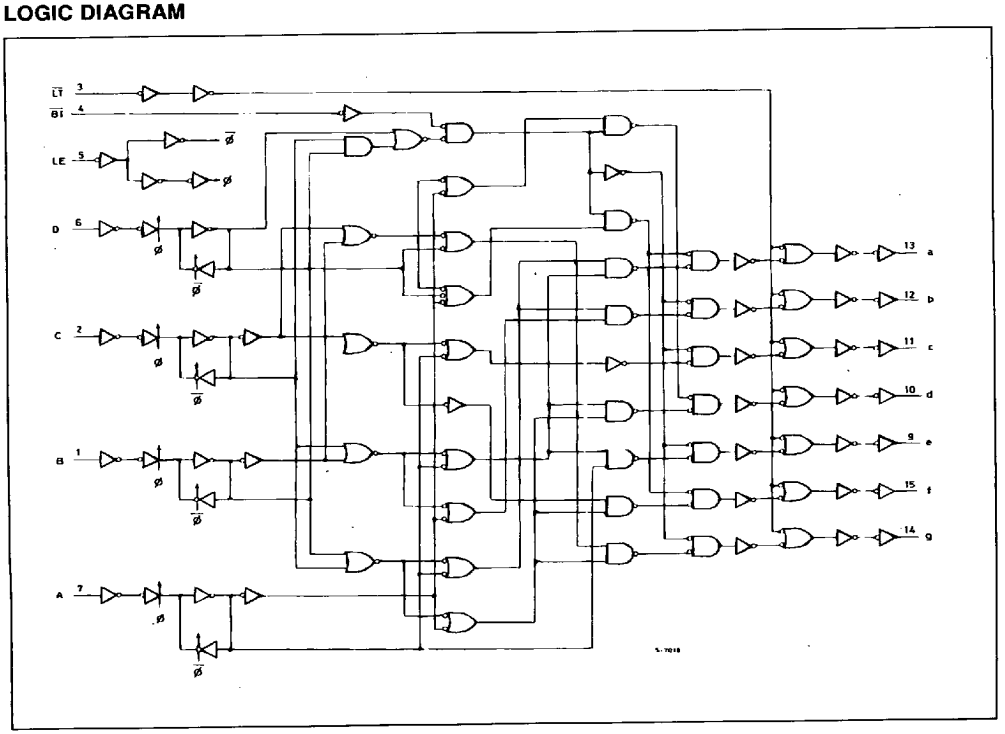
TRUTH TABLE

INPUTS							OUTPUTD							DISPLAY MODE
$\overline{LE}$	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	L	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

X: Don't Care

LOGIC DIAGRAM



7929237 0055302 13T

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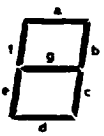
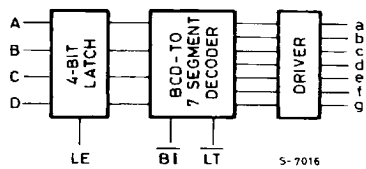
DISPLAY MODE



INPUT CODE										
A	L	H	L	H	L	H	L	H	L	H
B	L	L	H	H	L	L	H	H	L	L
C	L	L	L	L	H	H	H	H	L	L
D	L	L	L	L	L	L	L	L	H	H
DISPLAY	0	1	2	3	4	5	6	7	8	9
	0	1	2	3	4	5	6	7	8	9

BLOCK DIAGRAM



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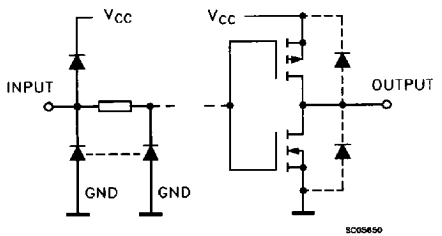
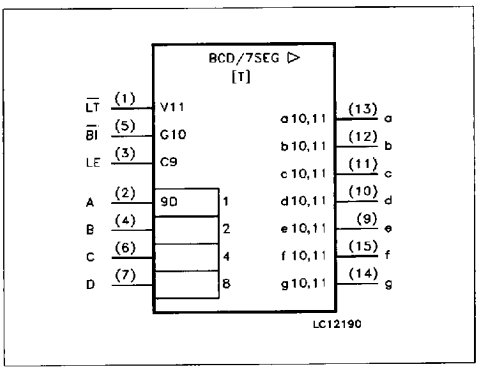
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3	LT	Lamp Test Input (Active LOW)
4	BI	Ripple Blanking Input (Active LOW)
5	LE	Latch Enable Input
7, 1, 2, 6	A to D	BCD Address Inputs
13, 12, 11, 10, 9 , 15, 14	a to g	Segment Outputs
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	-35/25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	+150/-50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
(*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series		-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6 V	0 to 400	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5			1.5		1.5		V
		4.5			3.15			3.15		3.15		
		6.0			4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0					0.5		0.5		0.5	V
		4.5					1.35		1.35		1.35	
		6.0					1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O=-20 μA	1.9	2.0		1.9		1.9		V
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5		I_O=-4.0 mA	3.2	3.8		2.9				
		6.0		I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	V_I = V_{IH} or V_{IL}	I_O= 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I_O= 4.0 mA		0.17	0.26		0.37		0.40	
		6.0		I_O= 5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND				±0.1		±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND				4		40		80	μA

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH}	Output Transition Time	2.0			25	60		75		90	ns
		4.5			7	12		15		18	
		6.0			6	11		13		15	
t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (BCD - Seg.)	2.0			125	255		320		385	ns
		4.5			33	51		64		77	
		6.0			23	43		54		65	
t_{PLH} t_{PHL}	Propagation Delay Time (BI - Seg.)	2.0			70	175		220		265	ns
		4.5			22	35		44		53	
		6.0			17	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LT}$ - Seg.)	2.0			60	120		150		180	ns
		4.5			15	24		30		36	
		6.0			12	20		26		31	
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{LE}$ - Seg.)	2.0			95	240		300		360	ns
		4.5			32	48		60		72	
		6.0			23	41		51		61	
$t_{W(L)}$	Minimum Pulse Width	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_s	Minimum Set-up Time	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				95						pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

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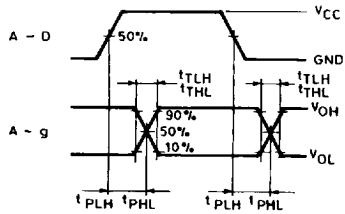
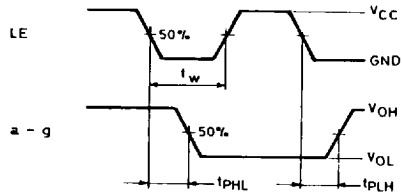
SWITCHING CHARACTERISTICS TEST WAVEFORM

Data Segment Delay Time



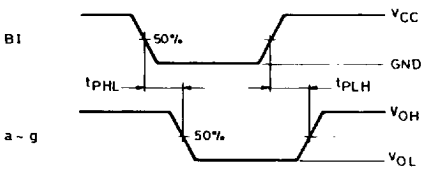
S-10229

LE-Segment Delay Time



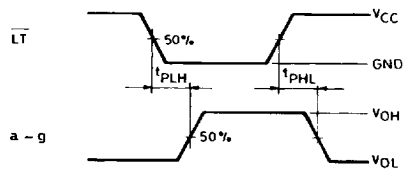
S-10230

$\overline{BI}$-Segment Delay Time



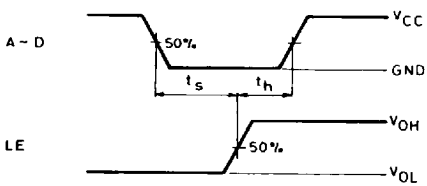
S-10231

$\overline{LT}$-Segment Delay Time



S-10232

Data Set-up/Hold Time



S-10233

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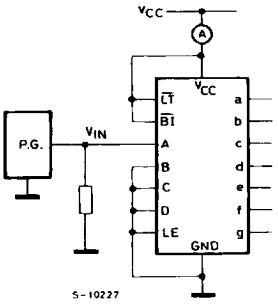
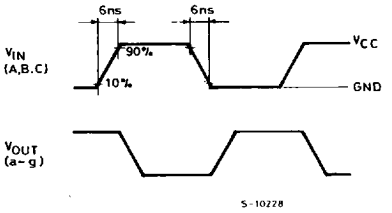
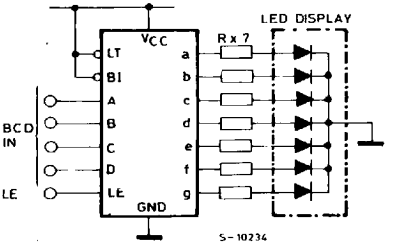
TEST CIRCUIT Icc (Opr.)





APPLICATION CIRCUIT

Static Display Circuit



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