HS-C²MOS™ INTEGRATED CIRCUITS

0-41946

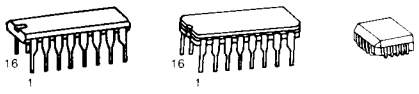
M54HC109
M74HC109

PRELIMINARY DATA

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

DESCRIPTION

The M54/74HC109 is a high speed CMOS DUAL J-K FLIP FLOP WITH PRESET AND CLEAR fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
In accordance with the logic level on the J and $\overline{K}$ input this device changes state on positive going transitions of the clock pulse. $\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and accomplished by a low logic level on the corrisponding input.
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.



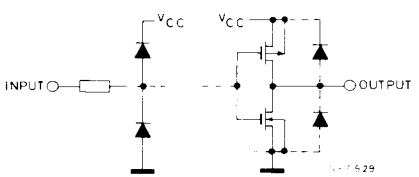
B1	F1	C1
Plastic Package	Ceramic Package	Chip Carrier

ORDERING NUMBERS: M54HC109 F1
M74HC109 B1
M74HC109 F1
M74HC109 C1

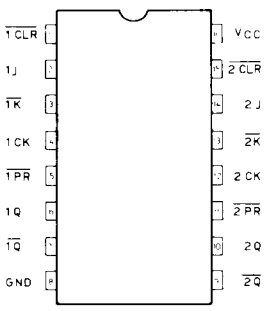
FEATURES

- High Speed
  f_{MAX} = 60 MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS109

INPUT AND OUTPUT EQUIVALENT CIRCUIT

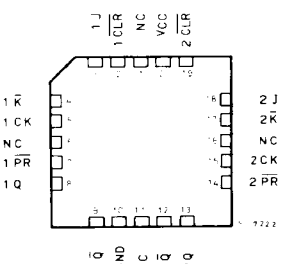


PIN CONNECTIONS
(top view)



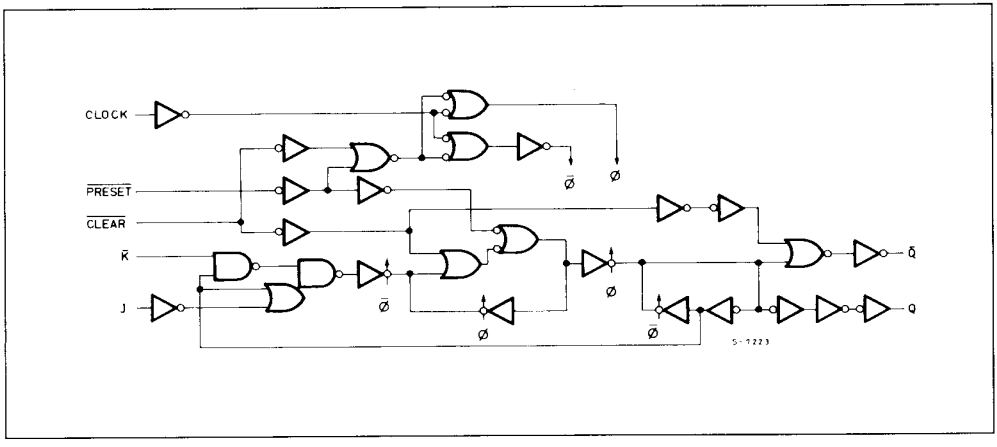
Dual in line

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM (1/2 Package)



TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↑	Qn	$\overline{Q}$n	NO CHANGE
H	H	L	L	↑	L	H	
H	H	H	H	↑	H	L	
H	H	H	L	↑	$\overline{Q}$n	Qn	TOOGLE
H	H	X	X	↓	Qn	$\overline{Q}$n	NO CHANGE

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	– 40 to 85 – 55 to 125		°C
t_r, t_f	Input Rise and Fall Time		V_{CC} 2 V	0 to 1000	ns
			4.5V	0 to 500	
			6 V	0 to 400	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20		40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, C_L = 15 pF, T_A = 25°C, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC MIN.	TYP.	MAX.	Unit
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK-Q, $\overline{Q}$)		18	29	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)		21	33	ns
f_{MAX}	Maximum Clock Frequency	33	63		MHz

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC Min.	Typ.	Max.	−40 to 85°C 74HC Min.	Max.	−55 to 125°C 54HC Min.	Max.	Unit
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	90 18 16			ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOK - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	80 21 18	165 33 28	— — —	200 40 34			ns
t_{PLH} t_{PHL}	Progation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	2.0 4.5 6.0		— — —	90 24 21	190 38 33	— — —	230 46 40			ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		6 30 35	15 57 65	— — —	5 25 29	— — —			MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	90 18 16			ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	90 18 16			ns
t_s	Minimum Set-up Time	2.0 4.5 6.0		— — —	35 8 5	75 15 13	— — —	90 18 16			ns
t_h	Minimum Hold Time	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0			ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	2.0 4.5 6.0		— — —	40 10 9	100 20 17	— — —	120 24 21			ns
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	47	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.