M54HC390
M74HC390

040666

HS-C²MOS™ INTEGRATED CIRCUITS

PRELIMINARY DATA

DUAL DECADE COUNTER

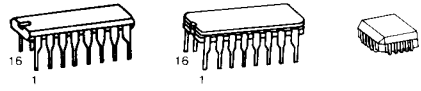
DESCRIPTION

The M54/74HC390 is a high speed CMOS DUAL DECADE COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This counter circuit contains independent ripple carry counters and incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual biquinary, or various combinations up to a single divide-by-100 counter.

Each 4-bit counter is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are ser to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

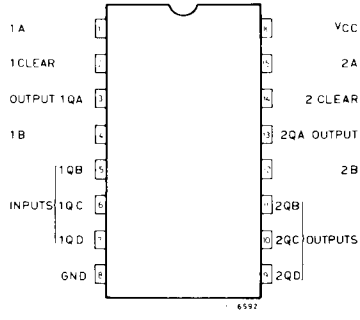
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

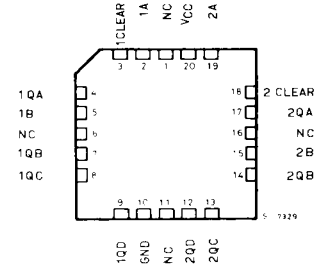
ORDERING NUMBERS: **M54HC390 F1**
M74HC390 B1
M74HC390 F1
M74HC390 C1

PIN CONNECTIONS
(top view)



Dual in line

CHIP CARRIER

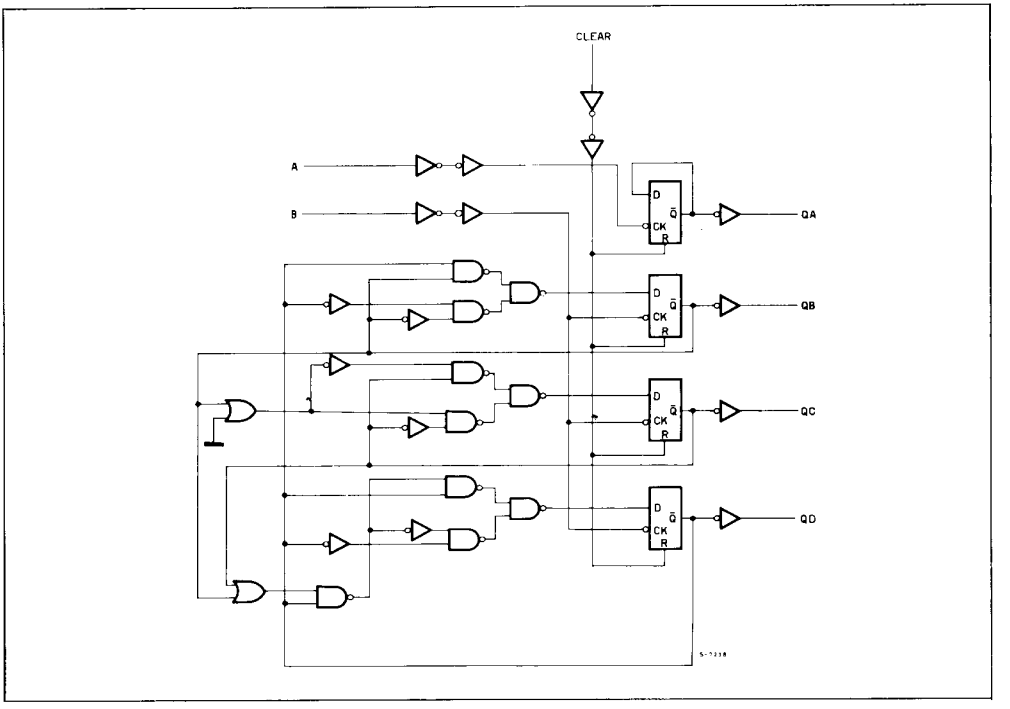


NC = No Internal Connection

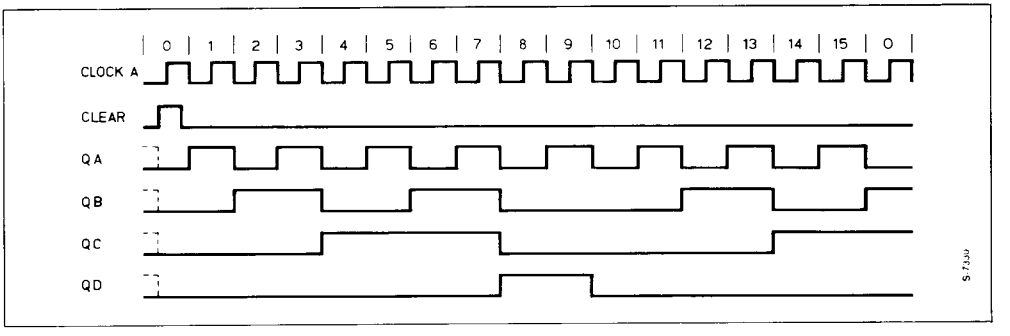
FEATURES

- High Speed
  t_{PD} = 13 ns (Typ) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS390

LOGIC DIAGRAM



TIMING CHART



TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT *				BI-QUINARY **			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

Note: * Output QA is connected to input B for BCD count.
** Output QD is connected to input A for bi-quinary count.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series	− 40 to 85		°C
		54HC Series	−55 to 125		
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V	0 to 1000		ns
		V_{CC} 4.5V	0 to 500		
		V_{CC} 6 V	0 to 400		

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1	—	0.1	V
		4.5			—	0	0.1	—	0.1	—	0.1	
		6.0			—	0	0.1	—	0.1	—	0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$-QA)		13	21	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QB, QD)		14	23	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QC)		21	33	ns
t_{PHL}	Propagation Delay Time (CL - Q)		16	26	ns
f_{MAX}	Maximum Clock Frequency	38	76		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse width (CK)		8	15	ns
$t_{W(L)}$	Minimum Pulse width (CL)		8	15	ns
t_{REM}	Minimum Removal Time (CL)		8	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{A}$ - QA)	2.0		—	73	130	—	160			ns
		4.5		—	16	26	—	32			
		6.0		—	14	22	—	28			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QB, QD)	2.0		—	73	135	—	165			ns
		4.5		—	17	27	—	33			
		6.0		—	15	23	—	28			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{B}$ - QC)	2.0		—	108	190	—	230			ns
		4.5		—	24	38	—	46			
		6.0		—	21	33	—	39			
t_{PHL}	Propagation Delay Time (CL - Q)	2.0		—	77	150	—	180			ns
		4.5		—	19	30	—	36			
		6.0		—	14	26	—	31			
f_{MAX}	Maximum Clock Frequency	2.0		7	20	—	5	—			MHz
		4.5		35	62	—	29	—			
		6.0		41	72	—	34	—			
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0		—	24	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(L)}$	Minimum Pulse Width (CL)	2.0		—	26	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{REM}	Minimum Removal Time	2.0		—	16	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	46	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$