HS-C²MOS™ INTEGRATED CIRCUITS

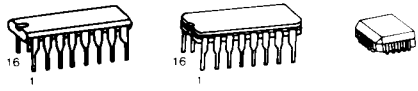
M54HC4017
M74HC4017

PRELIMINARY DATA

DECADE COUNTER/DIVIDER

DESCRIPTION

The M54/74HC4017 is a high speed CMOS DECADE COUNTER/DIVIDER fabricated in silicon gate C2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.
The M54/74HC4017 is a 5-stage Johnson counter with 10 decoded outputs. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output goes low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET inut is also provided which when taken high sets all the decoded outputs low.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



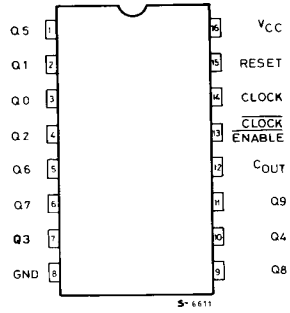
B1	F1	C1
Plastic Package	Ceramic Package	Chip Carrier

ORDERING NUMBERS: M54HC4017 F1
M74HC4017 B1
M74HC4017 F1
M74HC4017 C1

FEATURES

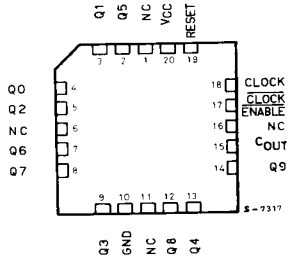
- High Speed
  t_{PD} = 21 ns (Typ.) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 4017 B

PIN CONNECTIONS
(top view)



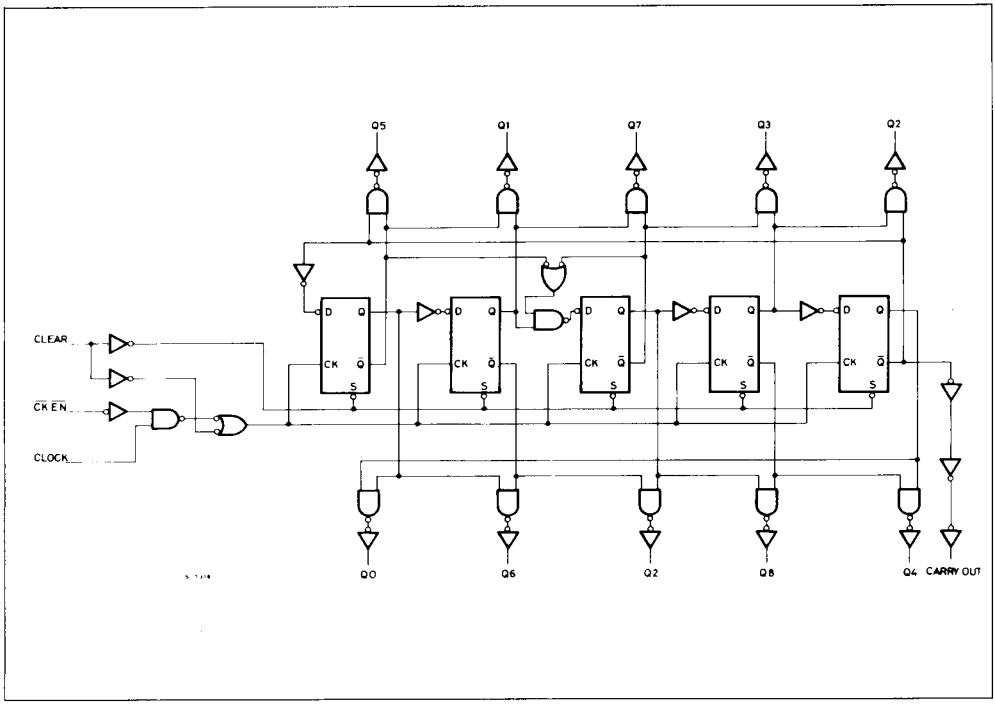
Dual in line

CHIP CARRIER



NC = No Internal Connection

LOGIC DIAGRAM



TRUTH TABLE

CLOCK	$\overline{\text{CLOCK ENABLE}}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↑	L	L	Qn + 1
↓	L	L	Qn
H	↑	L	Qn
H	↓	L	Qn + 1

X: DON'T CARE

Qn: NO CHANGE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

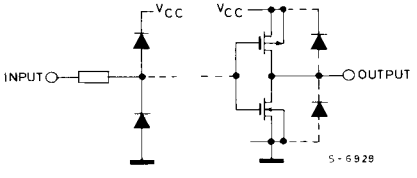
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit		Unit
V_{CC}	Supply Voltage	2 to 6		V
V_I	Input Voltage	0 to V_{CC}		V
V_O	Output Voltage	0 to V_{CC}		V
T_A	Operating Temperature 74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} 2 V 4.5V 6 V	0 to 1000 0 to 500 0 to 400	ns

INPUT AND OUTPUT EQUIVALENT CIRCUIT



DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5		V
		4.5			3.15	—	—	3.15	—	3.15		
		6.0			4.2	—	—	4.2	—	4.2		
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5		0.5	V
		4.5			—	—	1.35	—	1.35		1.35	
		6.0			—	—	1.8	—	1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9		V
		4.5	V_{IH} or V_{IL}	−20 μA	4.4	4.5	—	4.4	—	4.4		
		6.0			5.9	6.0	—	5.9	—	5.9		
		4.5		−4.0 mA	4.18	4.31	—	4.13	—	4.10		
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60		
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or V_{IL}	20 μA	—	0	0.1	—	0.1		0.1	V
		4.5			—	0	0.1	—	0.1		0.1	
		6.0			—	0	0.1	—	0.1		0.1	
		4.5		4.0 mA	—	0.17	0.26	—	0.33		0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33		0.40	
I_I	Input Leakage Current*	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND I_O = 0		—	—	4	—	40		80	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QN, CARRY OUT)		21	33	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q - CARRY OUT)		21	33	ns
f_{MAX}	Maximum Clock Frequency	30	47		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)		8	15	ns
$t_{W(H)}$	Minimum Pulse Width (CL)		8	15	ns
t_s	Minimum Set-up Time (CKEN)		—	0	ns
t_h	Minimum Hold Time (CKEN)		8	15	ns
t_{REM}	Minimum Removal Time (CL)		8	15	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	22	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time (CK - QN CARRY OUT)	2.0		—	109	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	21	34	—	40			
t_{PLH} t_{PHL}	Propagation Delay Time (CLEAR - Q CARRY OUT)	2.0		—	111	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	21	34	—	40			
f_{MAX}	Maximum Clock Frequency	2.0		5	12	—	4	—			ns
		4.5		25	41	—	20	—			
		6.0		29	48	—	23	—			
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	2.0		—	31	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(H)}$	Minimum Pulse Width (CL)	2.0		—	32	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_h	Minimum Hold Time (CKEN)	2.0		—	33	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{REM}	Minimum Removal Time (CL)	2.0		—	28	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
C_{IN}	Input capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance				74						pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.