DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

		BFQ10	11	12	13	14	15	16	
Difference in gate current	$\lvert\Delta I_G\rvert$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	< 5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0.98 < 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.98 1.02	0.95 1.05	0.95 1.05	
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	< 18	30	40	50	60	70	100	μV/V
Common mode rejection ratio	CMRR	> 95	90	85	85	80	80	80	dB

MECHANICAL DATA

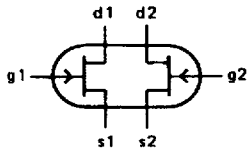
Dimensions in mm

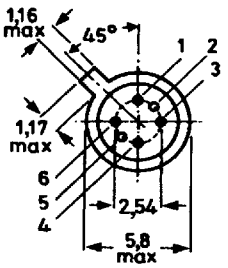
Fig. 1 TO-71.

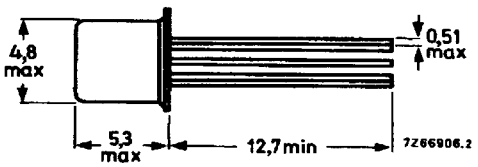
All leads insulated from the case.

Pinning

1 = source 1
2 = drain 1
3 = gate 1
4 = source 2
5 = drain 2
6 = gate 2







RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30 V
Drain-gate voltage (open source)	V_{DGO}	max.	30 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30 V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40 V
Drain current	I_D	max.	30 mA
Gate current	I_G	max.	10 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to + 200 °C
Junction temperature	T_j	max.	200 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	500 K/W

CHARACTERISTICS (total device)

T_{amb} = 25 °C unless otherwise specified

Measured at: I_D = 200 μA; V_{DG} = 15 V except for drain current ratio.

			BFQ10	11	12	13	14	15	16	
Drain current ratio (note 1) V_{DG} = 15 V; V_{GS} = 0	$\frac{I_{1D\text{-}1SS}}{I_{2D\text{-}2SS}}$	>	0.97	0.95	0.95	0.95	0.92	0.90	0.80	
		<	1.03	1.05	1.05	1.05	1.08	1.10	1.20	
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0.98	0.98	0.98	0.98	0.98	0.95	0.95	
		<	1.02	1.02	1.02	1.02	1.02	1.05	1.05	
Difference in transfer impedance (note 2)	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor (note 3)	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	18	30	40	50	60	70	100	μV/V
Common mode rejection ratio (note 4)	CMRR	>	95	90	85	85	80	80	80	dB

Notes

1. Measured under pulse conditions.
2. The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.
   $\left(\Delta\frac{1}{g_{fs}} = \frac{d\Delta V_{GS}}{dI_D}\right.$ at V_{DG} = constant).
3. The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.
   $\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\Delta V_{GS}}{dV_{DG}}\right.$ at I_D = constant).
4. Common mode rejection ratio:
   CMRR (in dB) = $-20\log\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$.

CHARACTERISTICS (Individual transistor)

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100 pA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20 nA
Gate current			
I_D = 200 μA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10 nA
Drain current (note 1)			
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		0.5 to 10 mA
Gate-source voltage			
I_D = 200 μA; V_{DG} = 15 V	$-V_{GS}$	<	2.7 V
Gate-source cut-off voltage			
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$		0.5 to 3.5 V
Transfer conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{fs}	>	1.0 mS
Output conductance at f = 1 kHz			
I_D = 200 μA; V_{DG} = 15 V	g_{os}	<	5 μS
Input capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{is}	<	8 pF
Feedback capacitance at f = 1 MHz (note 2)			
I_D = 200 μA; V_{DG} = 15 V	C_{rs}	<	1.0 pF
Equivalent noise voltage			
I_D = 200 μA; V_{DS} = 15 V; B = 0.6 to 100 Hz	V_n	<	0.5 μV

Notes

1. Measured under pulse conditions.
2. Measured with case grounded.