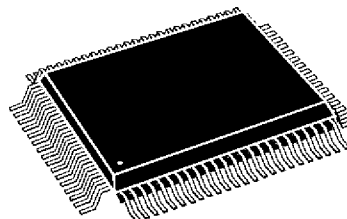
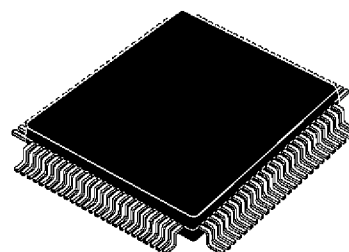


16-BIT ROMLESS MICROCONTROLLER**ADVANCE DATA**

- High performance 16-bit CPU with 4-stage pipeline
- 100 ns instruction cycle time at 20-MHz CPU clock
- 500 ns multiplication (16×16 bits), 1 μ s division (32 / 16 bit)
- Enhanced boolean bit manipulation facilities
- Additional instructions to support HLL and operating systems
- Register-based design with multiple variable register banks
- Single-cycle context switching support
- Up to 16 Mbytes linear address space for code and data
- 2 Kbytes on-chip RAM
- Programmable external bus characteristics for different address ranges
- 8-Bit or 16-bit external data bus
- Multiplexed or demultiplexed external address/data buses
- Five programmable chip-select signals
- Hold- and hold-acknowledge bus arbitration support
- 1024 bytes on-chip special function register area
- Idle and power down modes
- 8-channel interrupt-driven single-cycle data transfer facilities via peripheral event controller (PEC)
- 16-priority-level interrupt system with 28 sources, sample-rate down to 50 ns
- Two multi-functional general purpose timer units with 5 timers
- Two serial channels (synchronous/asynchronous and high-speed-synchronous)
- Programmable watchdog timer
- Up to 77 general purpose I/O lines
- Supported by a wealth of development tools like C-compilers, macro-assembler packages, emulators, evaluation boards, HLL-debuggers, simulators, logic analyser disassemblers, programming boards
- On-chip bootstrap loader
- 100-Pin TQFP and PQFP package (EIAJ)

**PQFP100****TQFP100**

(Ordering Information at the end of the datasheet)

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1 INTRODUCTION

The ST10R165 is a new derivative of the SGS-THOMSON ST10 family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 10 million instructions per second) with high peripheral functionality and enhanced IO-capabilities.

Figure 1. Logic Symbol

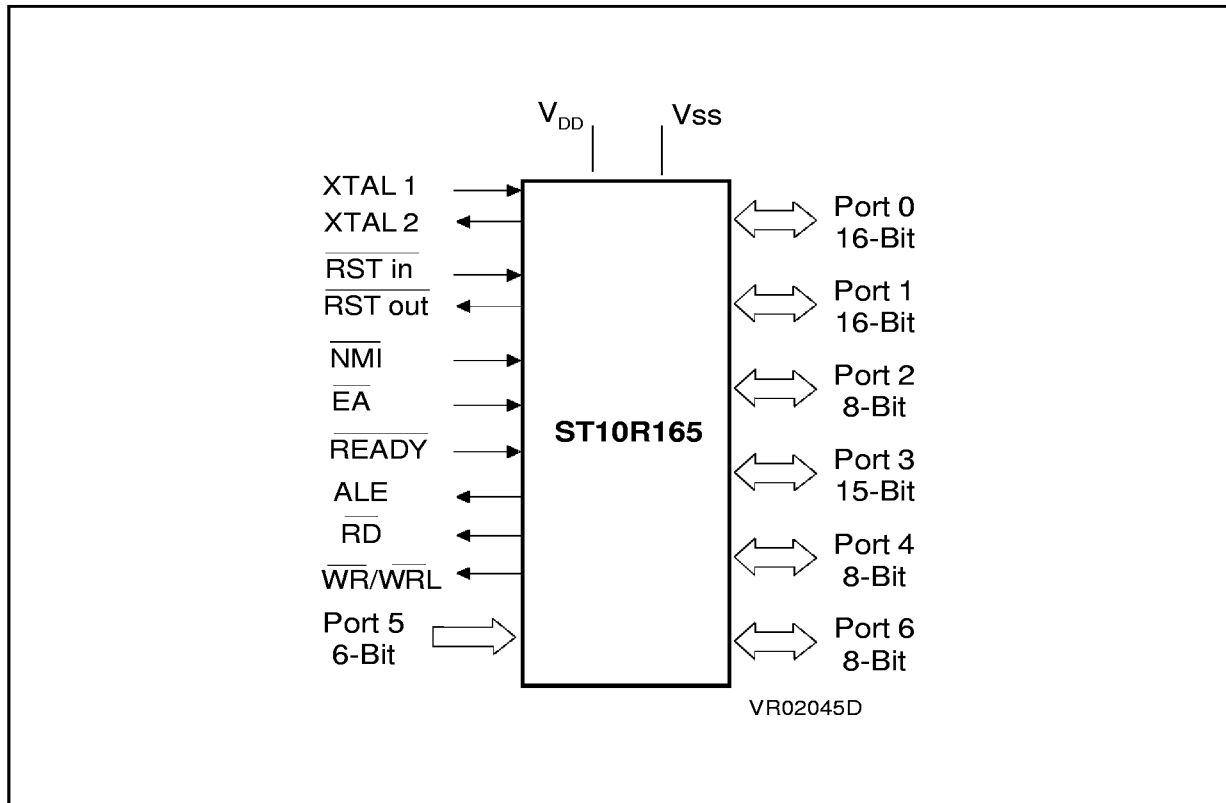


Figure 2. PQFP Pin Configuration (top view)

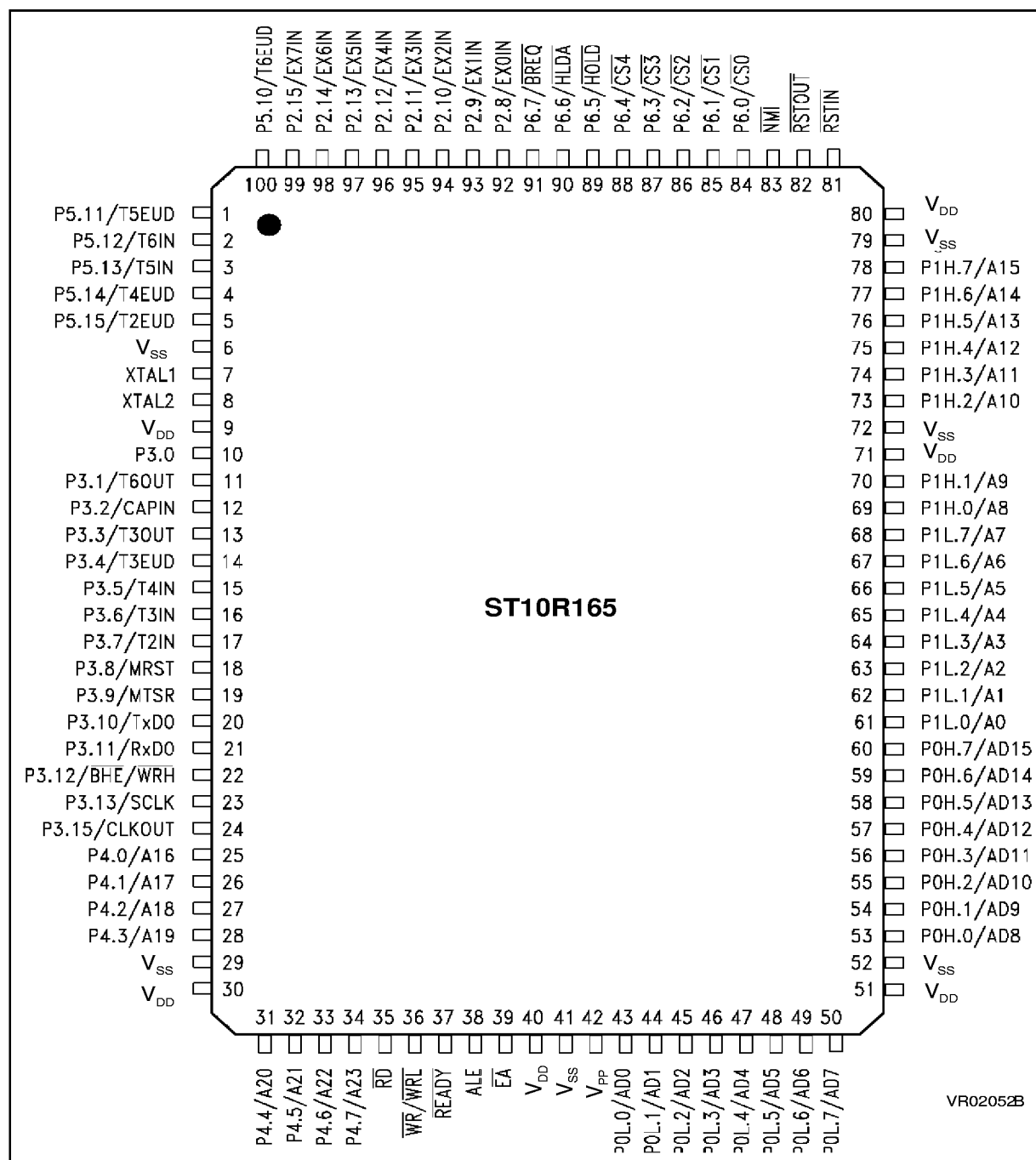


Figure 3. TQFP Pin Configuration (top view)

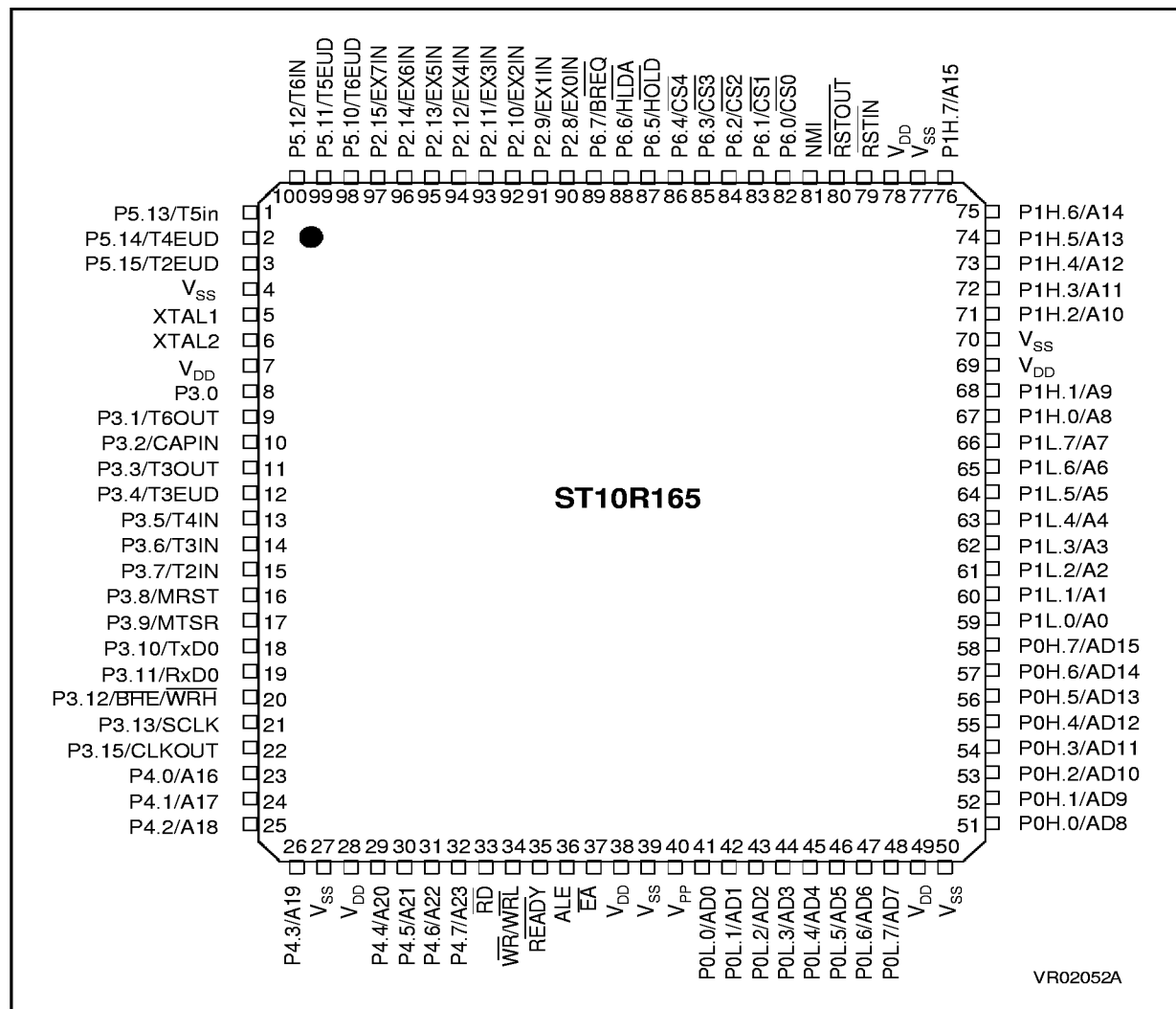


Table 1. Pin Definitions and Functions

| Symbol | Pin Number | | Input (I) Output (O) | Function |
|---------------------|---|--|---|---|
| | PQFP | TQFP | | |
| P5.10 – P5.15 | 100 1 - 5 100 1 2 3 4 5 | 98 99 - 3 98 99 100 1 2 3 | I I I I I I I I | Port 5 is a 6-bit input-only port with Schmitt-Trigger characteristics. The pins of Port 5 also serve as timer inputs: P5.10 T6EUD GPT2 Timer T6 Ext.Up/Down Ctrl.Input P5.11 T5EUD GPT2 Timer T5 Ext.Up/Down Ctrl.Input P5.12 T6IN GPT2 Timer T6 Count Input P5.13 T5IN GPT2 Timer T5 Count Input P5.14 T4EUD GPT1 Timer T4 Ext.Up/Down Ctrl.Input P5.15 T2EUD GPT1 Timer T2 Ext.Up/Down Ctrl.Input |
| XTAL1 | 7 | 5 | I | XTAL1: Input to the oscillator amplifier and input to the internal clock generator |
| XTAL2 | 8 | 6 | O | XTAL2: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed. |
| P3.0 – P3.13, P3.15 | 10 – 23, 24 11 12 13 14 15 16 17 18 19 20 21 22 23 24 | 8 21 22 9 10 11 12 13 14 15 16 17 18 19 20 21 22 | I/O I/O I/O O I O I I I I I/O I/O O I/O O O O I/O O | Port 3 is a 15-bit (P3.14 is missing) bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The following Port 3 pins also serve for alternate functions: P3.1 T6OUT GPT2 Timer T6 Toggle Latch Output P3.2 CAPIN GPT2 Register CAPREL Capture Input P3.3 T3OUT GPT1 Timer T3 Toggle Latch Output P3.4 T3EUD GPT1 Timer T3 Ext.Up/Down Ctrl.Input P3.5 T4IN GPT1 Timer T4 Input for Count/Gate/Reload/Capture P3.6 T3IN GPT1 Timer T3 Count/Gate Input P3.7 T2IN GPT1 Timer T2 Input for Count/Gate/Reload/Capture P3.8 MRST SSC Master-Rec./Slave-Transmit I/O P3.9 MTSR SSC Master-Transmit/Slave-Rec. O/I P3.10 TxD0 ASC0 Clock/Data Output (Asyn./Syn.) P3.11 RxD0 ASC0 Data Input (Asyn.) or I/O (Syn.) P3.12 BHE Ext. Memory High Byte Enable Signal, WRH Ext. Memory High Byte Write Strobe P3.13 SCLK SSC Master Clock Outp./Slave Cl. Inp. P3.15 CLKOUT System Clock Output (=CPU Clock) |

Table 1. Pin Definitions and Functions (Cont'd)

| Symbol | Pin Number | | Input (I) Output (O) | Function |
|--------------------------------|------------------|------------------|-------------------------|--|
| | PQFP | TQFP | | |
| P4.0 – P4.7 | 25 - 28, 31 - 34 | 23 - 26, 29 - 32 | I/O | Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, Port 4 can be used to output the segment address lines: P4.0 A16 Least Significant Segment Addr. Line P4.7 A23 Most Significant Segment Addr. Line |
| \overline{RD} | 35 | 33 | O | External Memory Read Strobe. \overline{RD} is activated for every external instruction or data read access. |
| $\overline{WR}/\overline{WRL}$ | 36 | 34 | O | External Memory Write Strobe. In \overline{WR} -mode this pin is activated for every external data write access. In \overline{WRL} -mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection. |
| \overline{READY} | 37 | 35 | I | Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. |
| ALE | 38 | 36 | O | Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes. |
| EA | 39 | 37 | I | External Access Enable pin. A low level at this pin during and after Reset forces the ST10R165 to begin instruction execution out of external memory. A high level forces execution out of the internal ROM. The ST10R165 must have this pin tied to '0'. |

Table 1. Pin Definitions and Functions (Cont'd)

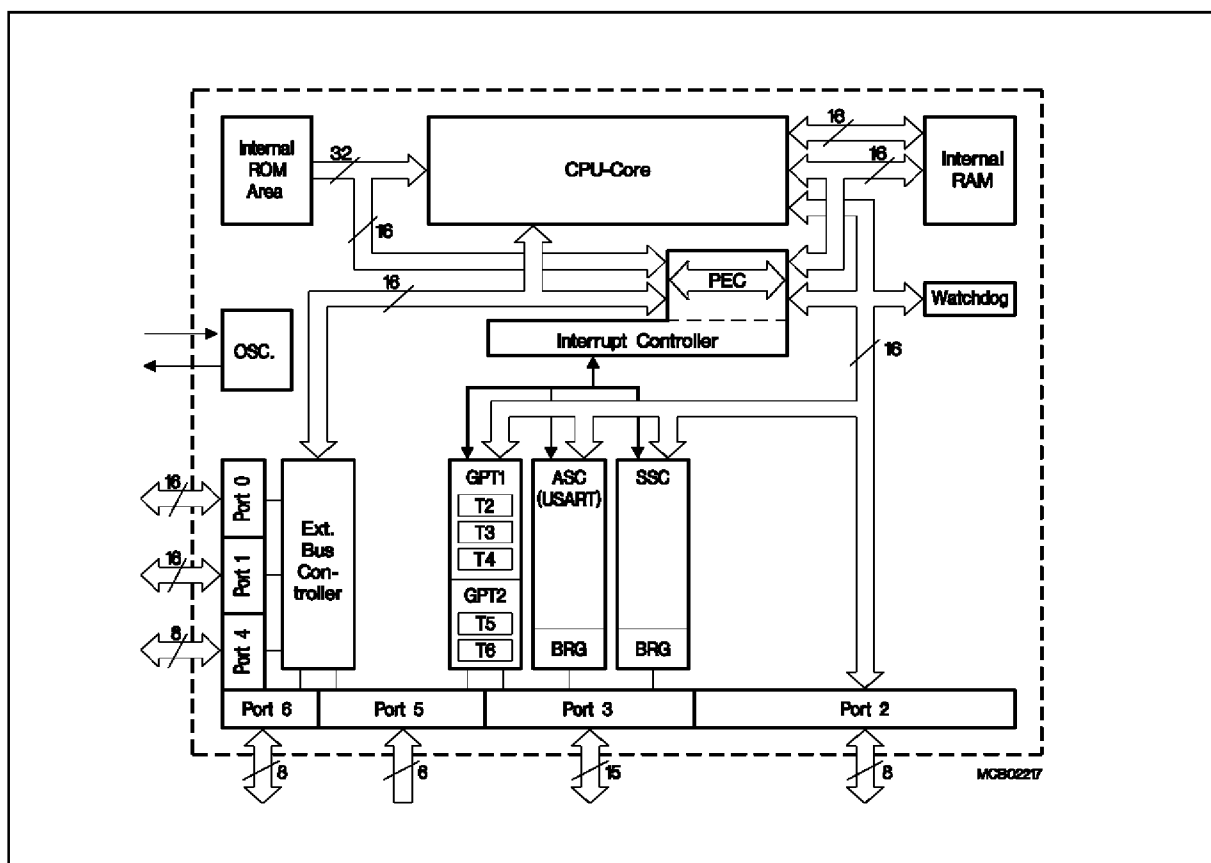
| Symbol | Pin Number | | Input (I) Output (O) | Function |
|---|--------------------------------------|--------------------------------|-------------------------|--|
| | PQFP | TQFP | | |
| PORT0: P0L.0 – P0L.7, P0H.0 - P0H.7 | 43 – 50 53 – 60 | 41 48 51 58 | I/O | PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes: Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 Multiplexed bus modes: Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15 |
| PORT1: P1L.0 – P1L.7, P1H.0 - P1H.7 | 61 - 68 69 - 70, 73 - 78 | 59 66 67 - 68 71 - 76 | I/O | PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. |
| RSTIN | 81 | 79 | I | Reset Input with Schmitt-Trigger characteristics. A low level at this pin for a specified duration while the oscillator is running re-sets the ST10R165. An internal pullup resistor permits power-on reset using only a capacitor connected to V _{SS} . |
| RSTOUT | 82 | 80 | O | Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. RSTOUT remains low until the EINIT (end of initialization) instruction is executed. |
| NMI | 83 | 81 | I | Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the ST10R65 to go into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally. |

Table 1. Pin Definitions and Functions (Cont'd)

| Symbol | Pin Number | | Input (I) Output (O) | Function |
|-----------------|-----------------------|-----------------------|-------------------------|--|
| | PQFP | TQFP | | |
| P6.0 – P6.7 | 84 - 91 | 82 - 89 | I/O | Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The following Port 6 pins also serve for alternate functions: P6.0 $\overline{CS0}$ Chip Select 0 Output P6.4 $\overline{CS4}$ Chip Select 4 Output P6.5 \overline{HOLD} External Master Hold Request Input P6.6 \overline{HLDA} Hold Acknowledge Output P6.7 \overline{BREQ} Bus Request Output |
| P2.8 – P2.15 | 92 - 99 | 90 - 97 | I/O | Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins also serve for alternate functions: P2.8 EX0IN Fast External Interrupt 0 Input P2.15 EX7IN Fast External Interrupt 7 Input |
| V _{PP} | 42 | 40 | - | Flash programming voltage. This pin accepts the programming voltage for flash versions of the ST10R165. Note: This pin is not connected (NC) on non-flash versions. |
| V _{DD} | 9, 30, 40, 51, 71, 80 | 7, 28, 38, 49, 69, 78 | - | Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode |
| V _{SS} | 6, 29, 41, 52, 72, 79 | 4, 27, 39, 50, 70, 77 | - | Digital Ground. |

Note: All time specifications refer to a CPU clock of 20 MHz (see definition in the AC Characteristics section).

Figure 4. Block Diagram



3 MEMORY ORGANIZATION

The memory space of the ST10R165 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have additionally been made directly bit addressable. The ST10R165 is prepared to incorporate on-chip mask-programmable ROM for code or constant data. Currently no ROM is integrated.

2 KBytes of on-chip RAM are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) named General Purpose Registers (GPRs).

1024 bytes (2 * 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word-wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future derivatives of the ST10R165.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

4 EXTERNAL BUS CONTROLLER

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

- 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
- 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
- 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adoption of a wide range of different types of memories. In addition, different address ranges may be accessed with different bus characteristics. Up to 5 external \overline{CS} signals can be generated in order to save external glue logic. Access to very slow memories is supported via a particular 'Ready' function. A $\overline{HOLD}/\overline{HLDA}$ protocol is available for bus arbitration.

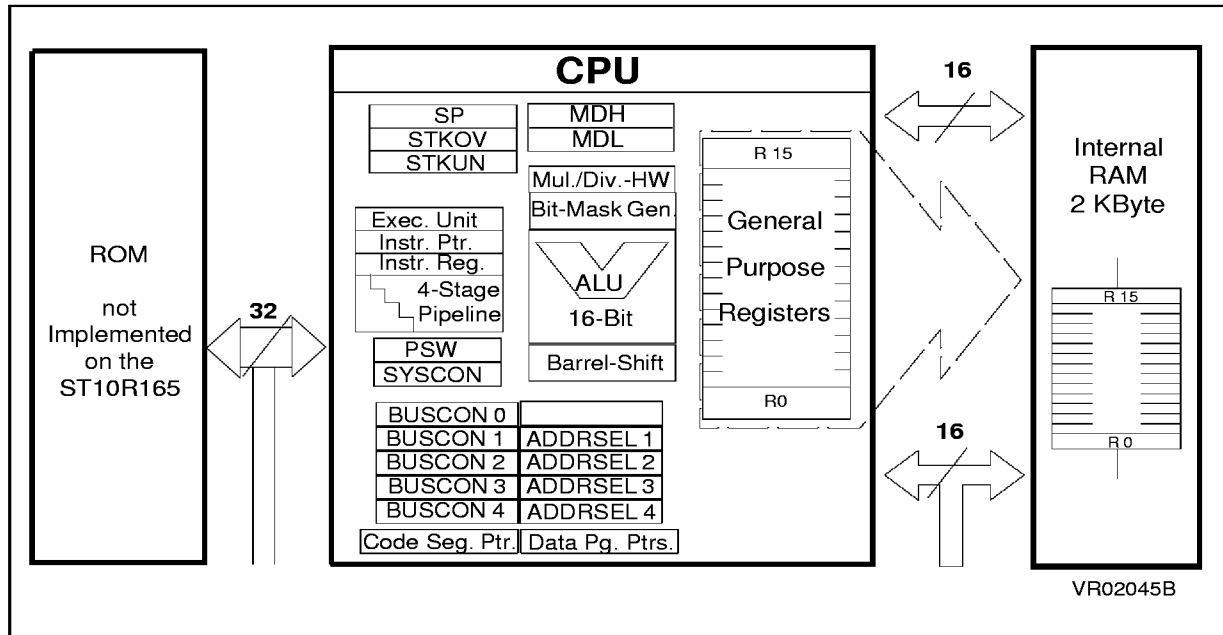
For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte or to 64 KByte. In this case Port 4 outputs four, two or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

5 CENTRAL PROCESSING UNIT (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been added for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the ST10R165's instructions can be executed in just one machine cycle which requires 100 ns at 20 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16×16 bit multiplication in 5 cycles and a 32/16 bit division in 10 cycles. Another pipeline optimization, the named 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

Figure 5. CPU Block Diagram



Central Processing Unit (Cont'd)

The CPU includes an actual register context consisting of up to 16 wordwide GPRs which are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at a time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 2048 bytes is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient ST10R165 instruction set which includes the following instruction classes:

- Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

6 INTERRUPT SYSTEM

With an interrupt response time within a range from just 250 ns to 600 ns (in case of internal program execution), the ST10R165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the ST10R165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The ST10R165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

The following table shows all of the possible ST10R165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers:

Note: Four nodes in the table (X-Peripheral nodes) are prepared to accept interrupt requests from integrated X-Bus peripherals. Nodes, where no X-Peripherals are connected, may be used to generate software controlled interrupt requests by setting the respective XPNR bit. Also the three listed Software Nodes can be used for this purpose.

Interrupt System (Cont'd)

| Source of Interrupt or PEC Service Request | Request Flag | Enable Flag | Interrupt Vector | Vector Location | Trap Number |
|--|--------------|-------------|------------------|-----------------|-------------|
| External Interrupt 0 | CC8IR | CC8IE | CC8INT | 60h | 18h |
| External Interrupt 1 | CC9IR | CC9IE | CC9INT | 64h | 19h |
| External Interrupt 2 | CC10IR | CC10IE | CC10INT | 68h | 1Ah |
| External Interrupt 3 | CC11IR | CC11IE | CC11INT | 6Ch | 1Bh |
| External Interrupt 4 | CC12IR | CC12IE | CC12INT | 70h | 1Ch |
| External Interrupt 5 | CC13IR | CC13IE | CC13INT | 74h | 1Dh |
| External Interrupt 6 | CC14IR | CC14IE | CC14INT | 78h | 1Eh |
| External Interrupt 7 | CC15IR | CC15IE | CC15INT | 7Ch | 1Fh |
| GPT1 Timer 2 | T2IR | T2IE | T2INT | 88h | 22h |
| GPT1 Timer 3 | T3IR | T3IE | T3INT | 8Ch | 23h |
| GPT1 Timer 4 | T4IR | T4IE | T4INT | 90h | 24h |
| GPT2 Timer 5 | T5IR | T5IE | T5INT | 94h | 25h |
| GPT2 Timer 6 | T6IR | T6IE | T6INT | 98h | 26h |
| GPT2 CAPREL Register | CRIR | CRIE | CRINT | 9Ch | 27h |
| ASC0 Transmit | S0TIR | S0TIE | S0TINT | A8h | 2Ah |
| ASC0 Transmit Buffer | S0TBIR | S0TBIE | S0TBINT | 11Ch | 47h |
| ASC0 Receive | S0RIR | S0RIE | S0RINT | ACh | 2Bh |
| ASC0 Error | S0EIR | S0EIE | S0EINT | B0h | 2Ch |
| SSC Transmit | SCTIR | SCTIE | SCTINT | B4h | 2Dh |
| SSC Receive | SCRIR | SCRIE | SCRINT | B8h | 2Eh |
| SSC Error | SCEIR | SCEIE | SCEINT | BCh | 2Fh |
| X-Peripheral Node 0 | XP0IR | XP0IE | XP0INT | 100h | 40h |
| X-Peripheral Node 1 | XP1IR | XP1IE | XP1INT | 104h | 41h |
| X-Peripheral Node 2 | XP2IR | XP2IE | XP2INT | 108h | 42h |
| X-Peripheral Node 3 | XP3IR | XP3IE | XP3INT | 10Ch | 43h |
| Software Node | CC29IR | CC29IE | CC29INT | 110h | 44h |
| Software Node | CC30IR | CC30IE | CC30INT | 114h | 45h |
| Software Node | CC31IR | CC31IE | CC31INT | 118h | 46h |

Interrupt System (Cont'd)

The ST10R165 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, named 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

The following table shows all of the possible exceptions or error conditions that can arise during run-time:

| Exception Condition | Trap Flag | Trap Vector | Vector Location | Trap Number | Trap Priority |
|--|--|---|--|---|-------------------------------|
| Reset Functions: Hardware Reset Software Reset Watchdog Timer Overflow | | RESET RESET RESET | 00'0000h 00'0000h 00'0000h | 00h 00h 00h | III III III |
| Class A Hardware Traps: Non-Maskable Interrupt Stack Overflow Stack Underflow | NMI STKOF STKUF | NMITRAP STOTRAP STUTRAP | 00'0008h 00'0010h 00'0018h | 02h 04h 06h | II II II |
| Class B Hardware Traps: Undefined Opcode Protected Instruction Fault Illegal Word Operand Access Illegal Instruction Access Illegal External Bus Access | UNDOPC PRTFLT ILLOPA ILLINA ILLBUS | BTRAP BTRAP BTRAP BTRAP BTRAP | 00'0028h 00'0028h 00'0028h 00'0028h 00'0028h | 0Ah 0Ah 0Ah 0Ah 0Ah | I I I I I |
| Reserved | | | [2Ch – 3Ch] | [0Bh – 0Fh] | |
| Software Traps TRAP Instruction | | | Any [00'0000h – 00'01FCh] in steps of 4h | Any [00h – 7Fh] | Current CPU Priority |

7 GENERAL PURPOSE TIMER (GPT) UNIT

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of module GPT1 can be configured individually for one of three basic modes of operation, which are Timer, Gated Timer, and Counter Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 400 ns (@ 20 MHz CPU clock).

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e. g. position tracking.

Timers T3 and T4 have output toggle latches (TxOTL) which change their state on each timer over-flow/underflow. The state of these latches may be output on port pins (TxOUT) e. g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

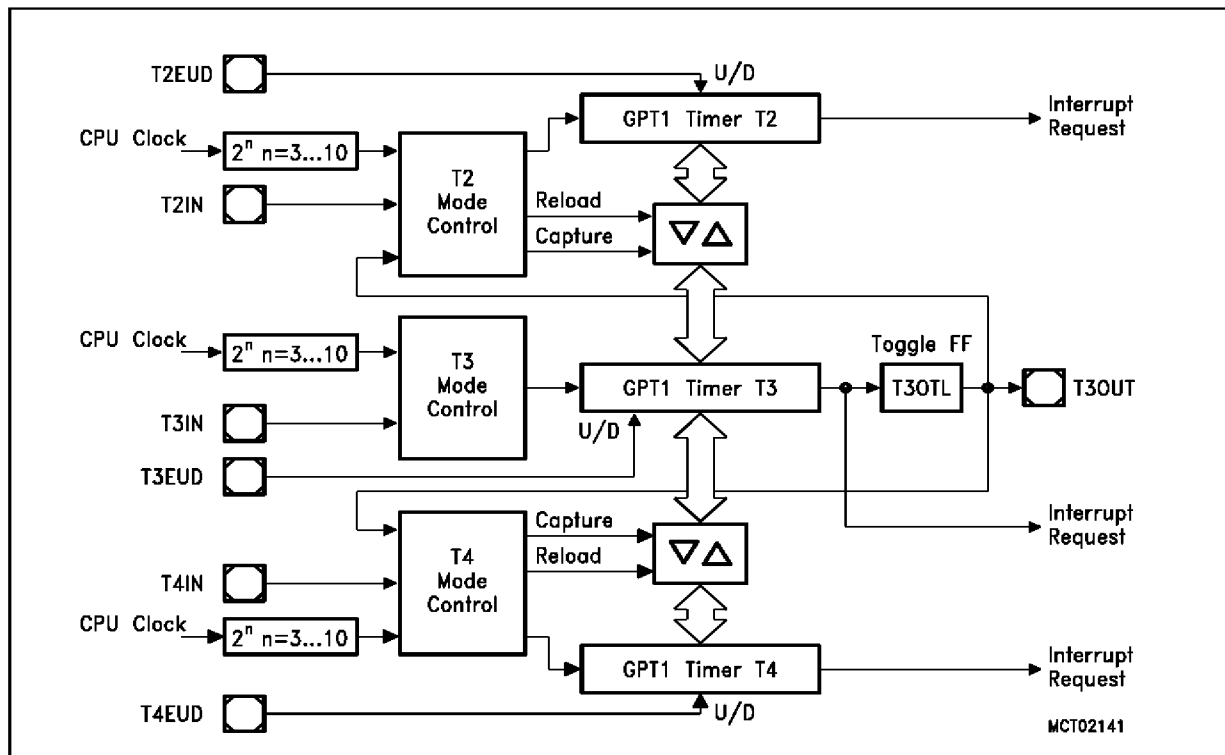
In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

General Purpose Timer (GPT) Unit (Cont'd)

With its maximum resolution of 200 ns (@ 20 MHz), the GPT2 module provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

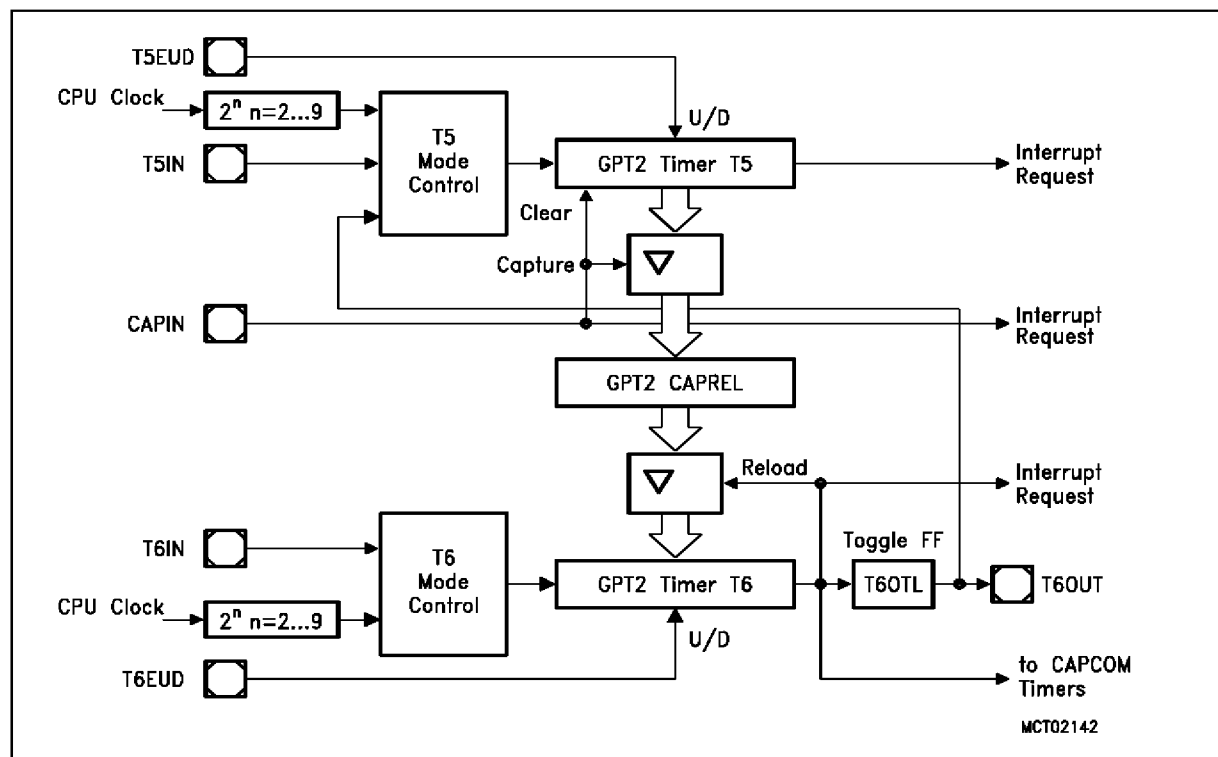
The state of this latch may be used to clock timer T5, or it may be output on a port pin (T6OUT). The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM timers T0 or T1, and to cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows absolute time differences to be measured or pulse multiplication to be performed without software overhead.

Figure 6. Block Diagram of GPT1



General Purpose Timer (GPT) Unit (Cont'd)

Figure 7. Block Diagram of GPT2



8 PARALLEL PORTS

The ST10R165 provides up to 77 I/O lines which are organized into six input/output ports and one input port. All port lines are bit-addressable, and all input/output lines are individually (bit-wise) programmable as inputs or outputs via direction registers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. The output drivers of three I/O ports can be configured (pin by pin) for push/pull operation or open-drain operation via control registers. During the internal reset, all port pins are configured as inputs.

All port lines have programmable alternate input or output functions associated with them. PORT0 and PORT1 may be used as address and data lines when accessing external memory, while Port 4 outputs the additional segment address bits A23/19/17...A16 in systems where segmentation is enabled to access more than 64KBytes of memory. Port 6 provides optional bus arbitration signals ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) and chip select signals. Port 3 includes alternate functions of timers, serial interfaces, the optional bus control signal $\overline{\text{BHE}}$ and the system clock output (CLKOUT). Port 5 is used for timer control signals. All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

9 SERIAL CHANNELS

Serial communication with other microcontrollers, processors, terminals or external peripheral components is provided by two serial interfaces with different functionality, an Asynchronous/Synchronous Serial Channel (ASC0) and a High-Speed Synchronous Serial Channel (SSC).

They support full-duplex asynchronous communication up to 625 KBaud and half-duplex synchronous communication up to 5 Mbaud (2.5 Mbaud on the ASC0) @ 20 MHz system clock.

Two dedicated baud rate generators allow to set up all standard baud rates without oscillator tuning. For transmission, reception, and erroneous reception 3 separate interrupt vectors are provided for each serial channel.

In asynchronous mode, 8- or 9-bit data frames are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data + wake up bit mode).

Serial Channels (Cont'd)

In synchronous mode, the ASC0 transmits or receives bytes (8 bits) synchronously to a shift clock which is generated by the ASC0. The SSC transmits or receives characters of 2...16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB, while the ASC0 always shifts the LSB first. A loop back option is available for testing purposes.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

10 WATCHDOG TIMER

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided either by 2 or by 128. The high byte of the Watchdog Timer register can be set to a pre-specified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 25 μs and 420 ms can be monitored (@ 20 MHz). The default Watchdog Timer interval after reset is 6.55 ms (@ 20 MHz).

11 INSTRUCTION SET SUMMARY

The table below lists the instructions of the ST10R165 in a condensed way. The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the “**ST10 Programming Manual**”.

This document also provides a detailed description of each instruction.

| Mnemonic | Description | Bytes |
|-----------------|---|-------|
| ADD(B) | Add word (byte) operands | 2 / 4 |
| ADDC(B) | Add word (byte) operands with Carry | 2 / 4 |
| SUB(B) | Subtract word (byte) operands | 2 / 4 |
| SUBC(B) | Subtract word (byte) operands with Carry | 2 / 4 |
| MUL(U) | (Un)Signed multiply direct GPR by direct GPR (16-16-bit) | 2 |
| DIV(U) | (Un)Signed divide register MDL by direct GPR (16-/16-bit) | 2 |
| DIVL(U) | (Un)Signed long divide reg. MD by direct GPR (32-/16-bit) | 2 |
| CPL(B) | Complement direct word (byte) GPR | 2 |
| NEG(B) | Negate direct word (byte) GPR | 2 |
| AND(B) | Bitwise AND, (word/byte operands) | 2 / 4 |
| OR(B) | Bitwise OR, (word/byte operands) | 2 / 4 |
| XOR(B) | Bitwise XOR, (word/byte operands) | 2 / 4 |
| BCLR | Clear direct bit | 2 |
| BSET | Set direct bit | 2 |
| BMOV(N) | Move (negated) direct bit to direct bit | 4 |
| BAND, BOR, BXOR | AND/OR/XOR direct bit with direct bit | 4 |
| BCMP | Compare direct bit to direct bit | 4 |
| BFLDH/L | Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data | 4 |
| CMP(B) | Compare word (byte) operands | 2 / 4 |
| CMPD1/2 | Compare word data to GPR and decrement GPR by 1/2 | 2 / 4 |
| CMPI1/2 | Compare word data to GPR and increment GPR by 1/2 | 2 / 4 |
| PRIOR | Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR | 2 |
| SHL / SHR | Shift left/right direct word GPR | 2 |
| ROL / ROR | Rotate left/right direct word GPR | 2 |

Instruction Set (Cont'd)

| Mnemonic | Description | Bytes |
|---------------------|---|-------|
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS | Move byte operand to word operand with sign extension | 2 / 4 |
| MOVBZ | Move byte operand to word operand. with zero extension | 2 / 4 |
| JMPA, JMPI, JMPR | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| J(N)B | Jump relative if direct bit is (not) set | 4 |
| JBC | Jump relative and clear bit if direct bit is set | 4 |
| JNBS | Jump relative and set bit if direct bit is not set | 4 |
| CALLA, CALLI, CALLR | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH, POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET | Return from intra-segment subroutine | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETP | Return from intra-segment subroutine and pop direct word register from system stack | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Enter Power Down Mode (supposes NMI-pin being low) | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT | Disable Watchdog Timer | 4 |
| EINIT | Signify End-of-Initialization on RSTOUT-pin | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTENDED Register sequence | 2 |
| EXTP(R) | Begin EXTENDED Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTENDED Segment (and Register) sequence | 2 / 4 |
| NOP | Null operation | 2 |

12 SPECIAL FUNCTION REGISTER OVERVIEW

The following table lists all SFRs which are implemented in the ST10R165 in alphabetical order.

Bit-addressable SFRs are marked with the letter “b” in column “Name”. SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter “E” in column “Physical Address”.

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|----------|------------------|---------------|--|-------------|
| ADDRSEL1 | FE18h | 0Ch | Address Select Register 1 | 0000h |
| ADDRSEL2 | FE1Ah | 0Dh | Address Select Register 2 | 0000h |
| ADDRSEL3 | FE1Ch | 0Eh | Address Select Register 3 | 0000h |
| ADDRSEL4 | FE1Eh | 0Fh | Address Select Register 4 | 0000h |
| BUSCON0b | FF0Ch | 86h | Bus Configuration Register 0 | 0XX0h |
| BUSCON1b | FF14h | 8Ah | Bus Configuration Register 1 | 0000h |
| BUSCON2b | FF16h | 8Bh | Bus Configuration Register 2 | 0000h |
| BUSCON3b | FF18h | 8Ch | Bus Configuration Register 3 | 0000h |
| BUSCON4b | FF1Ah | 8Dh | Bus Configuration Register 4 | 0000h |
| CAPREL | FE4Ah | 25h | GPT2 Capture/Reload Register | 0000h |
| CC8IC b | FF88h | C4h | EX0IN Interrupt Control Register | 0000h |
| CC9IC b | FF8Ah | C5h | EX1IN Interrupt Control Register | 0000h |
| CC10IC b | FF8Ch | C6h | EX2IN Interrupt Control Register | 0000h |
| CC11IC b | FF8Eh | C7h | EX3IN Interrupt Control Register | 0000h |
| CC12IC b | FF90h | C8h | EX4IN Interrupt Control Register | 0000h |
| CC13IC b | FF92h | C9h | EX5IN Interrupt Control Register | 0000h |
| CC14IC b | FF94h | CAh | EX6IN Interrupt Control Register | 0000h |
| CC15IC b | FF96h | CBh | EX7IN Interrupt Control Register | 0000h |
| CC29IC b | F184h E | C2h | Software Node Interrupt Control Register | 0000h |
| CC30IC b | F18Ch E | C6h | Software Node Interrupt Control Register | 0000h |
| CC31IC b | F194h E | CAh | Software Node Interrupt Control Register | 0000h |
| CP | FE10h | 08h | CPU Context Pointer Register | FC00h |

Special Function Register Overview (Cont'd)

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|-------------|--------------------|---------------|---|-------------|
| CRIC b | FF6Ah | B5h | GPT2 CAPREL Interrupt Control Register | 0000h |
| CSP | FE08h | 04h | CPU Code Segment Pointer Register (read only) | 0000h |
| DP0L b | F100h _E | 80h | P0L Direction Control Register | 00h |
| DP0H b | F102h _E | 81h | P0h Direction Control Register | 00h |
| DP1L b | F104h _E | 82h | P1L Direction Control Register | 00h |
| DP1H b | F106h _E | 83h | P1h Direction Control Register | 00h |
| DP2 b | FFC2h | E1h | Port 2 Direction Control Register | 0000h |
| DP3 b | FFC6h | E3h | Port 3 Direction Control Register | 0000h |
| DP4 b | FFCAh | E5h | Port 4 Direction Control Register | 00h |
| DP6 b | FFCEh | E7h | Port 6 Direction Control Register | 00h |
| DPP0 | FE00h | 00h | CPU Data Page Pointer 0 Register (10 bits) | 0000h |
| DPP1 | FE02h | 01h | CPU Data Page Pointer 1 Register (10 bits) | 0001h |
| DPP2 | FE04h | 02h | CPU Data Page Pointer 2 Register (10 bits) | 0002h |
| DPP3 | FE06h | 03h | CPU Data Page Pointer 3 Register (10 bits) | 0003h |
| EXICON b | F1C0h _E | E0h | External Interrupt Control Register | 0000h |
| MDC b | FF0Eh | 87h | CPU Multiply Divide Control Register | 0000h |
| MDH | FE0Ch | 06h | CPU Multiply Divide Register – High Word | 0000h |
| MDL | FE0Eh | 07h | CPU Multiply Divide Register – Low Word | 0000h |
| ODP2 b | F1C2h _E | E1h | Port 2 Open Drain Control Register | 0000h |
| ODP3 b | F1C6h _E | E3h | Port 3 Open Drain Control Register | 0000h |
| ODP6 b | F1CEh _E | E7h | Port 6 Open Drain Control Register | 00h |
| ONES | FF1Eh | 8Fh | Constant Value 1's Register (read only) | FFFFh |
| P0L b | FF00h | 80h | Port 0 Low Register (Lower half of PORT0) | 00h |
| P0H b | FF02h | 81h | Port 0 High Register (Upper half of PORT0) | 00h |
| P1L b | FF04h | 82h | Port 1 Low Register (Lower half of PORT1) | 00h |
| P1H b | FF06h | 83h | Port 1 High Register (Upper half of PORT1) | 00h |
| P2 b | FFC0h | E0h | Port 2 Register | 0000h |
| P3 b | FFC4h | E2h | Port 3 Register | 0000h |
| P4 b | FFC8h | E4h | Port 4 Register (8 bits) | 00h |
| P5 b | FFA2h | D1h | Port 5 Register (read only) | XXXXh |
| P6 b | FFCCh | E6h | Port 6 Register (8 bits) | 00h |
| PECC0 | FEC0h | 60h | PEC Channel 0 Control Register | 0000h |

Special Function Register Overview (Cont'd)

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|------------|--------------------|---------------|---|-------------|
| PECC1 | FEC2h | 61h | PEC Channel 1 Control Register | 0000h |
| PECC2 | FEC4h | 62h | PEC Channel 2 Control Register | 0000h |
| PECC3 | FEC6h | 63h | PEC Channel 3 Control Register | 0000h |
| PECC4 | FEC8h | 64h | PEC Channel 4 Control Register | 0000h |
| PECC5 | FECAh | 65h | PEC Channel 5 Control Register | 0000h |
| PECC6 | FECCh | 66h | PEC Channel 6 Control Register | 0000h |
| PECC7 | FECEh | 67h | PEC Channel 7 Control Register | 0000h |
| PSW b | FF10h | 88h | CPU Program Status Word | 0000h |
| RP0H b | F108h _E | 84h | System Start-up Configuration Register (Rd. only) | XXh |
| S0BG | FEB4h | 5Ah | Serial Channel 0 Baud Rate Generator Reload Register | 0000h |
| S0CON b | FFB0h | D8h | Serial Channel 0 Control Register | 0000h |
| S0EIC b | FF70h | B8h | Serial Channel 0 Error Interrupt Control Register | 0000h |
| S0RBUF | FEB2h | 59h | Serial Channel 0 Receive Buffer Register (read only) | XXh |
| S0RIC b | FF6Eh | B7h | Serial Channel 0 Receive Interrupt Control Register | 0000h |
| S0TBIC b | F19Ch _E | CEh | Serial Channel 0 Transmit Buffer Interrupt Control Register | 0000h |
| S0TBUF | FEB0h | 58h | Serial Channel 0 Transmit Buffer Register (write only) | 00h |
| S0TIC b | FF6Ch | B6h | Serial Channel 0 Transmit Interrupt Control Register | 0000h |
| SP | FE12h | 09h | CPU System Stack Pointer Register | FC00h |
| SSCBR | F0B4h _E | 5Ah | SSC Baudrate Register | 0000h |
| SSCCON b | FFB2h | D9h | SSC Control Register | 0000h |
| SSCEIC b | FF76h | BBh | SSC Error Interrupt Control Register | 0000h |
| SSCRB | F0B2h _E | 59h | SSC Receive Buffer (read only) | XXXXh |
| SSCRIC b | FF74h | BAh | SSC Receive Interrupt Control Register | 0000h |
| SSCTB | F0B0h _E | 58h | SSC Transmit Buffer (write only) | 0000h |
| SSCTIC b | FF72h | B9h | SSC Transmit Interrupt Control Register | 0000h |
| STKOV | FE14h | 0Ah | CPU Stack Overflow Pointer Register | FA00h |
| STKUN | FE16h | 0Bh | CPU Stack Underflow Pointer Register | FC00h |
| SYSCON b | FF12h | 89h | CPU System Configuration Register | 0xx0h*) |
| T2 | FE40h | 20h | GPT1 Timer 2 Register | 0000h |
| T2CON b | FF40h | A0h | GPT1 Timer 2 Control Register | 0000h |

Special Function Register Overview (Cont'd)

| Name | Physical Address | 8-Bit Address | Description | Reset Value |
|------------|--------------------|---------------|---|-------------|
| T2IC b | FF60h | B0h | GPT1 Timer 2 Interrupt Control Register | 0000h |
| T3 | FE42h | 21h | GPT1 Timer 3 Register | 0000h |
| T3CON b | FF42h | A1h | GPT1 Timer 3 Control Register | 0000h |
| T3IC b | FF62h | B1h | GPT1 Timer 3 Interrupt Control Register | 0000h |
| T4 | FE44h | 22h | GPT1 Timer 4 Register | 0000h |
| T4CON b | FF44h | A2h | GPT1 Timer 4 Control Register | 0000h |
| T4IC b | FF64h | B2h | GPT1 Timer 4 Interrupt Control Register | 0000h |
| T5 | FE46h | 23h | GPT2 Timer 5 Register | 0000h |
| T5CON b | FF46h | A3h | GPT2 Timer 5 Control Register | 0000h |
| T5IC b | FF66h | B3h | GPT2 Timer 5 Interrupt Control Register | 0000h |
| T6 | FE48h | 24h | GPT2 Timer 6 Register | 0000h |
| T6CON b | FF48h | A4h | GPT2 Timer 6 Control Register | 0000h |
| T6IC b | FF68h | B4h | GPT2 Timer 6 Interrupt Control Register | 0000h |
| TFR b | FFACh | D6h | Trap Flag Register | 0000h |
| WDT | FEAEh | 57h | Watchdog Timer Register (read only) | 0000h |
| WDTCON | FFAEh | D7h | Watchdog Timer Control Register | 0000h |
| XP0IC b | F186h _E | C3h | X-Peripheral 0 Interrupt Control Register | 0000h |
| XP1IC b | F18Eh _E | C7h | X-Peripheral 1 Interrupt Control Register | 0000h |
| XP2IC b | F196h _E | CBh | X-Peripheral 2 Interrupt Control Register | 0000h |
| XP3IC b | F19Eh _E | CFh | X-Peripheral 3 Interrupt Control Register | 0000h |
| ZEROS b | FF1Ch | 8Eh | Constant Value 0's Register (read only) | 0000h |

*) The system configuration is selected during reset.

Note: The Interrupt Control Registers XPNIC are prepared to control interrupt requests from integrated X-Bus peripherals. Nodes, where no X-Peripherals are connected, may be used to generate software controlled interrupt requests by setting the respective XPNIR bit.

13 ELECTRICAL CHARACTERISTICS

13.1 Absolute Maximum Ratings

- Ambient temperature under bias (T_A): 0 to +70 °C
- Storage temperature (T_{ST}): – 65 to +150 °C
- Voltage on V_{DD} pins with respect to ground (V_{SS}): 0.5 to +6.5 V
- Voltage on any pin with respect to ground (V_{SS}): –0.5 to $V_{DD} + 0.5$ V
- Input current on any pin during overload condition: –10 to +10 mA
- Absolute sum of all input currents during overload condition: |100 mA|
- Power dissipation: 1.5 W

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the values defined by the Absolute Maximum Ratings.

13.2 Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the ST10R165 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (Controller Characteristics):

The logic of the ST10R165 will provide signals with the respective timing characteristics.

SR (System Requirement):

The external system must provide signals with the respective timing characteristics to the ST10R165.

13.3 DC Characteristics

$V_{DD} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$; $f_{CPU} = 20\text{ MHz}$; Reset active. $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$

| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|--|--------------------------|---------------------|--------------------|---------------|---|
| | | min. | max. | | |
| Input low voltage | V_{IL} SR | -0.5 | $0.2 V_{DD} - 0.1$ | V | — |
| Input high voltage (all except \overline{RSTIN} and XTAL1) | V_{IH} SR | $0.2 V_{DD} + 0.9$ | $V_{DD} + 0.5$ | V | — |
| Input high voltage \overline{RSTIN} | V_{IH1} SR | $0.6 V_{DD}$ | $V_{DD} + 0.5$ | V | — |
| Input high voltage XTAL1 | V_{IH2} SR | $0.7 V_{DD}$ | $V_{DD} + 0.5$ | V | — |
| Output low voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , BHE, CLKOUT, \overline{RSTOUT}) | V_{OL} CC | — | 0.45 | V | $I_{OL} = 2.4\text{ mA}$ |
| Output low voltage (all other outputs) | V_{OL1} CC | — | 0.45 | V | $I_{OL1} = 1.6\text{ mA}$ |
| Output high voltage (PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , BHE, CLKOUT, \overline{RSTOUT}) | V_{OH} CC | $0.9 V_{DD}$ 2.4 | — | V | $I_{OH} = -500\text{ }\mu\text{A}$ $I_{OH} = -2.4\text{ mA}$ |
| Output high voltage ¹⁾ (all other outputs) | V_{OH1} CC | $0.9 V_{DD}$ 2.4 | — | V V | $I_{OH} = -250\text{ }\mu\text{A}$ $I_{OH} = -1.6\text{ mA}$ |
| Input leakage current (Port 5) | I_{OZ1} CC | — | ± 200 | nA | $0\text{ V} < V_{IN} < V_{DD}$ |
| Input leakage current (all other) | I_{OZ2} CC | — | ± 500 | nA | $0\text{ V} < V_{IN} < V_{DD}$ |
| \overline{RSTIN} pull-up resistor | R_{RST} CC | 50 | 150 | k Ω | — |
| Read/Write inactive current ⁴⁾ | I_{RWH} ²⁾ | — | -40 | μA | $V_{OUT} = 2.4\text{ V}$ |
| Read/Write active current ⁴⁾ | I_{RWL} ³⁾ | -500 | — | μA | $V_{OUT} = V_{OLmax}$ |
| ALE inactive current ⁴⁾ | I_{ALEL} ²⁾ | — | 40 | μA | $V_{OUT} = V_{OLmax}$ |
| ALE active current ⁴⁾ | I_{ALEH} ³⁾ | 500 | — | μA | $V_{OUT} = 2.4\text{ V}$ |
| Port 6 inactive current ⁴⁾ | I_{P6H} ²⁾ | — | -40 | μA | $V_{OUT} = 2.4\text{ V}$ |
| Port 6 active current ⁴⁾ | I_{P6L} ³⁾ | -500 | — | μA | $V_{OUT} = V_{OL1max}$ |

DC Characteristics (Cont'd)

$V_{DD} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$; $f_{CPU} = 20\text{ MHz}$; Reset active. $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$

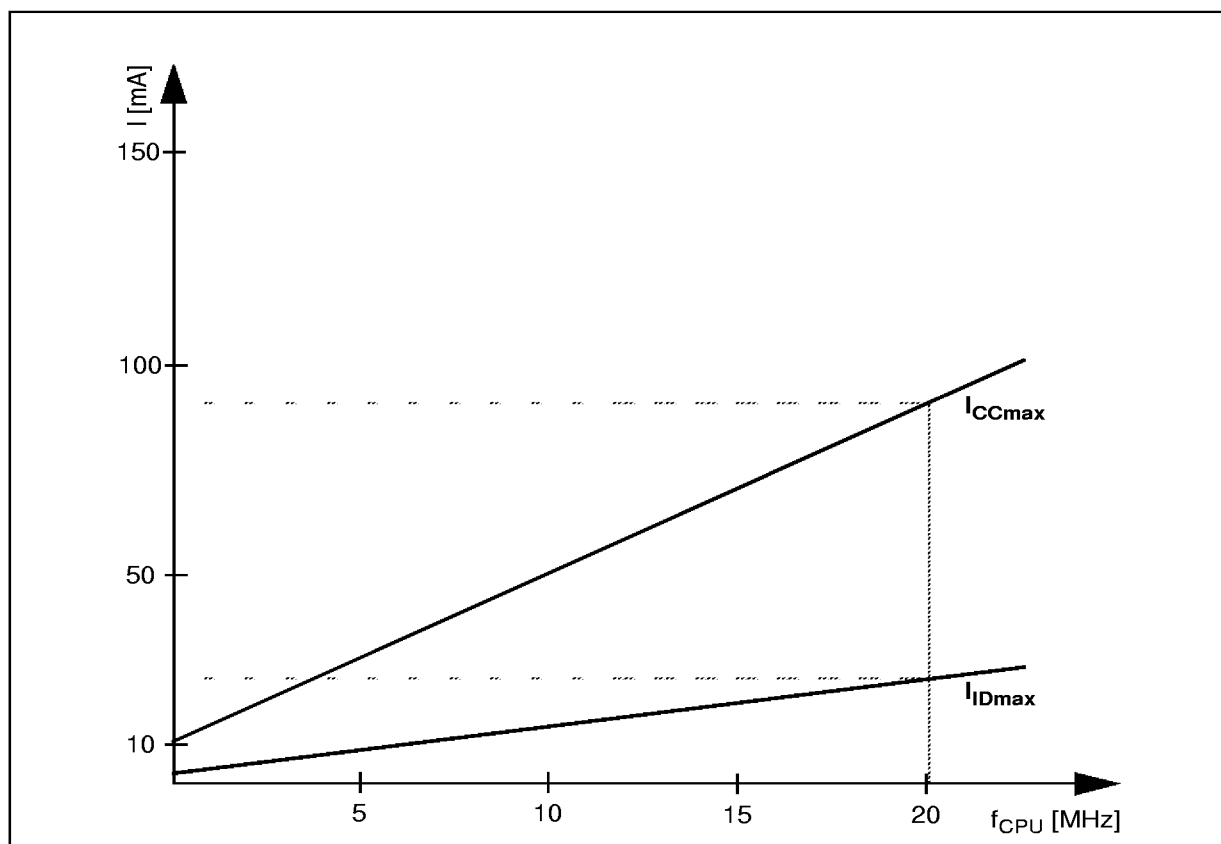
| Parameter | Symbol | Limit Values | | Unit | Test Condition |
|---|-------------------------|--------------|---------------------|---------------|--|
| | | min. | max. | | |
| PORT0 configuration current ⁴⁾ | I_{POH} ²⁾ | — | -10 | μA | $V_{IN} = V_{IHmin}$ |
| | I_{POL} ³⁾ | -100 | — | μA | $V_{IN} = V_{ILmax}$ |
| XTAL1 input current | I_{IL} CC | — | ± 20 | μA | $0\text{ V} < V_{IN} < V_{DD}$ |
| Pin capacitance ⁵⁾ (digital inputs/outputs) | C_{IO} CC | — | 10 | pF | $f = 1\text{ MHz}$ $T_A = 25\text{ }^{\circ}\text{C}$ |
| Power supply current | I_{CC} | — | $10 + 4 * f_{CPU}$ | mA | $\overline{RSTIN} = V_{IL2}$ f_{CPU} in [MHz] ⁶⁾ |
| Idle mode supply current | I_{ID} | — | $2 + 1.2 * f_{CPU}$ | mA | $\overline{RSTIN} = V_{IH1}$ f_{CPU} in [MHz] ⁶⁾ |
| Power-down mode supply current | I_{PD} | — | 100 | μA | $V_{DD} = 5.5\text{ V}$ ⁷⁾ |

Notes:

- 1) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.
- 2) The maximum current may be drawn while the respective signal line remains inactive.
- 3) The minimum current must be drawn in order to drive the respective signal line active.
- 4) This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for \overline{CS} output and the open drain function is not enabled.
- 5) Not 100% tested, guaranteed by design characterization.
- 6) The supply current is a function of the operating frequency. This dependency is illustrated in the figure below.
These parameters are tested at V_{DDmax} and 20 MHz CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH} .
- 7) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at $V_{DD} - 0.1\text{ V}$ to V_{DD} , $V_{REF} = 0\text{ V}$, all outputs (including pins configured as outputs) disconnected.

DC Characteristics (Cont'd)

Figure 8. Supply/Idle Current as a Function of Operating Frequency



13.4 Testing Waveforms

Figure 9. Input Output Waveforms

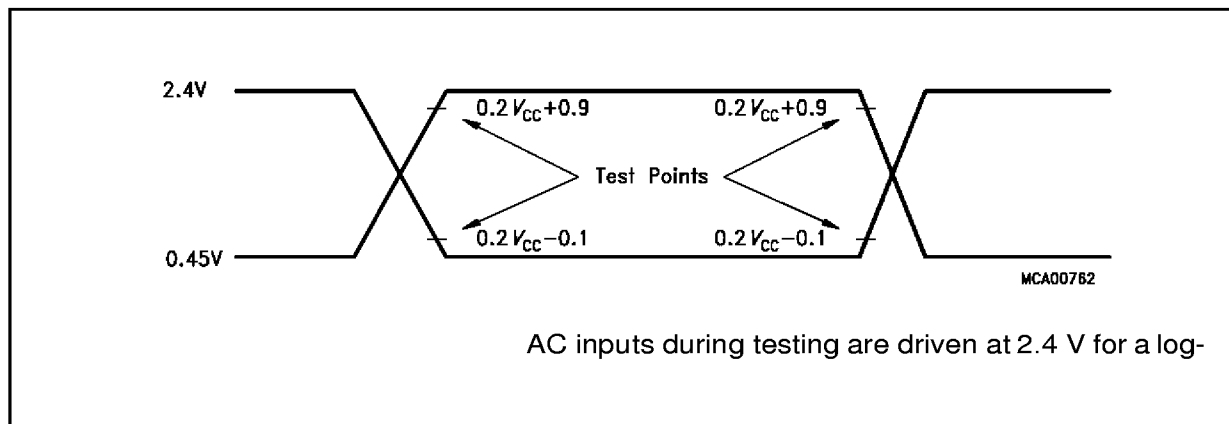
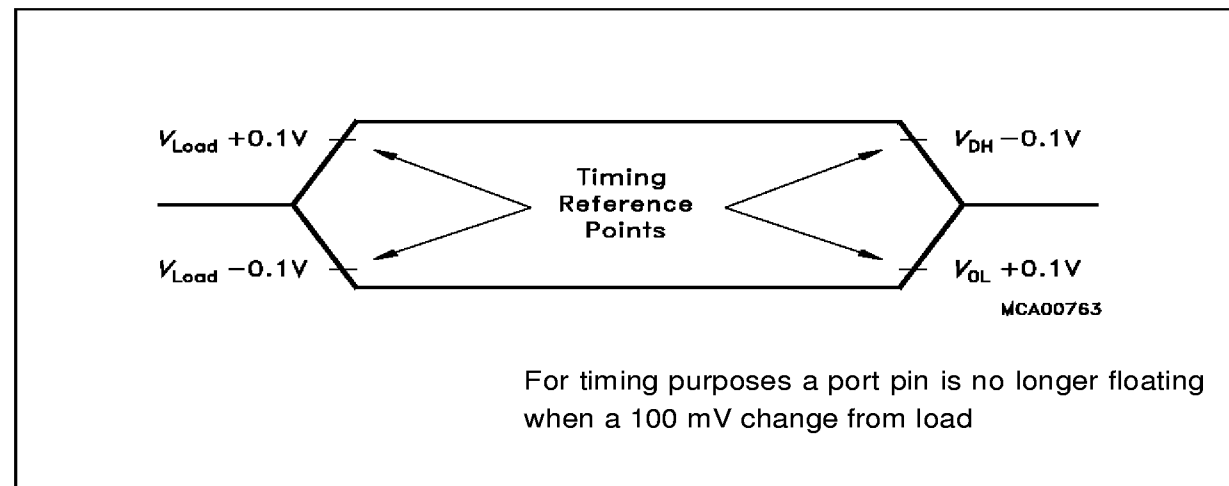


Figure 10. Float Waveforms



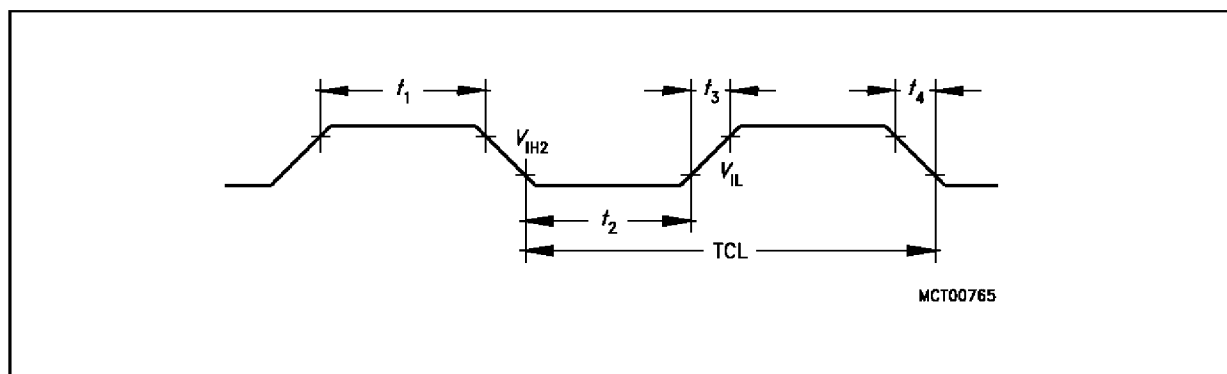
13.5 AC Characteristics

External Clock Drive XTAL1

$V_{DD} = 5\text{ V} \pm 10\%$; $V_{SS} = 0\text{ V}$ $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|-------------------|----------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| Oscillator period | TCL SR | 25 | 25 | 25 | 500 | ns |
| High time | t_1 SR | 6 | — | 6 | — | ns |
| Low time | t_2 SR | 6 | — | 6 | — | ns |
| Rise time | t_3 SR | — | 5 | — | 5 | ns |
| Fall time | t_4 SR | — | 5 | — | 5 | ns |

Figure 11. External Clock Drive XTAL1



13.5.1 Memory Cycle Variables

The timing tables below use three variables which are derived from the BUSCONx registers and represent the special characteristics of the programmed memory cycle. The following table describes, how these variables are to be computed.

| Description | Symbol | Values |
|------------------------------|--------|--------------------------------------|
| ALE Extension | t_A | $TCL * \langle ALECTL \rangle$ |
| Memory Cycle Time Waitstates | t_C | $2TCL * (15 - \langle MCTC \rangle)$ |
| Memory Tristate Time | t_F | $2TCL * (1 - \langle MTTC \rangle)$ |

13.5.2 Multiplexed Bus

 $V_{DD} = 5\text{ V} \pm 10\%; V_{SS} = 0\text{ V}$
 $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$
 C_L (for PORT0, PORT1, Port 4, ALE, \overline{RD} , \overline{WR} , \overline{BHE} , CLKOUT) = 100 pF

 C_L (for Port 6, \overline{CS}) = 100 pF

 ALE cycle time = $6\text{ TCL} + 2t_A + t_C + t_F$ (150 ns at 20-MHz CPU clock without waitstates)

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|-------------------|--|---------------------------------|------|
| | | min. | max. | min. | max. | |
| ALE high time | t_5 CC | $15 + t_A$ | — | $\text{TCL} - 10 + t_A$ | — | ns |
| Address setup to ALE | t_6 CC | $10 + t_A$ | — | $\text{TCL} - 15 + t_A$ | — | ns |
| Address hold after ALE | t_7 CC | $15 + t_A$ | — | $\text{TCL} - 10 + t_A$ | — | ns |
| ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay) | t_8 CC | $15 + t_A$ | — | $\text{TCL} - 10 + t_A$ | — | ns |
| ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay) | t_9 CC | $-10 + t_A$ | — | $-10 + t_A$ | — | ns |
| Address float after \overline{RD} , \overline{WR} (with RW-delay) | t_{10} CC | — | 5 | — | 5 | ns |
| Address float after \overline{RD} , \overline{WR} (no RW-delay) | t_{11} CC | — | 30 | — | $\text{TCL} + 5$ | ns |
| \overline{RD} , \overline{WR} low time (with RW-delay) | t_{12} CC | $40 + t_C$ | — | $2\text{TCL} - 10 + t_C$ | — | ns |
| \overline{RD} , \overline{WR} low time (no RW-delay) | t_{13} CC | $65 + t_C$ | — | $3\text{TCL} - 10 + t_C$ | — | ns |
| \overline{RD} to valid data in (with RW-delay) | t_{14} SR | — | $30 + t_C$ | — | $2\text{TCL} - 20 + t_C$ | ns |
| \overline{RD} to valid data in (no RW-delay) | t_{15} SR | — | $55 + t_C$ | — | $3\text{TCL} - 20 + t_C$ | ns |
| ALE low to valid data in | t_{16} SR | — | $55 + t_A + t_C$ | — | $3\text{TCL} - 20 + t_A + t_C$ | ns |
| Address to valid data in | t_{17} SR | — | $70 + 2t_A + t_C$ | — | $4\text{TCL} - 30 + 2t_A + t_C$ | ns |
| Data hold after \overline{RD} rising edge | t_{18} SR | 0 | — | 0 | — | ns |
| Data float after \overline{RD} | t_{19} SR | — | $35 + t_F$ | — | $2\text{TCL} - 15 + t_F$ | ns |
| Data valid to \overline{WR} | t_{22} SR | $35 + t_C$ | — | $2\text{TCL} - 15 + t_C$ | — | ns |
| Data hold after \overline{WR} | t_{23} CC | $35 + t_F$ | — | $2\text{TCL} - 15 + t_F$ | — | ns |
| ALE rising edge after \overline{RD} , \overline{WR} | t_{25} CC | $35 + t_F$ | — | $2\text{TCL} - 15 + t_F$ | — | ns |

Multiplexed Bus (Cont'd)

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|---|-------------|----------------------------|-------------------|--|--------------------------|------|
| | | min. | max. | min. | max. | |
| Address hold after \overline{RD} , \overline{WR} | t_{27} CC | $35 + t_F$ | — | $2TCL - 15 + t_F$ | — | ns |
| ALE falling edge to \overline{CS} | t_{38} CC | $-5 - t_A$ | $10 - t_A$ | $-5 - t_A$ | $10 - t_A$ | ns |
| \overline{CS} low to Valid Data In | t_{39} SR | — | $55 + t_C + 2t_A$ | — | $3TCL - 20 + t_C + 2t_A$ | ns |
| \overline{CS} hold after \overline{RD} , \overline{WR} | t_{40} CC | $60 + t_F$ | — | $3TCL - 15 + t_F$ | — | ns |
| ALE fall. edge to \overline{RdCS} , \overline{WrCS} (with RW delay) | t_{42} CC | $20 + t_A$ | — | $TCL - 5 + t_A$ | — | ns |
| ALE fall. edge to \overline{RdCS} , \overline{WrCS} (no RW delay) | t_{43} CC | $-5 + t_A$ | — | $-5 + t_A$ | — | ns |
| Address float after \overline{RdCS} , \overline{WrCS} (with RW delay) | t_{44} CC | — | 0 | — | 0 | ns |
| Address float after \overline{RdCS} , \overline{WrCS} (no RW delay) | t_{45} CC | — | 25 | — | TCL | ns |
| \overline{RdCS} to Valid Data In (with RW delay) | t_{46} SR | — | $25 + t_C$ | — | $2TCL - 25 + t_C$ | ns |
| \overline{RdCS} to Valid Data In (no RW delay) | t_{47} SR | — | $50 + t_C$ | — | $3TCL - 25 + t_C$ | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (with RW delay) | t_{48} CC | $40 + t_C$ | — | $2TCL - 10 + t_C$ | — | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (no RW delay) | t_{49} CC | $65 + t_C$ | — | $3TCL - 10 + t_C$ | — | ns |
| Data valid to \overline{WrCS} | t_{50} CC | $35 + t_C$ | — | $2TCL - 15 + t_C$ | — | ns |
| Data hold after \overline{RdCS} | t_{51} SR | 0 | — | 0 | — | ns |
| Data float after \overline{RdCS} | t_{52} SR | — | $30 + t_F$ | — | $2TCL - 20 + t_F$ | ns |
| Address hold after \overline{RdCS} , \overline{WrCS} | t_{54} CC | $30 + t_F$ | — | $2TCL - 20 + t_F$ | — | ns |
| Data hold after \overline{WrCS} | t_{56} CC | $30 + t_F$ | — | $2TCL - 20 + t_F$ | — | ns |

Figure 12. External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Normal ALE

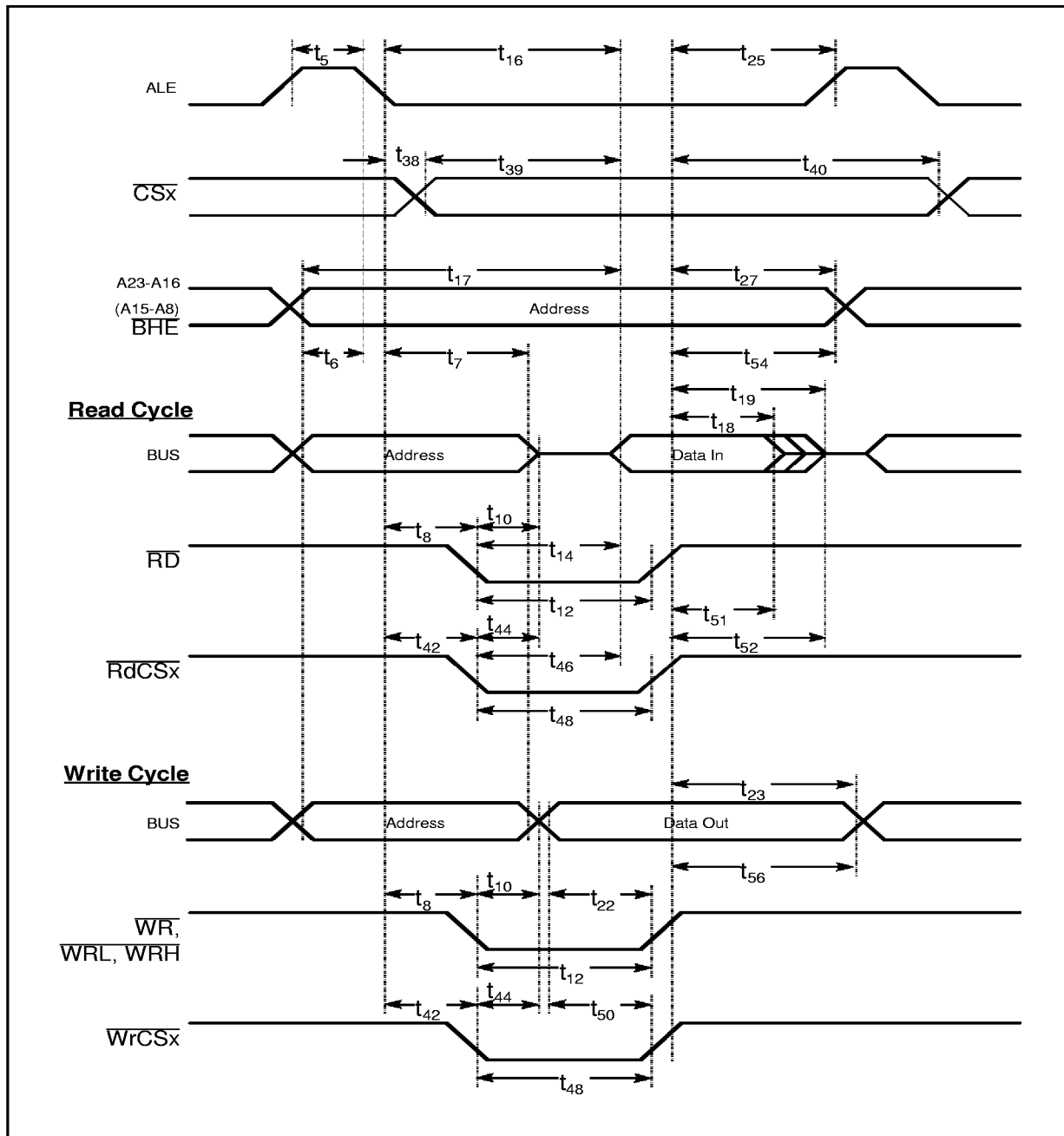


Figure 13. External Memory Cycle: Multiplexed Bus, With Read/Write Delay, Extended ALE

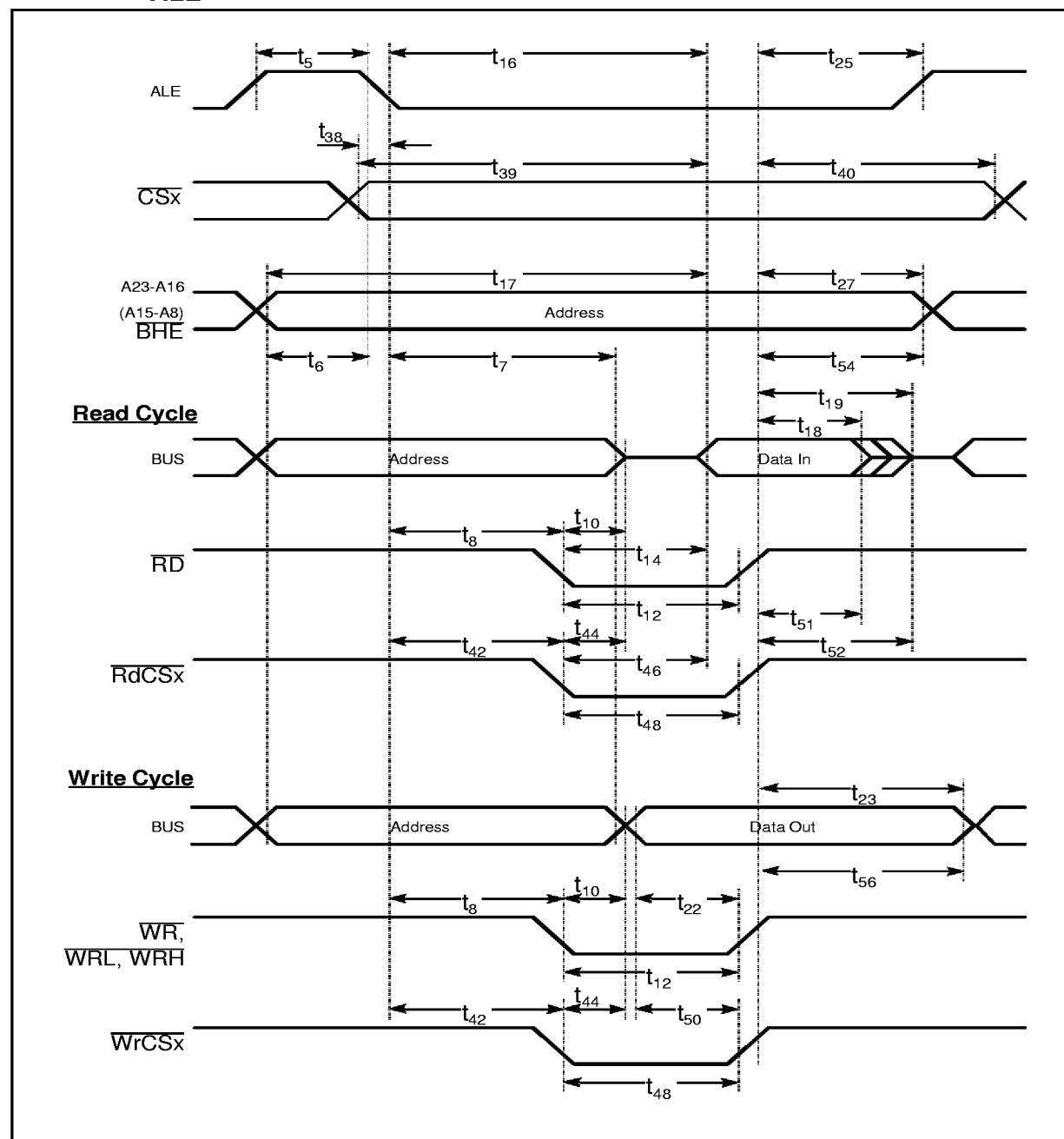


Figure 14. External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Normal ALE

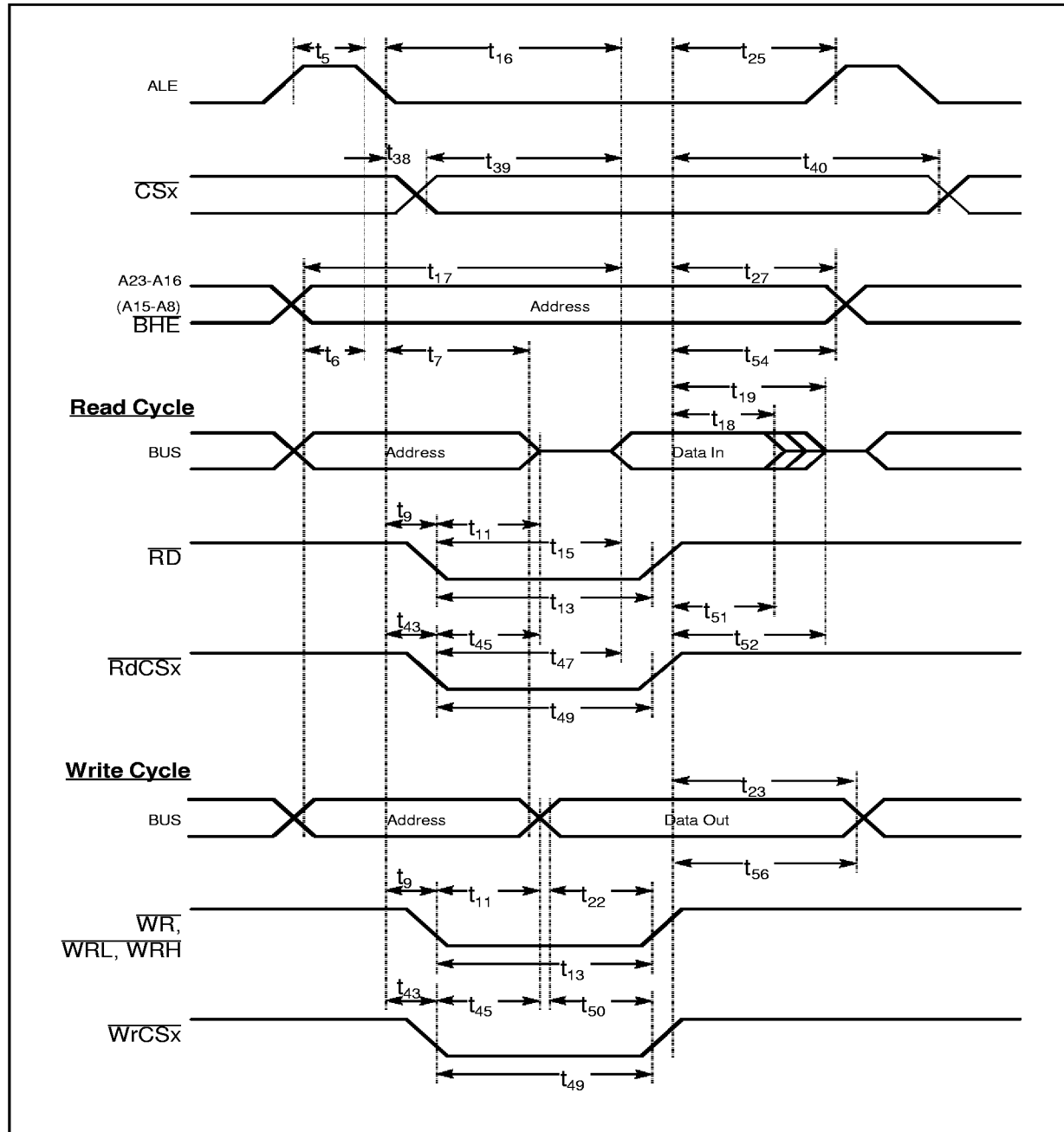
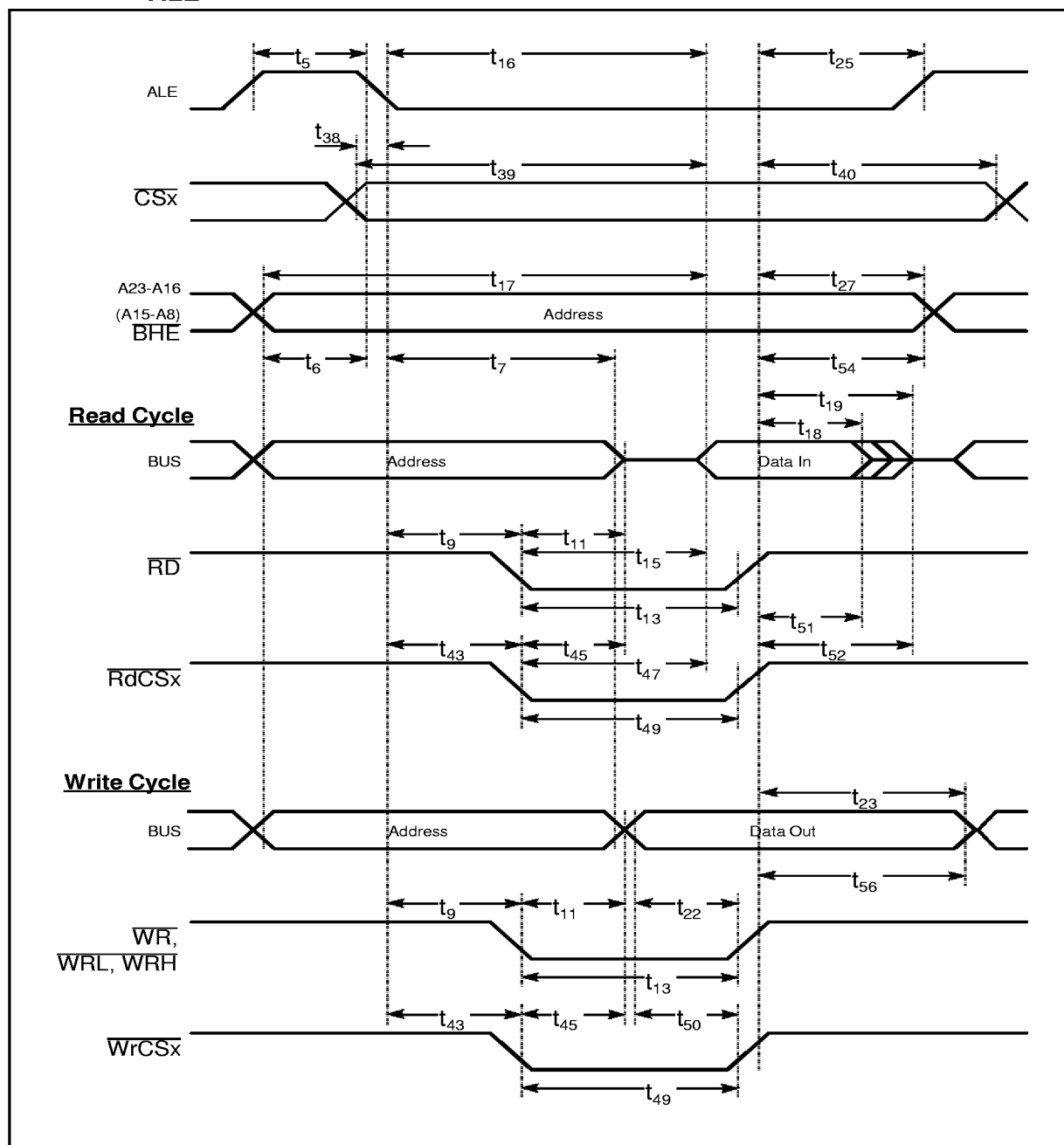


Figure 15. External Memory Cycle: Multiplexed Bus, No Read/Write Delay, Extended ALE



13.5.2.1 Demultiplexed Bus

$$V_{DD} = 5\text{ V} \pm 10\%; V_{SS} = 0\text{ V}$$

$$T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$$

$$C_L\text{ (for PORT0, PORT1, Port 4, ALE, } \overline{RD}, \overline{WR}, \overline{BHE}, \text{CLKOUT)} = 100\text{ pF}$$

$$C_L\text{ (for Port 6, } \overline{CS}) = 100\text{ pF}$$

$$\text{ALE cycle time} = 4\text{ TCL} + 2t_A + t_C + t_F\text{ (100 ns at 20 MHz CPU clock without waitstates)}$$

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|-------------------|--|---------------------------------|------|
| | | min. | max. | min. | max. | |
| ALE high time | t_5 CC | $15 + t_A$ | — | $\text{TCL} - 10 + t_A$ | — | ns |
| Address setup to ALE | t_6 CC | $10 + t_A$ | — | $\text{TCL} - 15 + t_A$ | — | ns |
| ALE falling edge to \overline{RD} , \overline{WR} (with RW-delay) | t_8 CC | $15 + t_A$ | — | $\text{TCL} - 10 + t_A$ | — | ns |
| ALE falling edge to \overline{RD} , \overline{WR} (no RW-delay) | t_9 CC | $-10 + t_A$ | — | $-10 + t_A$ | — | ns |
| \overline{RD} , \overline{WR} low time (with RW-delay) | t_{12} CC | $40 + t_C$ | — | $2\text{TCL} - 10 + t_C$ | — | ns |
| \overline{RD} , \overline{WR} low time (no RW-delay) | t_{13} CC | $65 + t_C$ | — | $3\text{TCL} - 10 + t_C$ | — | ns |
| \overline{RD} to valid data in (with RW-delay) | t_{14} SR | — | $30 + t_C$ | — | $2\text{TCL} - 20 + t_C$ | ns |
| \overline{RD} to valid data in (no RW-delay) | t_{15} SR | — | $55 + t_C$ | — | $3\text{TCL} - 20 + t_C$ | ns |
| ALE low to valid data in | t_{16} SR | — | $55 + t_A + t_C$ | — | $3\text{TCL} - 20 + t_A + t_C$ | ns |
| Address to valid data in | t_{17} SR | — | $70 + 2t_A + t_C$ | — | $4\text{TCL} - 30 + 2t_A + t_C$ | ns |
| Data hold after \overline{RD} rising edge | t_{18} SR | 0 | — | 0 | — | ns |
| Data float after \overline{RD} rising edge (with RW-delay) | t_{20} SR | — | $35 + t_F$ | — | $2\text{TCL} - 15 + t_F$ | ns |
| Data float after \overline{RD} rising edge (no RW-delay) | t_{21} SR | — | $15 + t_F$ | — | $\text{TCL} - 10 + t_F$ | ns |
| Data valid to \overline{WR} | t_{22} CC | $35 + t_C$ | — | $2\text{TCL} - 15 + t_C$ | — | ns |
| Data hold after \overline{WR} | t_{24} CC | $15 + t_F$ | — | $\text{TCL} - 10 + t_F$ | — | ns |
| ALE rising edge after \overline{RD} , \overline{WR} | t_{26} CC | $-10 + t_F$ | — | $-10 + t_F$ | — | ns |

Demultiplexed Bus (Cont'd)

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|---|-------------|----------------------------|-------------------|--|--------------------------|------|
| | | min. | max. | min. | max. | |
| Address hold after \overline{RD} , \overline{WR} | t_{28} CC | $0 + t_F$ | — | $0 + t_F$ | — | ns |
| ALE falling edge to \overline{CS} | t_{38} CC | $-5 - t_A$ | $10 - t_A$ | $-5 - t_A$ | $10 - t_A$ | ns |
| \overline{CS} low to Valid Data In | t_{39} SR | — | $55 + t_C + 2t_A$ | — | $3TCL - 20 + t_C + 2t_A$ | ns |
| \overline{CS} hold after \overline{RD} , \overline{WR} | t_{41} CC | $10 + t_F$ | — | $TCL - 15 + t_F$ | — | ns |
| ALE falling edge to \overline{RdCS} , \overline{WrCS} (with RW-delay) | t_{42} CC | $20 + t_A$ | — | $TCL - 5 + t_A$ | — | ns |
| ALE falling edge to \overline{RdCS} , \overline{WrCS} (no RW-delay) | t_{43} CC | $-5 + t_A$ | — | $-5 + t_A$ | — | ns |
| \overline{RdCS} to Valid Data In (with RW-delay) | t_{46} SR | — | $25 + t_C$ | — | $2TCL - 25 + t_C$ | ns |
| \overline{RdCS} to Valid Data In (no RW-delay) | t_{47} SR | — | $50 + t_C$ | — | $3TCL - 25 + t_C$ | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (with RW-delay) | t_{48} CC | $40 + t_C$ | — | $2TCL - 10 + t_C$ | — | ns |
| \overline{RdCS} , \overline{WrCS} Low Time (no RW-delay) | t_{49} CC | $65 + t_C$ | — | $3TCL - 10 + t_C$ | — | ns |
| Data valid to \overline{WrCS} | t_{50} CC | $35 + t_C$ | — | $2TCL - 15 + t_C$ | — | ns |
| Data hold after \overline{RdCS} | t_{51} SR | 0 | — | 0 | — | ns |
| Data float after \overline{RdCS} (with RW-delay) | t_{53} SR | — | $30 + t_F$ | — | $2TCL - 20 + t_F$ | ns |
| Data float after \overline{RdCS} (no RW-delay) | t_{68} SR | — | $5 + t_F$ | — | $TCL - 20 + t_F$ | ns |
| Address hold after \overline{RdCS} , \overline{WrCS} | t_{55} CC | $-5 + t_F$ | — | $-5 + t_F$ | — | ns |
| Data hold after \overline{WrCS} | t_{57} CC | $10 + t_F$ | — | $TCL - 15 + t_F$ | — | ns |

Figure 16. External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Normal ALE

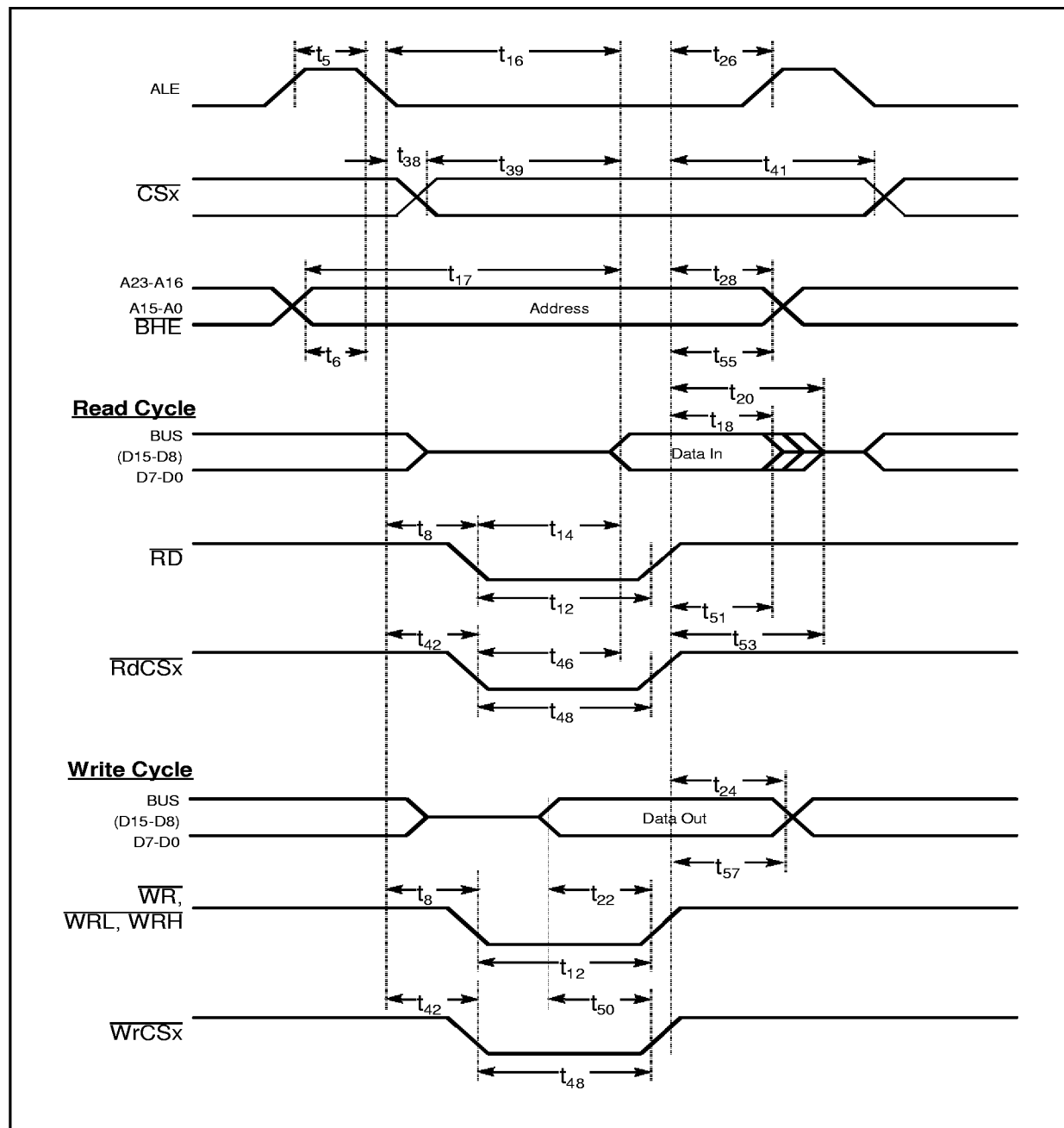


Figure 17. External Memory Cycle: Demultiplexed Bus, With Read/Write Delay, Extended ALE

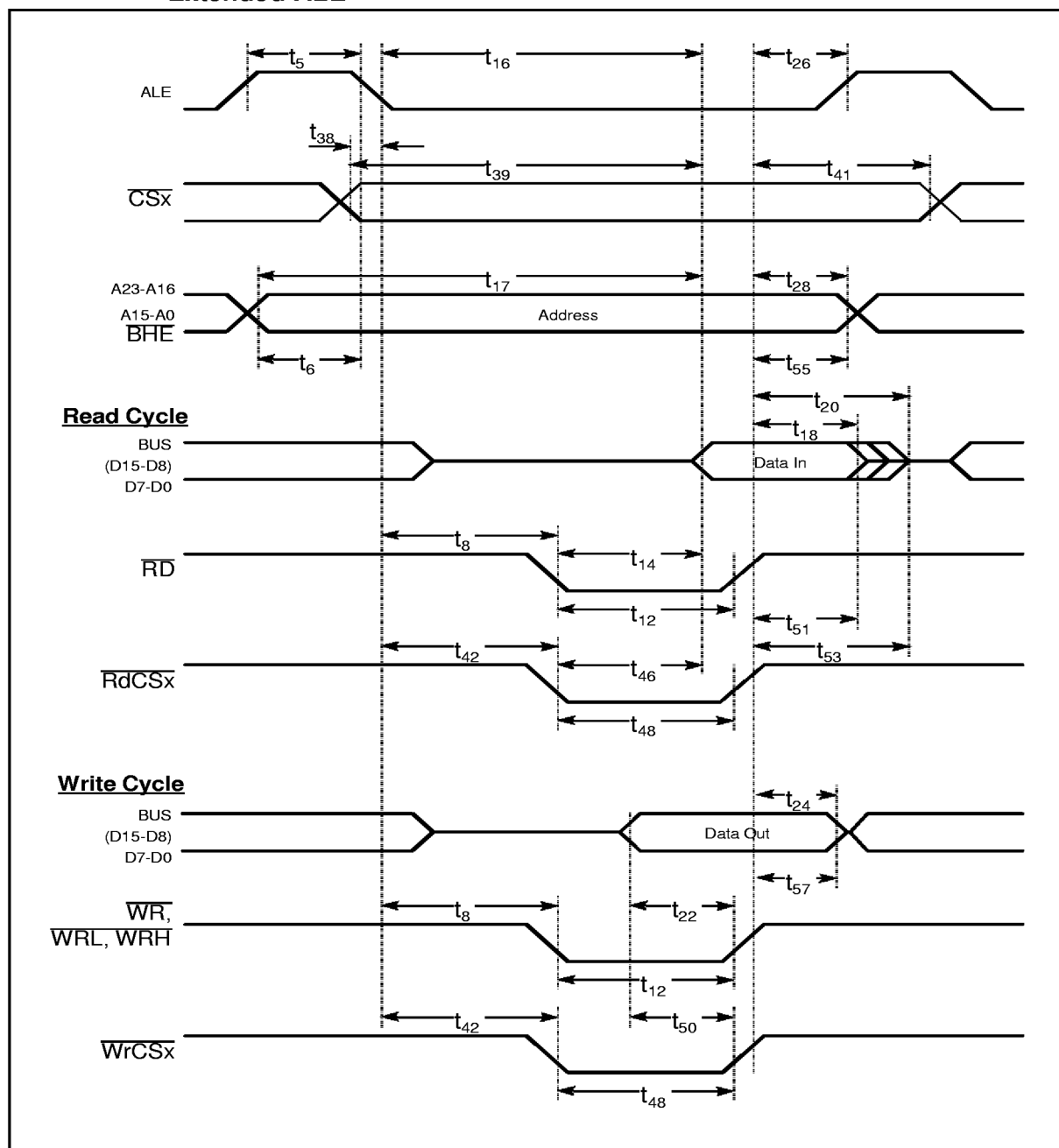


Figure 18. External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Normal ALE

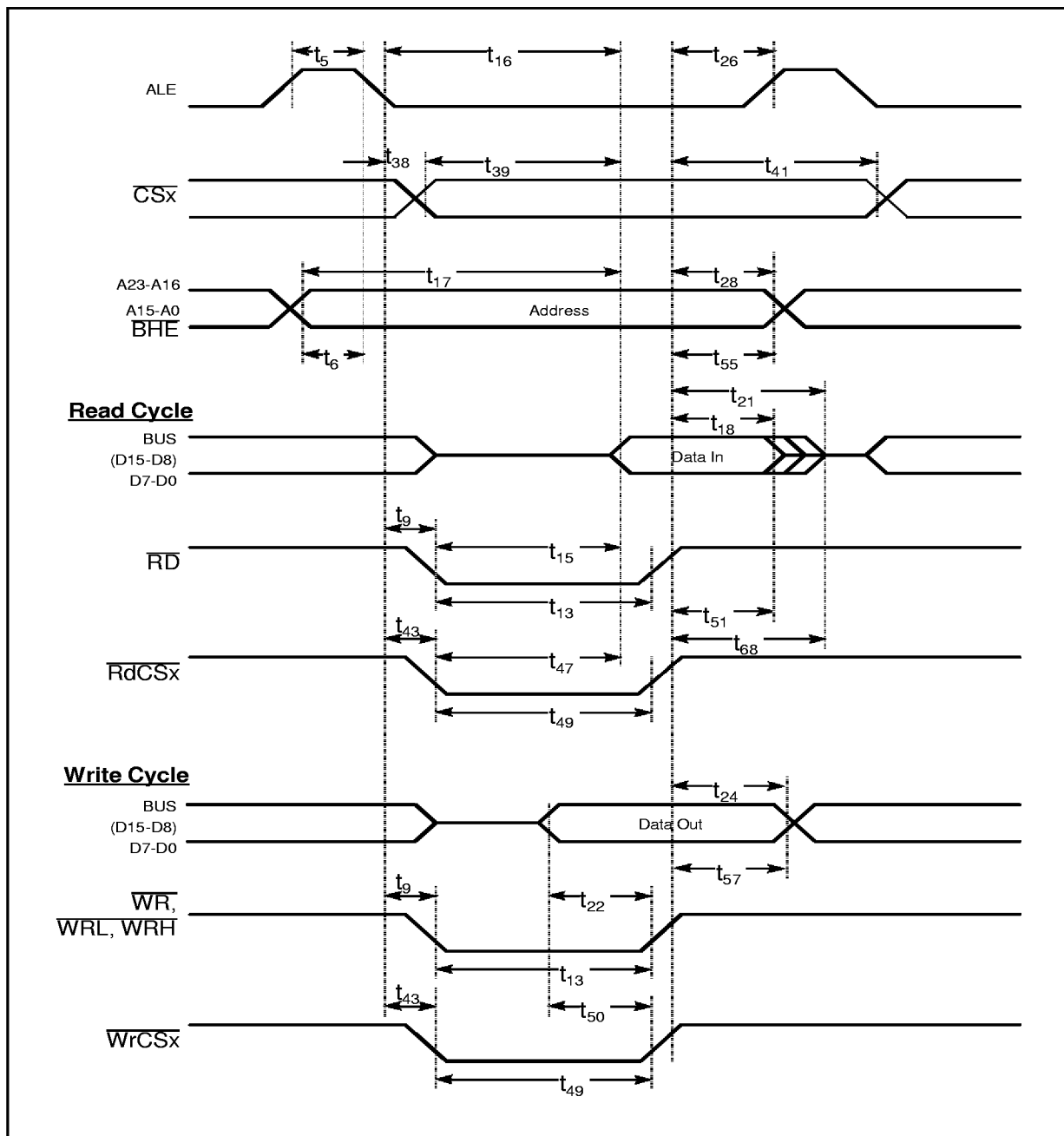
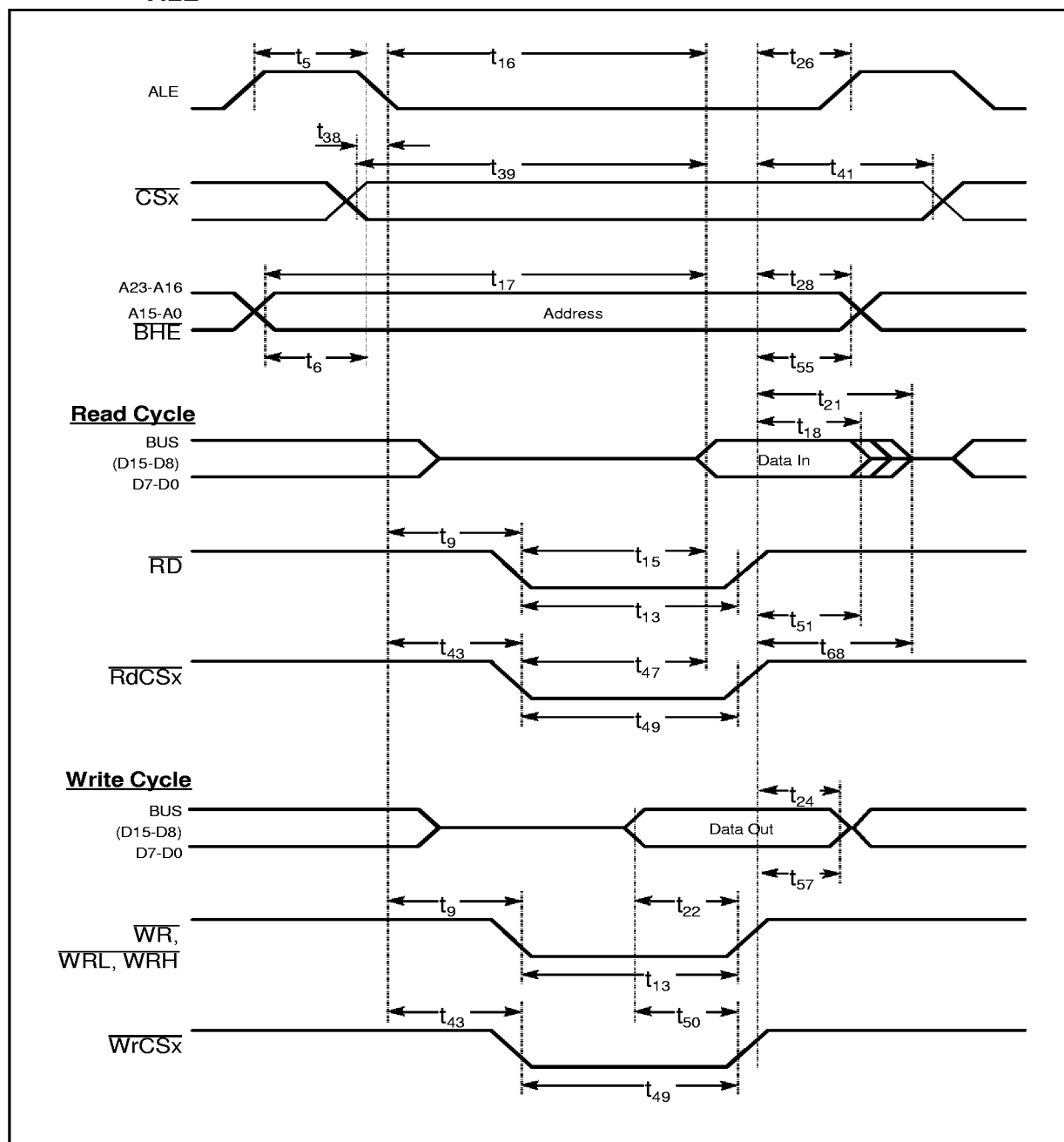


Figure 19. External Memory Cycle: Demultiplexed Bus, No Read/Write Delay, Extended ALE

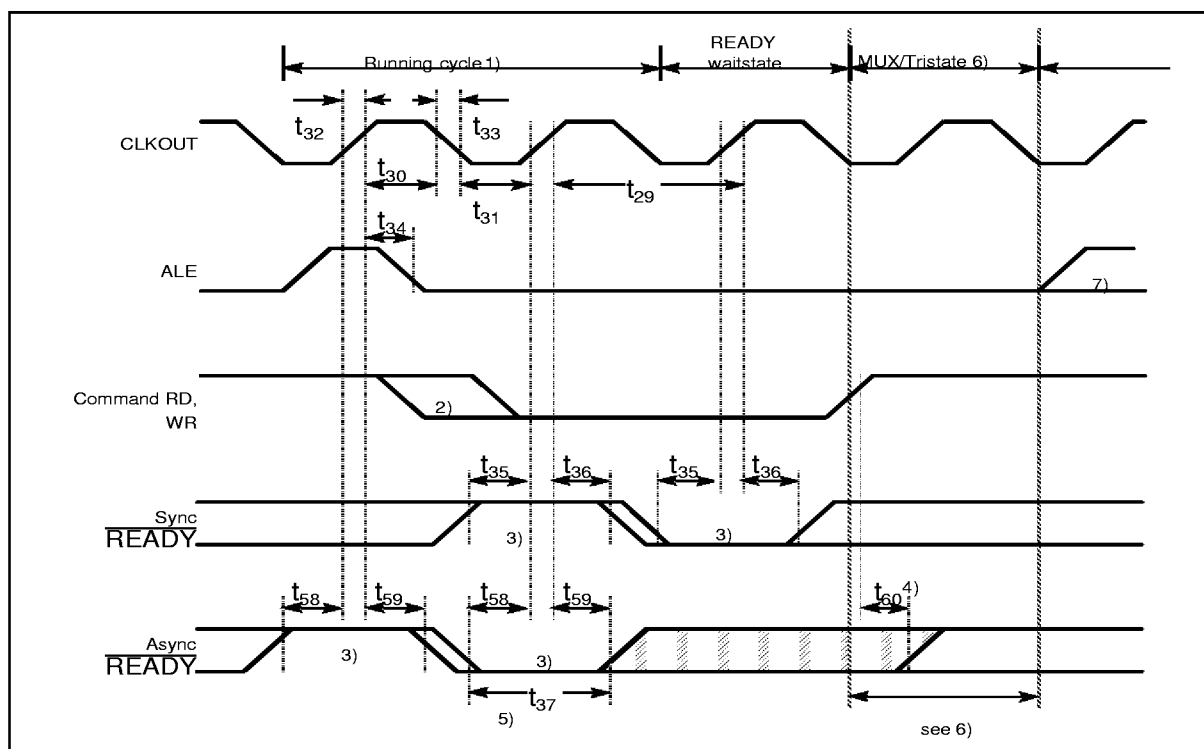


AC Characteristics (Cont'd)CLKOUT and $\overline{\text{READY}}$ $V_{DD} = 5 \text{ V} \pm 10\%; V_{SS} = 0 \text{ V}$ $T_A = 0 \text{ to } +70 \text{ }^\circ\text{C}$ C_L (for PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF C_L (for Port 6, $\overline{\text{CS}}$) = 100 pF

| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|---|-------------|----------------------------|---------------------|--|----------------------------|------|
| | | min. | max. | min. | max. | |
| CLKOUT cycle time | t_{29} CC | 50 | 50 | 2TCL | 2TCL | ns |
| CLKOUT high time | t_{30} CC | 20 | — | TCL – 5 | — | ns |
| CLKOUT low time | t_{31} CC | 15 | — | TCL – 10 | — | ns |
| CLKOUT rise time | t_{32} CC | — | 5 | — | 5 | ns |
| CLKOUT fall time | t_{33} CC | — | 5 | — | 5 | ns |
| CLKOUT rising edge to ALE falling edge | t_{34} CC | $0 + t_A$ | $10 + t_A$ | $0 + t_A$ | $10 + t_A$ | ns |
| Synchronous $\overline{\text{READY}}$ setup time to CLKOUT | t_{35} SR | 10 | — | 10 | — | ns |
| Synchronous $\overline{\text{READY}}$ hold time after CLKOUT | t_{36} SR | 0 | — | 0 | — | ns |
| Asynchronous $\overline{\text{READY}}$ low time | t_{37} SR | 65 | — | 2TCL + 15 | — | ns |
| Asynchronous $\overline{\text{READY}}$ setup time ¹⁾ | t_{58} SR | 15 | — | 15 | — | ns |
| Asynchronous $\overline{\text{READY}}$ hold time ¹⁾ | t_{59} SR | 0 | — | 0 | — | ns |
| Async. $\overline{\text{READY}}$ hold time after $\overline{\text{RD}}$, $\overline{\text{WR}}$ high (Demul- tiplexed Bus) ²⁾ | t_{60} SR | 0 | $0 + 2t_{A2} + t_F$ | 0 | $TCL - 25 + 2t_{A2} + t_F$ | ns |

Notes:

- ¹⁾ These timings are given for test purposes only, in order to assure recognition at a specific clock edge.
- ²⁾ Demultiplexed bus is the worst case. For multiplexed bus 2TCL are to be added to the maximum values. This adds even more time for deactivating $\overline{\text{READY}}$. The $2t_A$ refer to the next following bus cycle.

Figure 20. CLKOUT and $\overline{\text{READY}}$ **Notes:**

- 1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
- 2) The leading edge of the respective command depends on RW-delay.
- 3) $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled waitstate, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
- 4) $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
- 5) If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if $\overline{\text{READY}}$ is removed in response to the command (see Note 4)).
- 6) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTTC waitstate may be inserted here.
For a multiplexed bus with MTTTC waitstate this delay is 2 CLKOUT cycles, for a demultiplexed bus without MTTTC waitstate this delay is zero.
- 7) The next external bus cycle may start here.

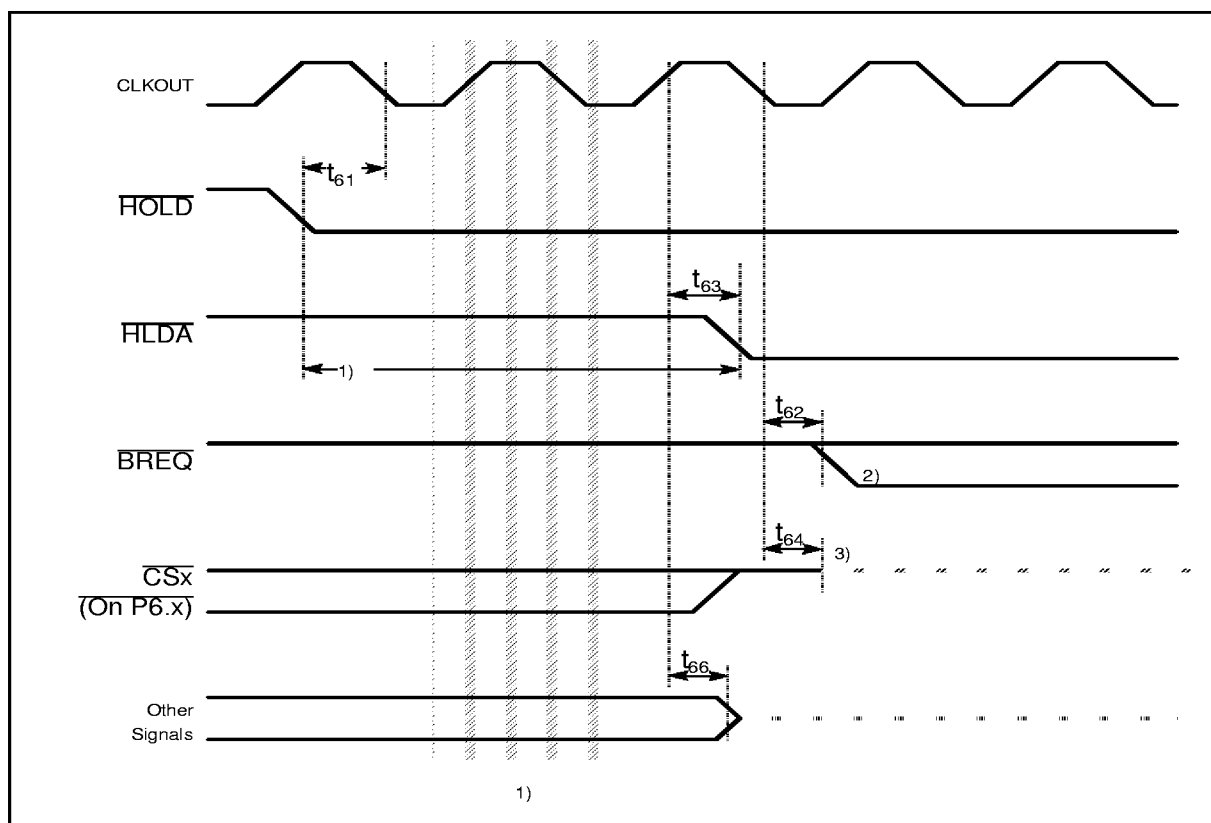
13.5.2.2 External Bus Arbitration

 $V_{DD} = 5\text{ V} \pm 10\%; V_{SS} = 0\text{ V}$
 $T_A = 0\text{ to }+70\text{ }^{\circ}\text{C}$
 C_L (for PORT0, PORT1, Port 4, ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BHE}}$, CLKOUT) = 100 pF

 C_L (for Port 6, $\overline{\text{CS}}$) = 100 pF

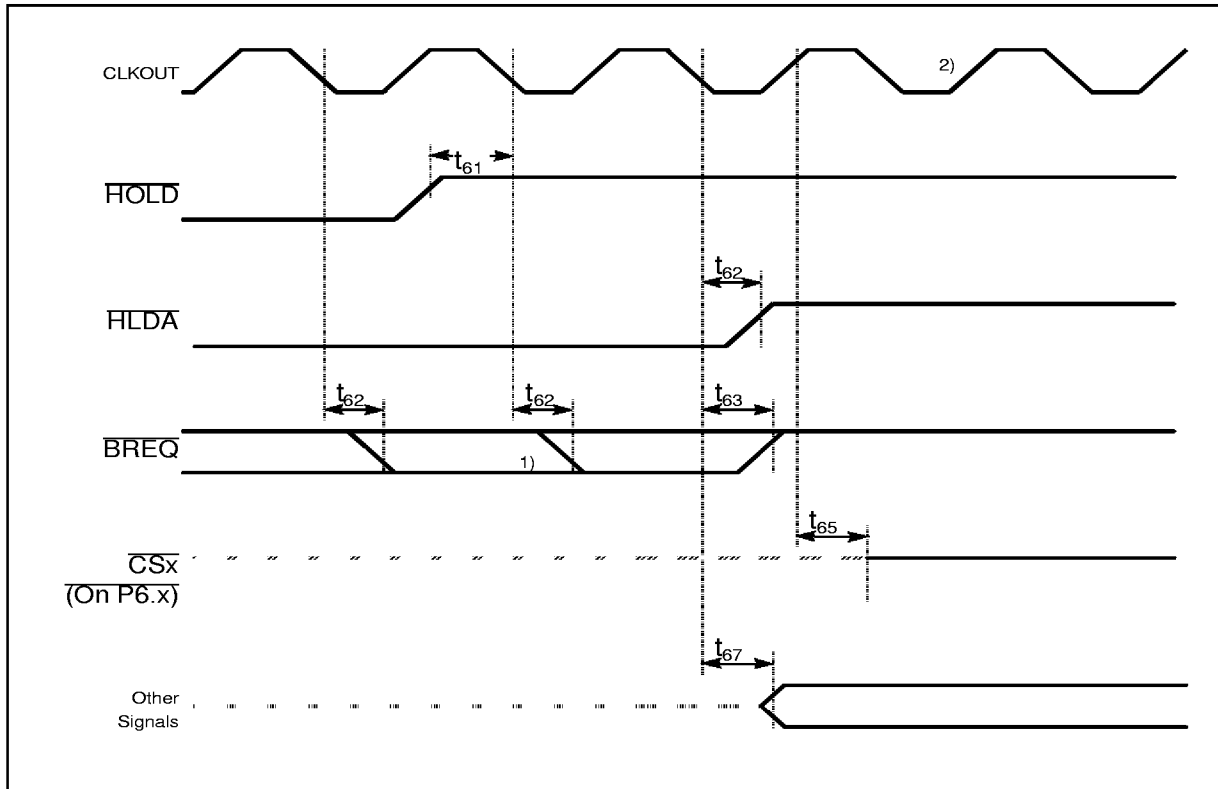
| Parameter | Symbol | Max. CPU Clock = 20 MHz | | Variable CPU Clock 1/2TCL = 1 to 20 MHz | | Unit |
|--|-------------|----------------------------|------|--|------|------|
| | | min. | max. | min. | max. | |
| HOLD input setup time to CLKOUT | t_{61} SR | 20 | — | 20 | — | ns |
| CLKOUT to $\overline{\text{HLD\!A}}$ high or $\overline{\text{BREQ}}$ low delay | t_{62} CC | — | 20 | — | 20 | ns |
| CLKOUT to $\overline{\text{HLD\!A}}$ low or $\overline{\text{BREQ}}$ high delay | t_{63} CC | — | 20 | — | 20 | ns |
| $\overline{\text{CSx}}$ release | t_{64} CC | — | 20 | — | 20 | ns |
| $\overline{\text{CSx}}$ drive | t_{65} CC | -5 | 25 | -5 | 25 | ns |
| Other signals release | t_{66} CC | — | 20 | — | 20 | ns |
| Other signals drive | t_{67} CC | -5 | 25 | -5 | 25 | ns |

Figure 21. External Bus Arbitration, Releasing the Bus

**Notes:**

- 1) The ST10R165 will complete the currently running bus cycle before granting bus access.
- 2) This is the first possibility for $\overline{\text{BREQ}}$ to get active.
- 3) The $\overline{\text{CS}}$ outputs will be resistive high (pullup) after t_{64} .

Figure 22. External Bus Arbitration, (Regaining the Bus)

**Notes:**

- 1) This is the last chance for $\overline{\text{BREQ}}$ to trigger the indicated regain-sequence. Even if $\overline{\text{BREQ}}$ is activated earlier, the regain-sequence is initiated by $\overline{\text{HOLD}}$ going high. Please note that $\overline{\text{HOLD}}$ may also be deactivated without the ST10R165 requesting the bus.
- 2) The next ST10R165 driven bus cycle may start here.

14 PACKAGE MECHANICAL DATA

Figure 23. Package Outline PQFP100 (14 x 20 mm)

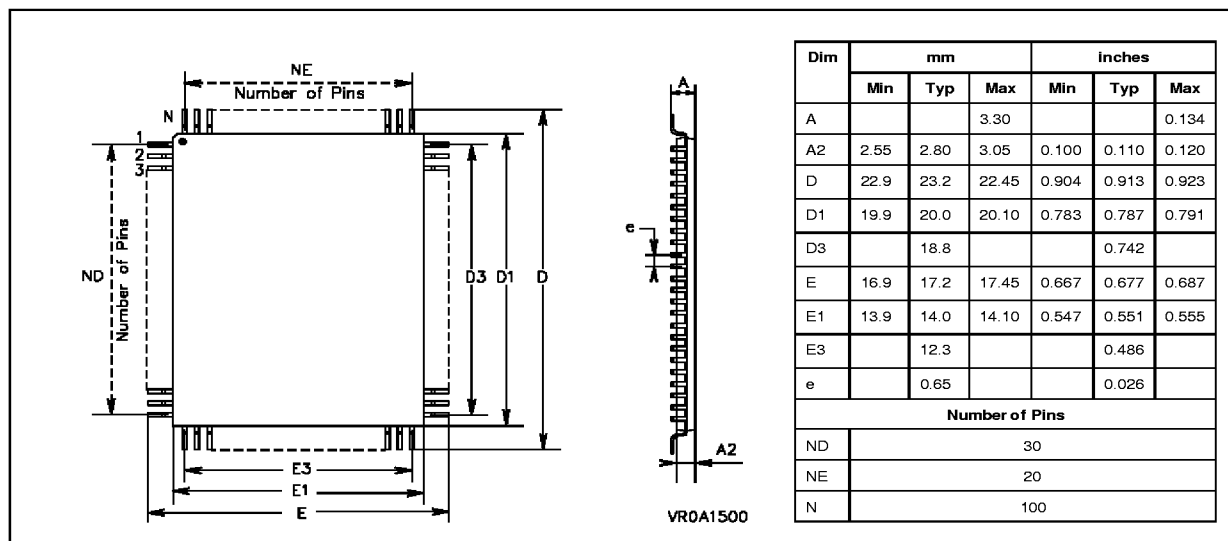
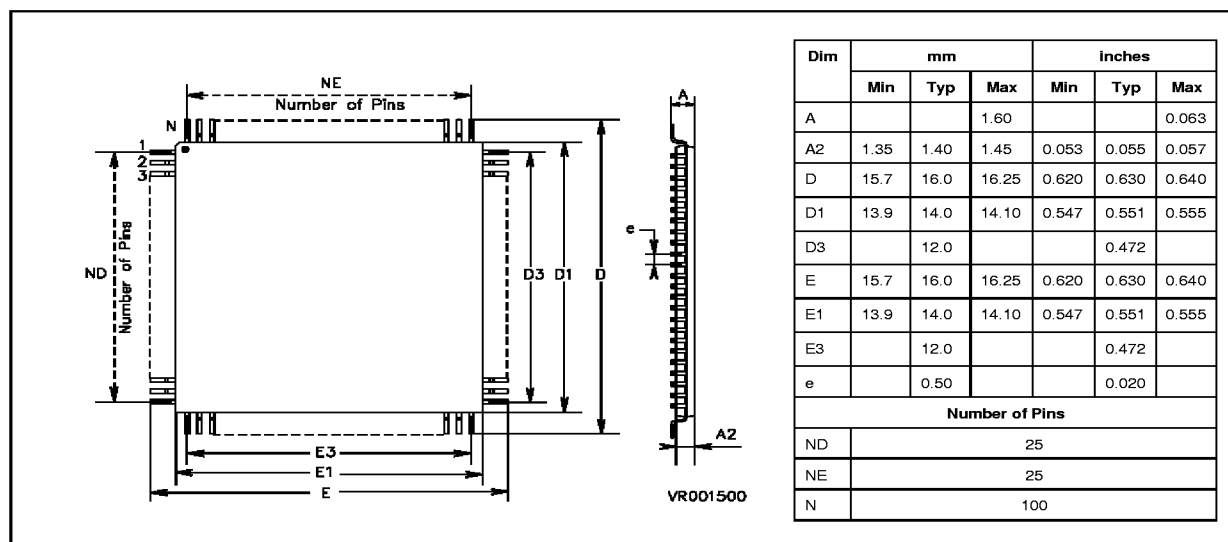


Figure 24. Package Outline TQFP100 (14 x 14 mm)



15 ORDERING INFORMATION

| Salestype | Temperature range | Package |
|------------------|--------------------------|-----------------|
| ST10R165BQ1 | 0°C to 70°C | PQFP100(14x 20) |
| ST10R165BQ6 | - 40°C to 85°C | PQFP100(14x 20) |
| ST10R165BT1 | 0°C to 70°C | TQFP100(14x 14) |
| ST10R165BT6 | - 40°C to 85°C | TQFP100(14x 14) |

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