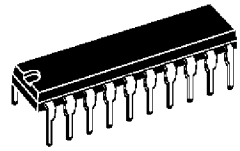
SGS-THOMSON MICROELECTRONICS

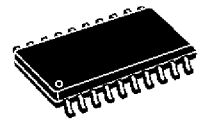
TDA7331

SINGLE CHIP RDS DEMODULATOR + FILTER

PRELIMINARY DATA

- VERY HIGH RDS DEMODULATION QUALITY WITH IMPROVED DIGITAL SIGNAL PROCESSING
- HIGH PERFORMANCE, 57KHz BANDPASS FILTER (8th ORDER)
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- ARI (SK INDICATION) AND RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR (8.664 and 17.328MHz OPTIONAL)
- LOW NOISE CMOS TECHNOLOGY
- LOW RADIATION





DIP20 **SO20**

ORDERING NUMBERS:

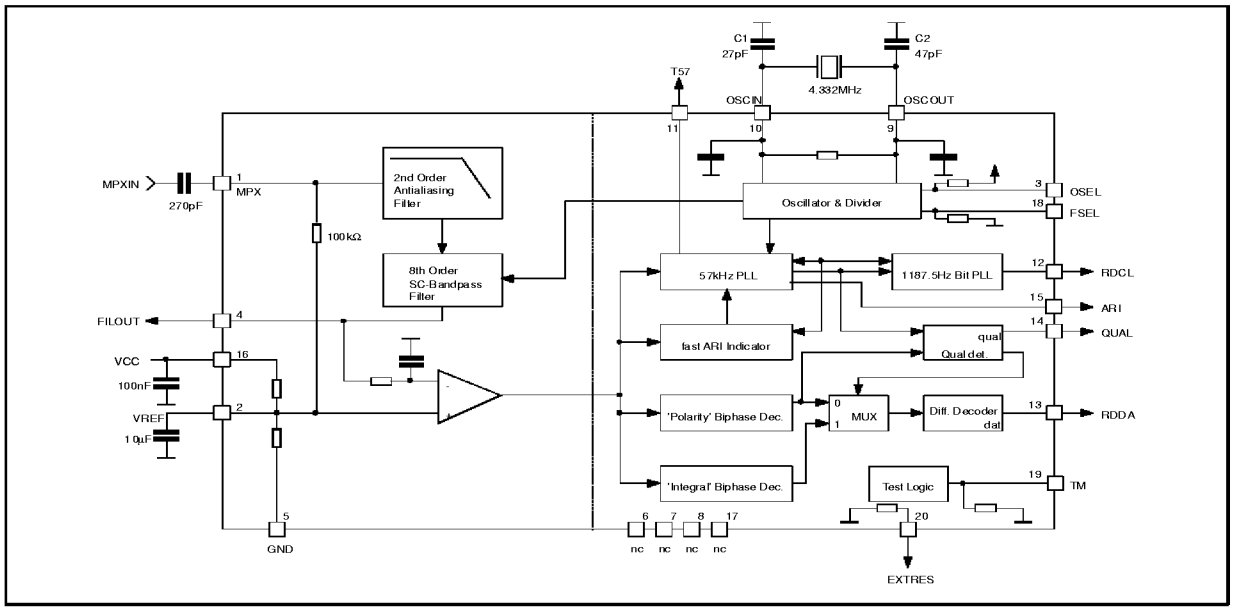
TDA7331 TDA7331D

DESCRIPTION

The TDA7331 is a RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations.
The output data signal (RDDA) and clock signal (RDCL) can be further processed by a suitable RDS decoder (microprocessor).

The device operates in accordance with the EBU (European Broadcasting Union) specifications.
The IC includes a 2nd order antialiasing input filter, a 57KHz switched capacitor band pass filter, a smoothing filter and cross detector, a bit rate clock recovery circuit, a 57KHz PLL, BI-PHASE PSK decoder, differential decoding circuit, ARI indication and RDS signal quality output.

BLOCK DIAGRAM



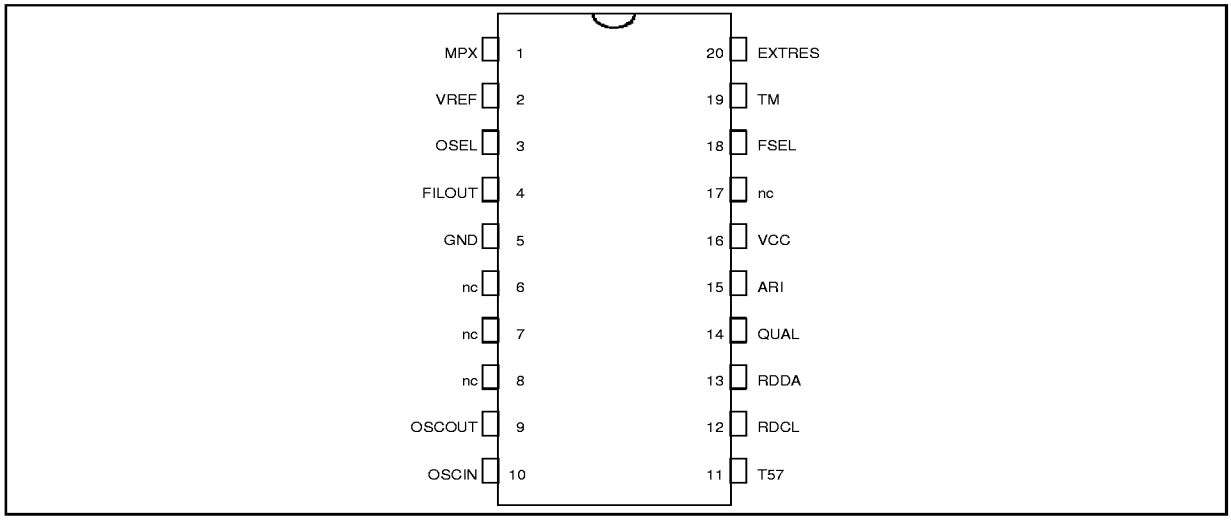
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-35 to 125	°C

PIN FUNCTION

N° pin	Name	Description
1	MPX	RDS input signal
2	VREF	Reference voltage
3	OSEL	Oscillator selector pin: - open, closed to VCC = quartz oscillator - closed to GND = external driven
4	FILOUT	Filter output
5	GND	Ground
6	nc	not connected
7	nc	not connected
8	nc	not connected
9	OSCOUT	Oscillator output
10	OSCIN	Oscillator input
11	T57	Testing output pin: 57kHz clock output
12	RDCL	RDS clock output 1187.5Hz
13	RDDA	RDS data output
14	QUAL	Output for signal quality indication (High = good)
15	ARI	Output for ARI indication: - high when RDS+ARI are present - high when only ARI is present
16	VCC	Supply voltage
17	nc	not connected
18	FSEL	Frequency selector pin: -100K to VCC = 17.328MHz - open=4.332MHz - closed to VCC = 8.664MHz
19	TM	Test mode pin: - open = normal RUN - closed to VCC = Testmode
20	EXTRES	Reset pin: - open = run mode - closed to VCC = reset condition

PIN CONNECTION



THERMAL DATA

Symbol	Description		DIP20	SO20	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ.	100	200	°C/W

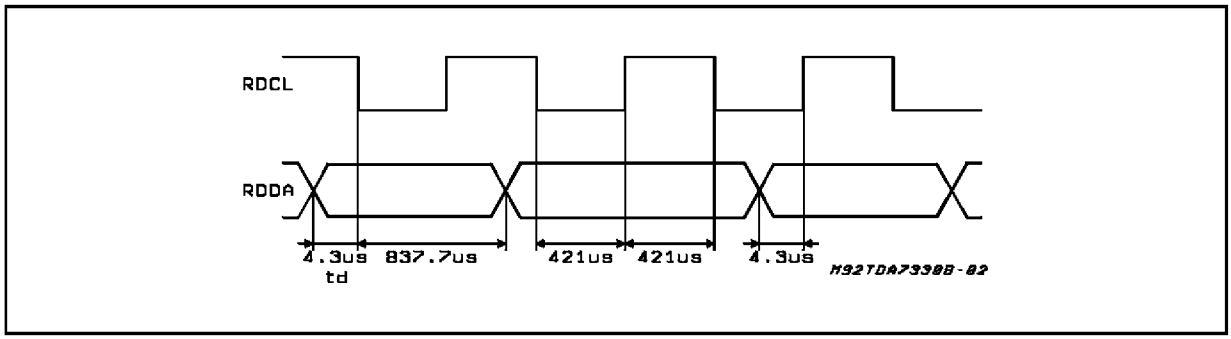
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_{cc} = 5V, unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{CC}	Supply current		4.0	6.5	9.0	mA
FILTER						
f_C	Center frequency		56.5	57	57.5	kHz
BW	3dB Bandwidth		2.5	3	3.5	kHz
G	Gain	f = 57kHz	18	20	22	dB
A	Attenuation	f = 4kHz	18	22		dB
		f = 38kHz	50	60		dB
		f = 67kHz	35	45		dB
R_I	Input impedance of MPX			120		KΩ
R_L	Load impedance on FILOUT		1			MΩ
S/N	Signal to noise ratio	V_{IN} = 3mV_{RMS}		40		dB
V_{IN}	MPX input signal	f = 19kHz; T3= 40dB(1) f = 57kHz (RDS+ ARI)	170	250	600 50	mV_{RMS}
V_{REF}	Reference			V_{CC}/2		V
DEMODULATOR						
Input pins (EXTRES, FSEL, TM) **Input pin (OSEL)**			**all with internal pull down resistor** **with internal pull up resistor**			
R_{PD}	Pull down			160		KΩ
R_{PU}	Pull up		80	120	160	KΩ
V_{IH}	Input voltage high		0.7V_{cc}	0.8V_{cc}		V
V_{IL}	Input voltage low			0.2V_{cc}	0.3Vcc	V
Output pins (RDCL, RDDA, ARI, QUAL, T57)						
V_{OH}	Ouput voltage high	I_L = 0.5mA	4	4.6		V
V_{OL}	Output voltage low	I_L = 0.5mA		0.4	1	V
OSCILLATOR						
VCLL	Clock input level	pin OSEL = open			1	V
VCLH	Clock input level	pin OSEL = open	4			V
	Amplitude OSCOUT	pin OSEL = open		4.5		V
V_{PP}	Amplitude OSCIN	pin OSEL = GND, F = 4.332MHz		60		mV
		pin OSEL = GND, F = 8.664MHz		80		mV
		pin OSEL = GND, F = 17.328MHz		150		mV

(1) The 3rd harmonic (57kHz) must be less than -40dB with respect to the input signal plus gain.

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	ΔPh max
A	56.5	57	57.5	<5°
B	56	57	58	<7.5°
C	55.5	57	58.5	<10°

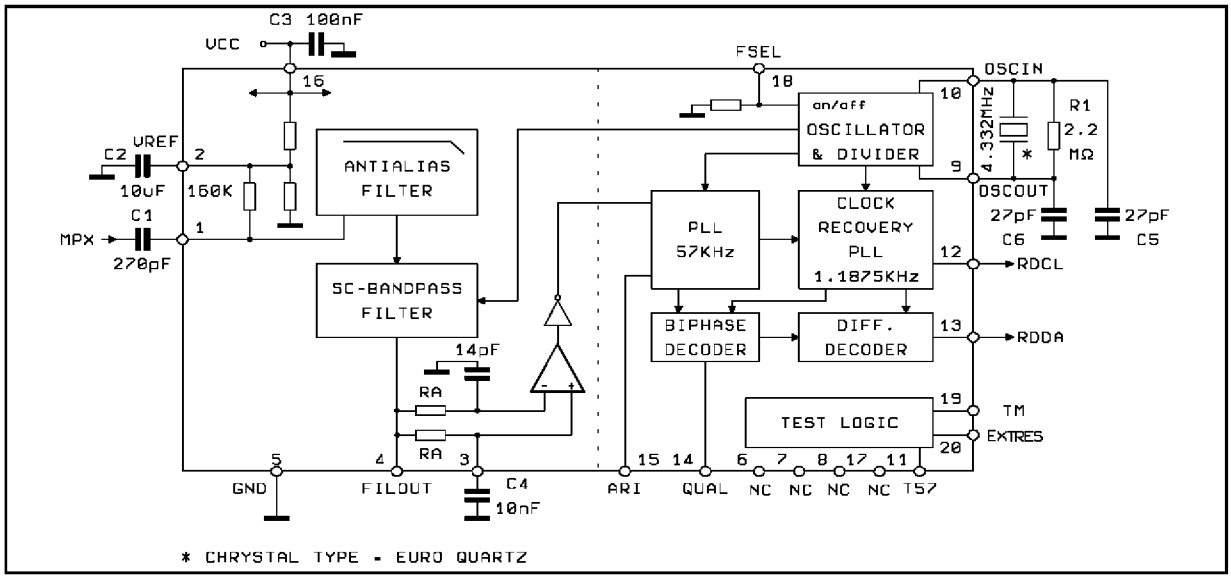
Figure 1. RDS timing diagram



OUTPUT TIMING

The generated 1187.5Hz output clock (RDCL line) is synchronized to the incoming data.
According to the internal PLL lock condition this data change can results on the falling or on the rising clock edge.
Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7 µsec after the clock transition.

Figure 2. Test Circuit



OSCILLATOR

Three different crystal-frequencies can be used. The adaption of the internal clock divider to the external crystal is achieved via the input pin FSEL. One has to select as follows:

Crystal	FSEL
4.332MHz	0, open
8.664MHz	1
17.328MHz	external resistor of 100K to VCC

A special mode is introduced to reduce EMI. With pin OSEL connected to GND the internal oscillator is switched off and an external sinusoidal frequency could be applied on OSCIN. The peak to peak voltage of this signal can be reduced down to 60mV.

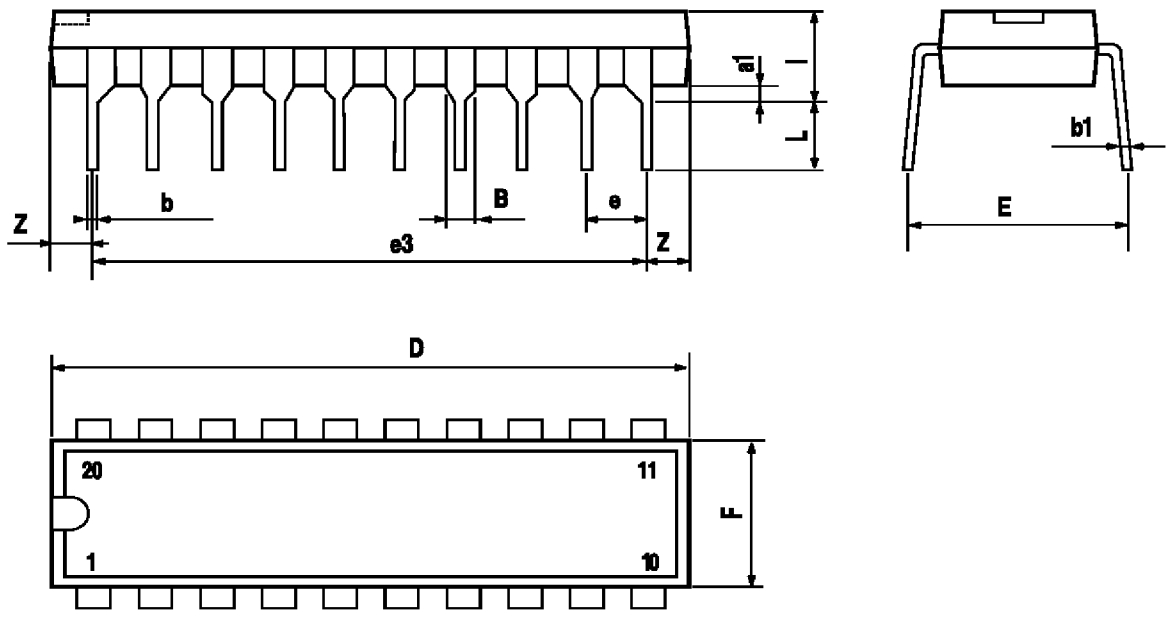
The frequency selection via FSEL is still active.

Suggested values of C1 and C2 are shown in the following table.

Crystal	C1	C2
4.332MHz	27pF	47pF
8.664MHz	27pF	-
17.328MHz	27pF	-

DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)