

SN74AS8839

32-Bit

Shuffle/Exchange Network

- High speed data manipulation
- Shuffles up to 32-Bit data streams
- Performs shuffle and exchange permutations on entire data streams or substrings for implementing algorithms and/or matrix operations
- 24 mA bus drivers
- 3-State outputs allow 32-bit and 16-bit bus interface
- 85-pin package
- Texas Instruments quality and reliability

Description

The SN74AS8839 is a high-speed 32-bit shuffle/exchange network in an 85-pin ceramic pin-grid array package. The device can perform data permutations on 32-bit, 16-bit, and 8-bit or 4-bit words in a single instruction cycle of under 25 ns.

The type of data permutation to be performed is determined by an input decoder. Data manipulation is not clock dependent and is restricted only by internal propagation delays. The delay is the same regardless of the number of positions to be routed, resulting in a high-speed shuffle.

Three-state output controls allow the 'AS8839 to be interfaced with 32-bit or 16-bit data buses.

The shuffle/exchange network is designed for use primarily in multiple processor applications. The device can be used to implement single instruction multiple data (SIMD) array processors. SIMD processors are used in applications such as matrix multiplication, parallel sorting, and parallel Fast Fourier Transforms (FFTs). The shuffle/exchange networks can also be used for fault tolerant computer applications.

Data Permutations

The 'AS8839 performs five types of data permutations on one 32-bit, two 16-bit, and four 8-bit or eight 4-bit data words:

1. Perfect shuffle
2. Inverse shuffle
3. Upper broadcast
4. Lower broadcast
5. Bit exchange

Hypothetical examples of these permutation types for an 8-bit data word are given in Figure 2.

Data permutations are performed by a series of multiplexers arranged in four levels:

1. A 32-bit multiplexer;
2. Two 16-bit multiplexers;
3. Four 8-bit multiplexers or eight 4-bit multiplexers;
4. One 32-bit multiplexer.

Data can be shuffled at each of these levels in a single pass through the chip or shifted at selected levels and passed through the others without alteration.

Data Flow

Data is input to the chip on the D port, which passes data to a 32-bit multiplexer, where it is shuffled or passed unaltered according to the inputs on the SFT6-SFT5 pins (see Tables 1-5). Output from the 32-bit multiplexer is input to two 16-bit multiplexers for permutation or pass operations as coded on SFT4-SFT3. Output from this stage passes to four 8-bit multiplexers or eight 4-bit multiplexers for parallel permutation operations, according to the SFT2-SFT1 inputs. Output from these processors passes to a 32-bit multiplexer where it is permuted or passed according to the SFT0 input. The result is passed out of the chip through the 32-bit Y port.

Instruction Set

Possible modes of operation at the device's four levels are shown in Tables 1-5. Mode selection is controlled by seven SFT inputs, as shown in the tables.

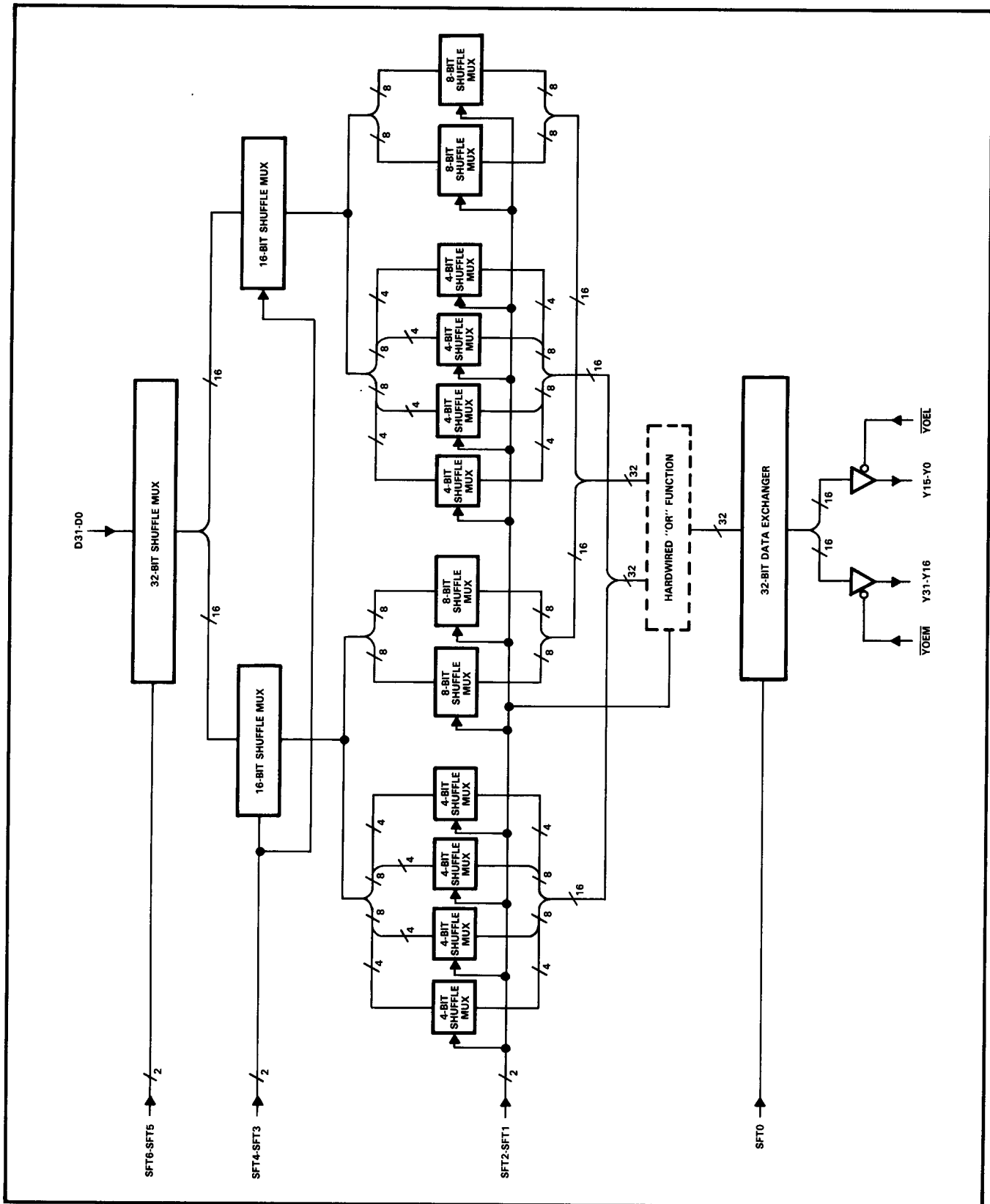


Figure 1. SN74AS8839 32-Bit Shuffle/Exchange Network

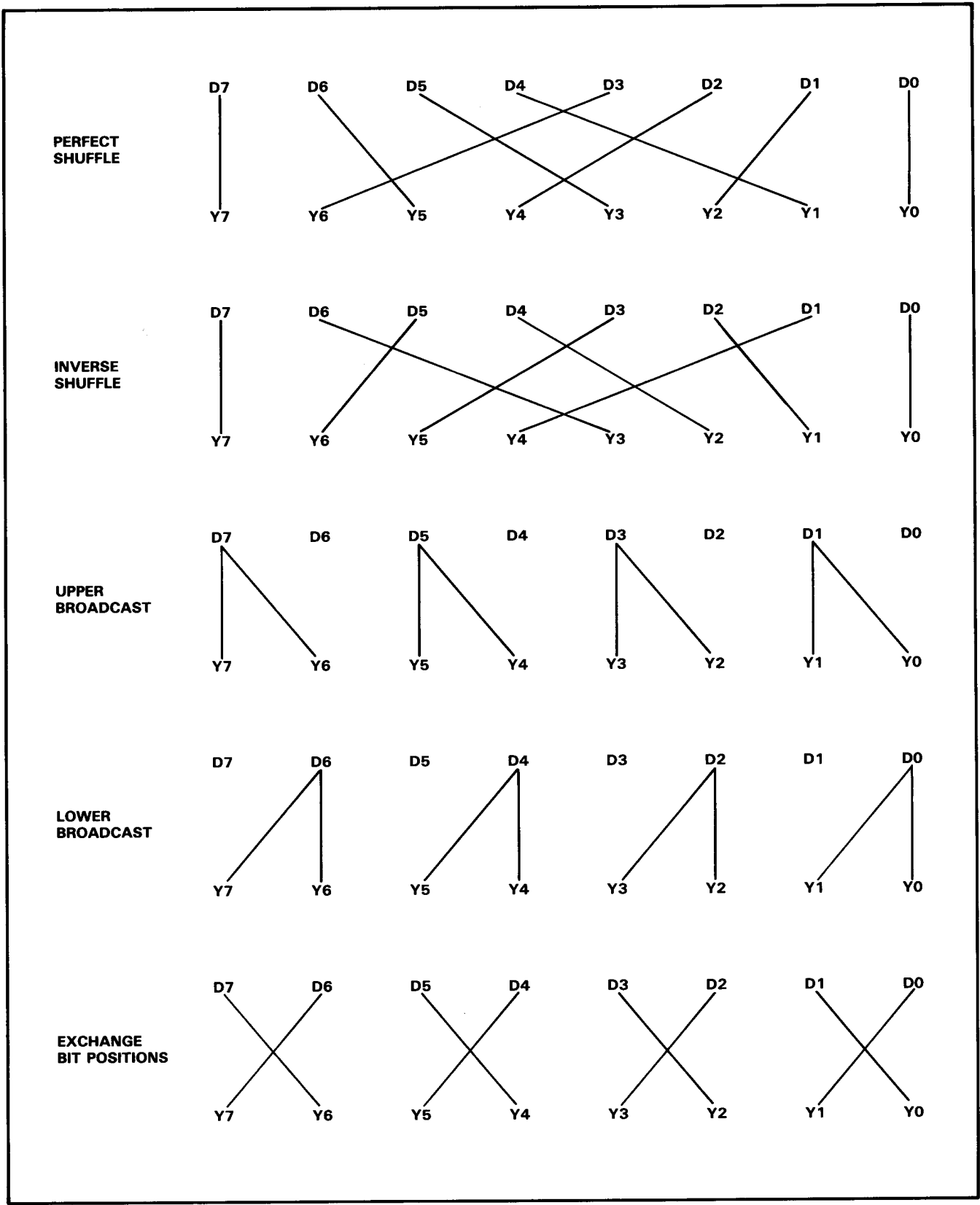


Figure 2. Permutation Types, 8-Bit String

Table 1. 32-Bit Multiplexer Operations

Multiplexer Level	Signal		Operation	Notes
	SFT6	SFT5		
1 (One 32-bit word)	0	0	Pass data unaltered	Can be performed as lower broadcast at 16-bit multiplexer level (see Table 2).
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
	1	1	Upper broadcast	
	—	—	Lower broadcast	

Table 2. 16-Bit Multiplexer Operations

Multiplexer Level	Signal		Operation	Notes
	SFT4	SFT3		
2 (Two 16-bit words)	0	0	Pass data unaltered	Can be performed as upper broadcast at 32-bit multiplexer level (see Table 1).
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
	—	—	Upper broadcast	
	1	1	Lower broadcast	

Table 3. 8-Bit Multiplexer Operations

Multiplexer Level	Signal		Operation	Notes
	SFT2	SFT1		
3 (Four 8-bit words)	0	0	Pass data unaltered	Can be performed as lower broadcast at 16-bit multiplexer level (see Table 2). Can be performed as upper broadcast at 32-bit multiplexer level (see Table 1).
	0	1	Perfect shuffle	
	1	0	Inverse shuffle	
	—	—	Lower broadcast	
	—	—	Upper broadcast	

Table 4. 4-Bit Multiplexer Operations

Multiplexer Level	Signal		Operation	Notes
	SFT2	SFT1		
3 (Eight 4-bit words)	0	0	Pass data unaltered	Can be performed as lower broadcast at 16-bit multiplexer level (see Table 2). Can be performed as upper broadcast at 32-bit multiplexer level (see Table 1).
	1	1	Perfect shuffle	
	1	1	Inverse shuffle	
	—	—	Lower broadcast	
	—	—	Upper broadcast	

Table 5. Bit Exchange Multiplexer Operations

Multiplexer Level	Signal SFT6	Operation	Notes
4 (One 32-bit word)	0 1	Pass data unaltered Exchange bits	

Examples

The instruction set for the 'AS8839 is further summarized in Examples 1-12. Examples 1-11 illustrate the data permutations possible at each multiplexer level, assuming that data is passed unaltered

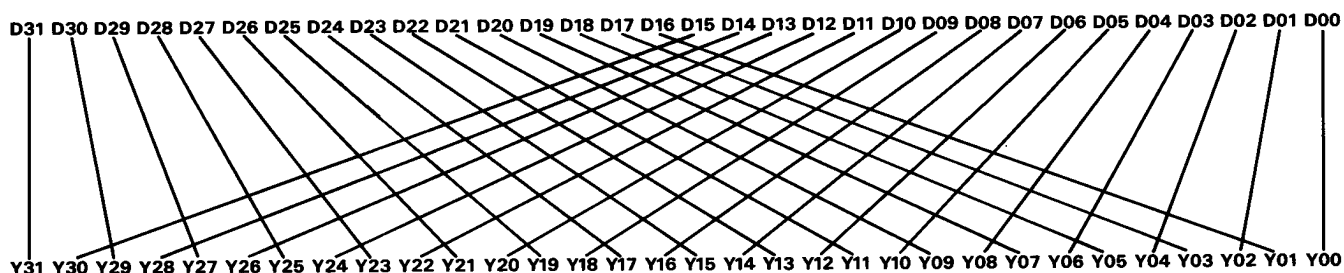
through the other levels. In example 12, data is permuted at two multiplexer levels during a single pass through the chip.

Example 1. Perform a perfect shuffle on a 32-bit word and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	1	0	0	0	0	0

RESULT

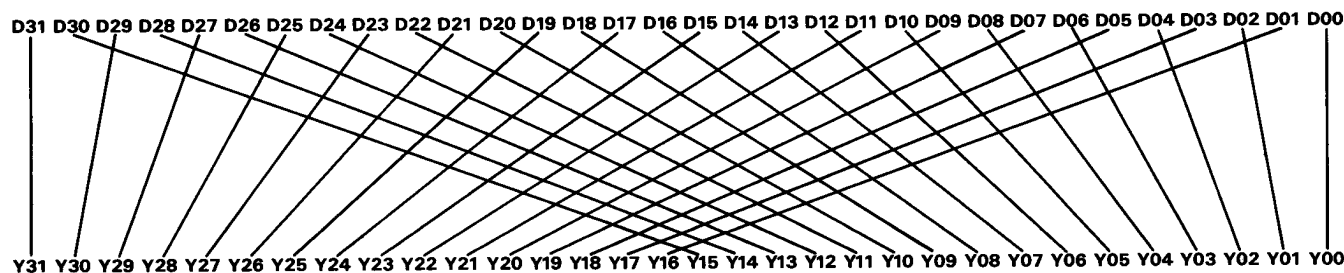


Example 2. Perform an inverse shuffle on a 32-bit word and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
1	0	0	0	0	0	0

RESULT

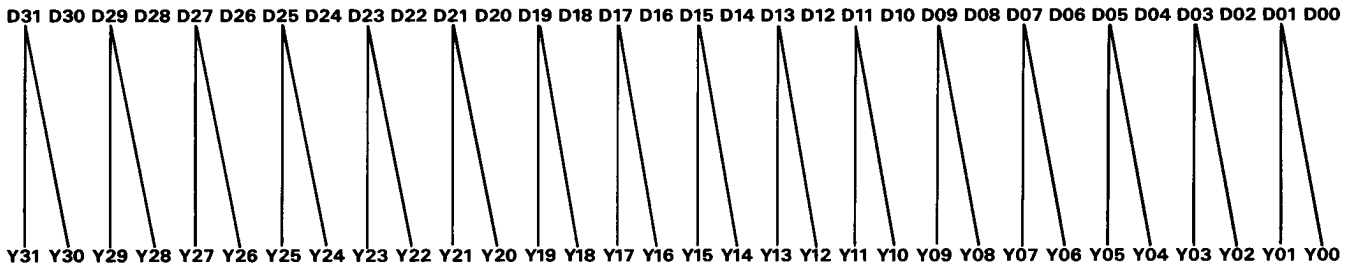


Example 3. Perform an upper broadcast on a 32-bit word and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
1	1	0	0	0	0	0

RESULT

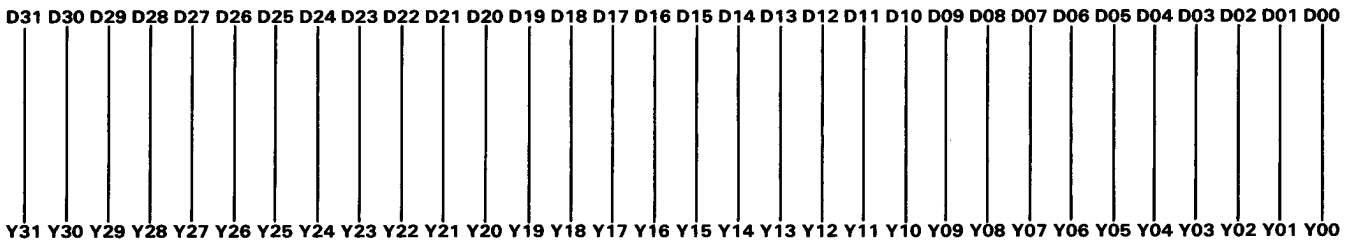


Example 4. Pass a 32-bit word through the 'AS8839 without permutation.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	0	0

RESULT

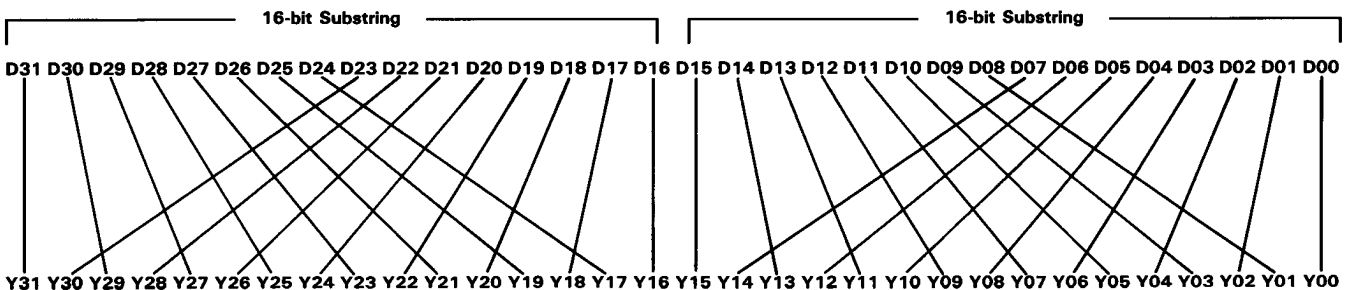


Example 5. Perform a perfect shuffle on two 16-bit words and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	1	0	0	0

RESULT

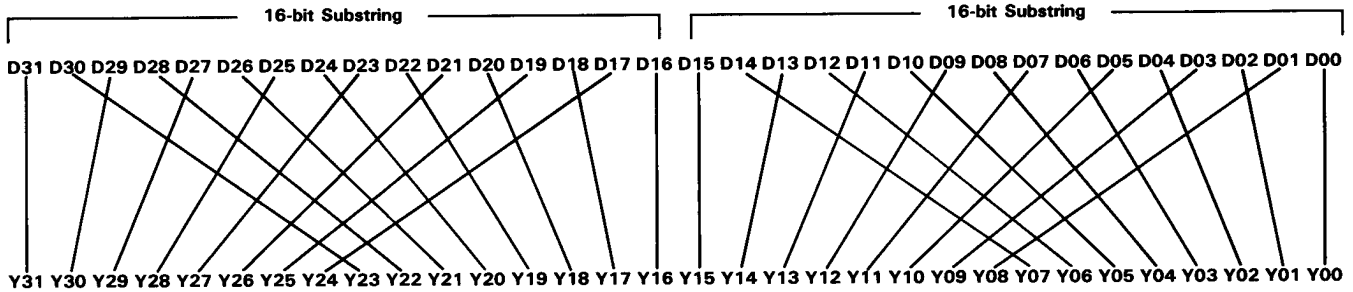


Example 6. Perform an inverse shuffle on two 16-bit words and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	1	0	0	0	0

RESULT

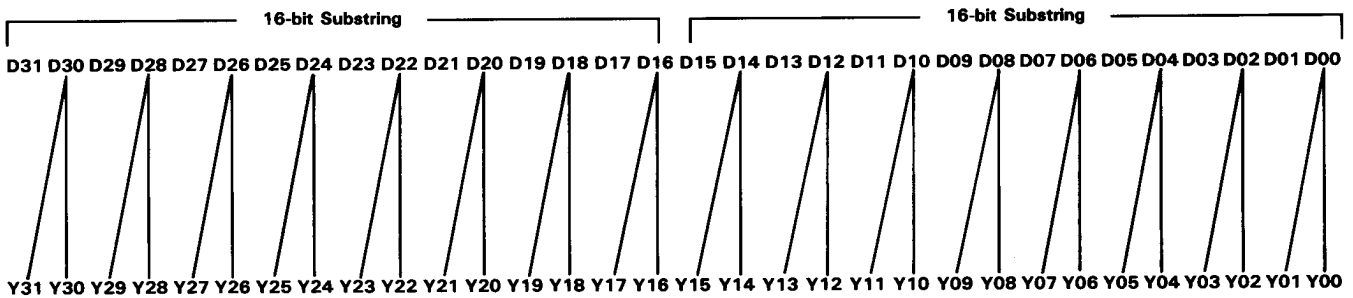


Example 7. Perform a lower broadcast on two 16-bit words and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	1	1	0	0	0

RESULT

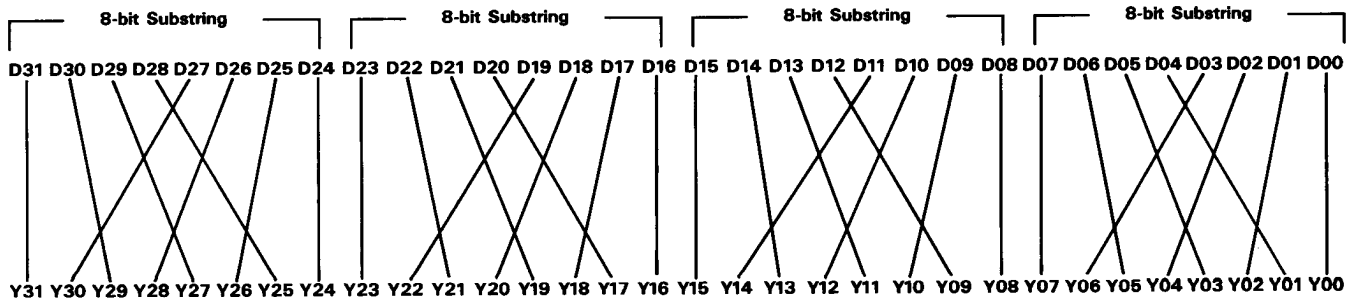


Example 8. Perform a perfect shuffle on four 8-bit words and pass the result to the Y port.

Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	1	0

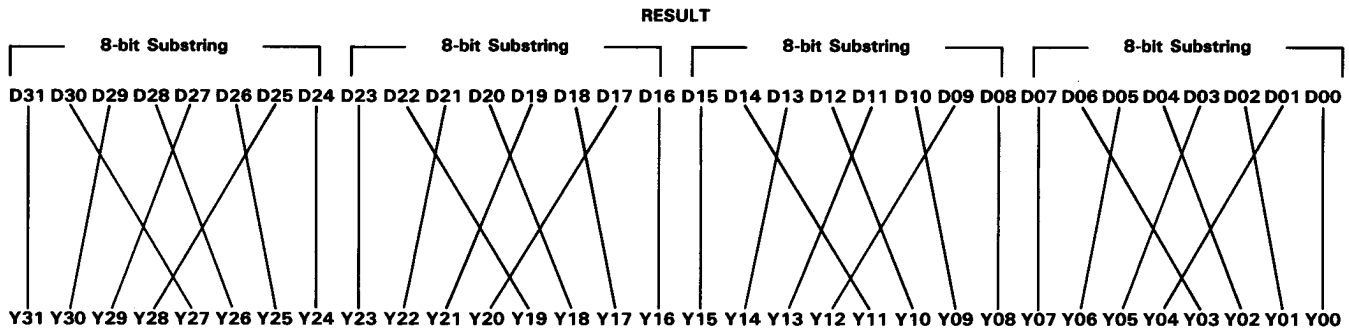
RESULT



Example 9. Perform an inverse shuffle on four 8-bit words and pass the result to the Y port.

Instruction

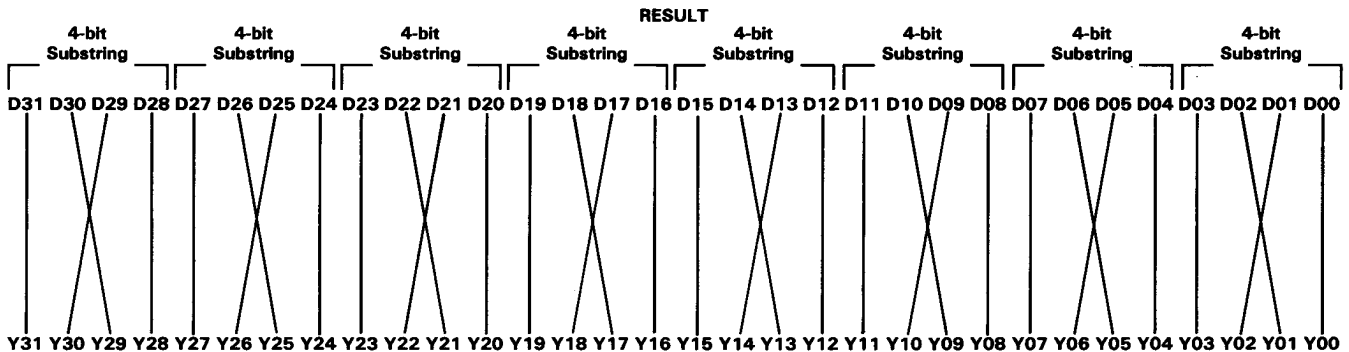
CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	1	0	0



Example 10. Perform a perfect shuffle on eight 4-bit words and pass the result to the Y port.

Instruction

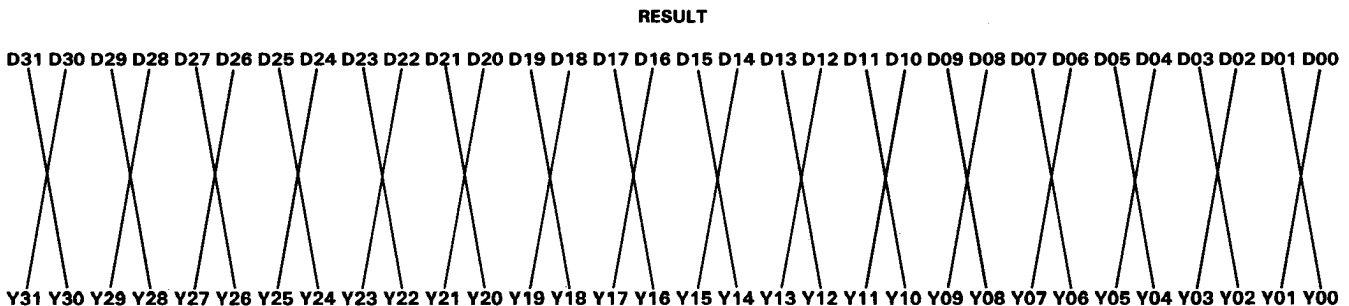
CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	1	1	0



Example 11. Bit-exchange a 32-bit word and pass the result to the Y port.

Instruction

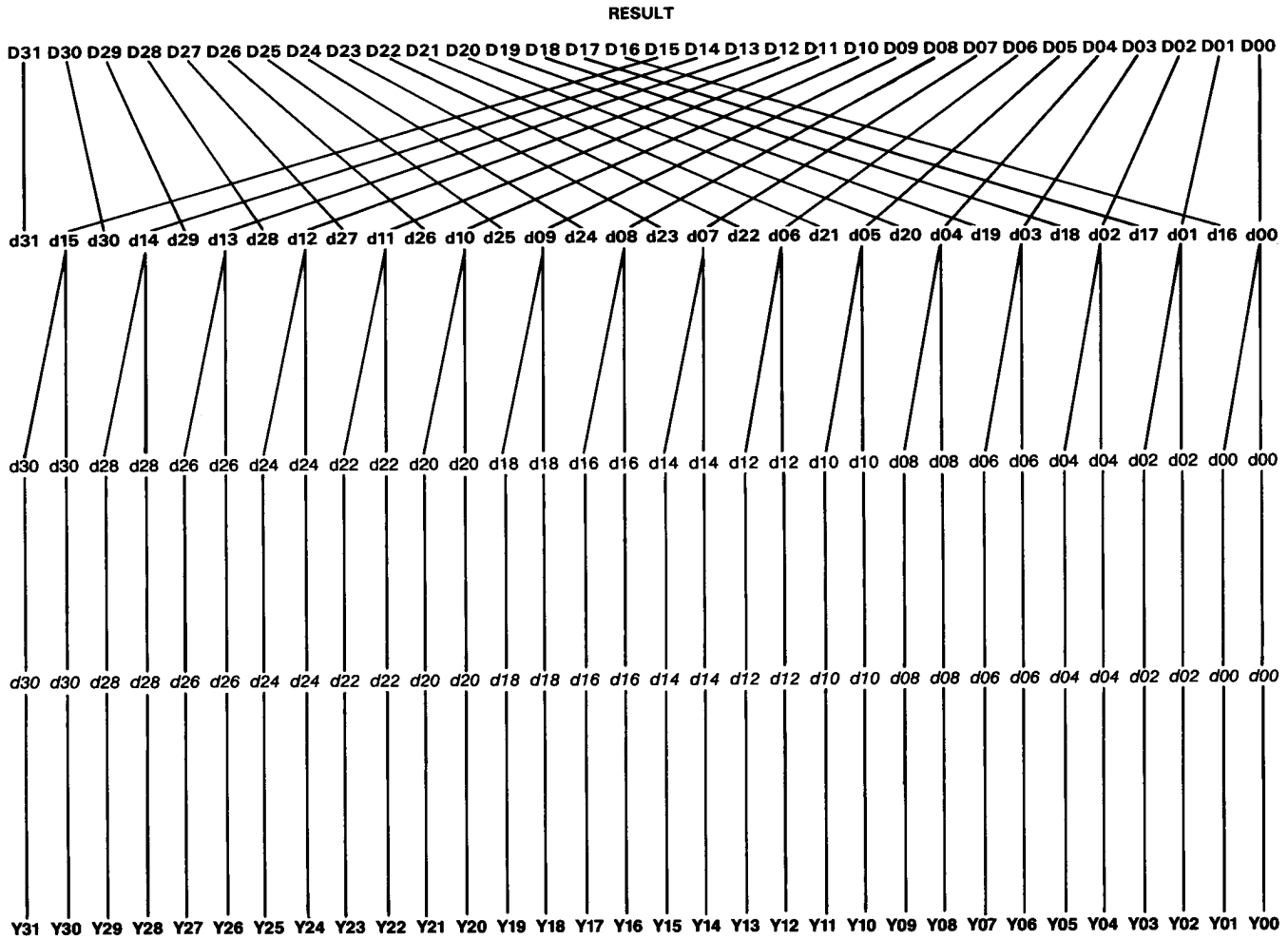
CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	0	0	0	0	0	1



Instruction

CONTROL INPUTS						
SFT6	SFT5	SFT4	SFT3	SFT2	SFT1	SFT0
0	1	1	1	0	0	01

Example 12. Perform a perfect shuffle on a 32-bit word, followed by a lower broadcast; pass the result to the Y port.



Fast Fourier Transforms Using the 'AS8839

Figure 3 is a generalized representation of a single instruction multiple data (SIMD) processor designed to perform the parallel Fast Fourier Transform (FFT) algorithm of Figure 4. 'AS8839 shuffle/exchange networks are used to perform all of the necessary vector permutations and present the resultant permuted vector to the processing elements (PEs). The PEs perform the required multiply and accumulate functions and present the

new vector to the next level of 'AS8839s. Vector permutations for each stage of the FFT calculation are shown in Figure 5.

Figure 6 shows the FFT algorithm in flow chart form. At certain points in the flow chart, the data flow has been broken into two paths to indicate shuffle/exchange operations that can be carried out

simultaneously if parallel banks of 'AS8839s are provided in the SIMD processor design. Figure 8 traces data flow through a system based on this option. The X7-X0 inputs in these figures represent vectors. Figure 7 shows how to interconnect Stage 1 of an eight-point, 4-bit precision FFT.

Each of the eight vectors in the Figure 3 illustration is N bits wide, where $N = 2^x$ and $X \geq 0$. The formula for calculating the number of shuffle/exchange devices necessary for a two-pass shuffle exchange network is $V \times N / 32$, where $V =$ number of vectors and $N =$ width of vector in bits. Figure 8 shows the connections required for one level of 'AS8839s for 8 vectors of 2^2 bits. This

example uses one 'AS8839 for each level ($8 \times 4 / 32$). If the 8 vectors were 2^4 bits wide, four 'AS8839s would be necessary for each level ($8 \times 16 / 32$).

The flow diagrams that are shown for 8-point FFT calculations throughout this application are valid for 8 vectors of up to 32-bit precision. The flow diagrams and required permutations for an FFT calculation on more than 8 data points will differ, but the overall idea is the same. In order to use the 'AS8839 for FFT calculation as described here, the number of points must be a radix of 2 ($2^2, 2^3, 2^4, \dots$), and the number of processing elements must equal the number of data points.

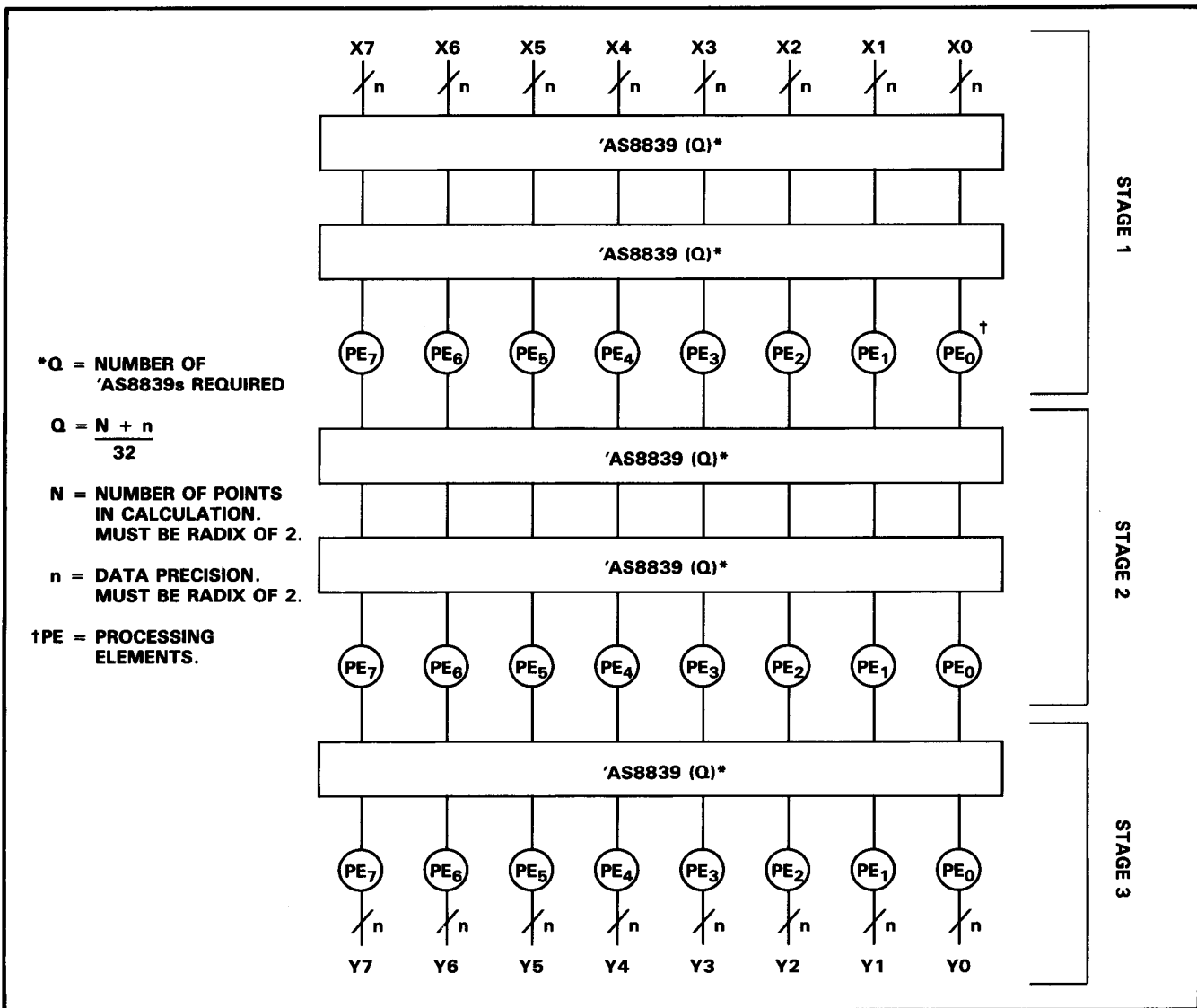


Figure 3. Generalized Architecture for N = 8 Point FFT Computations

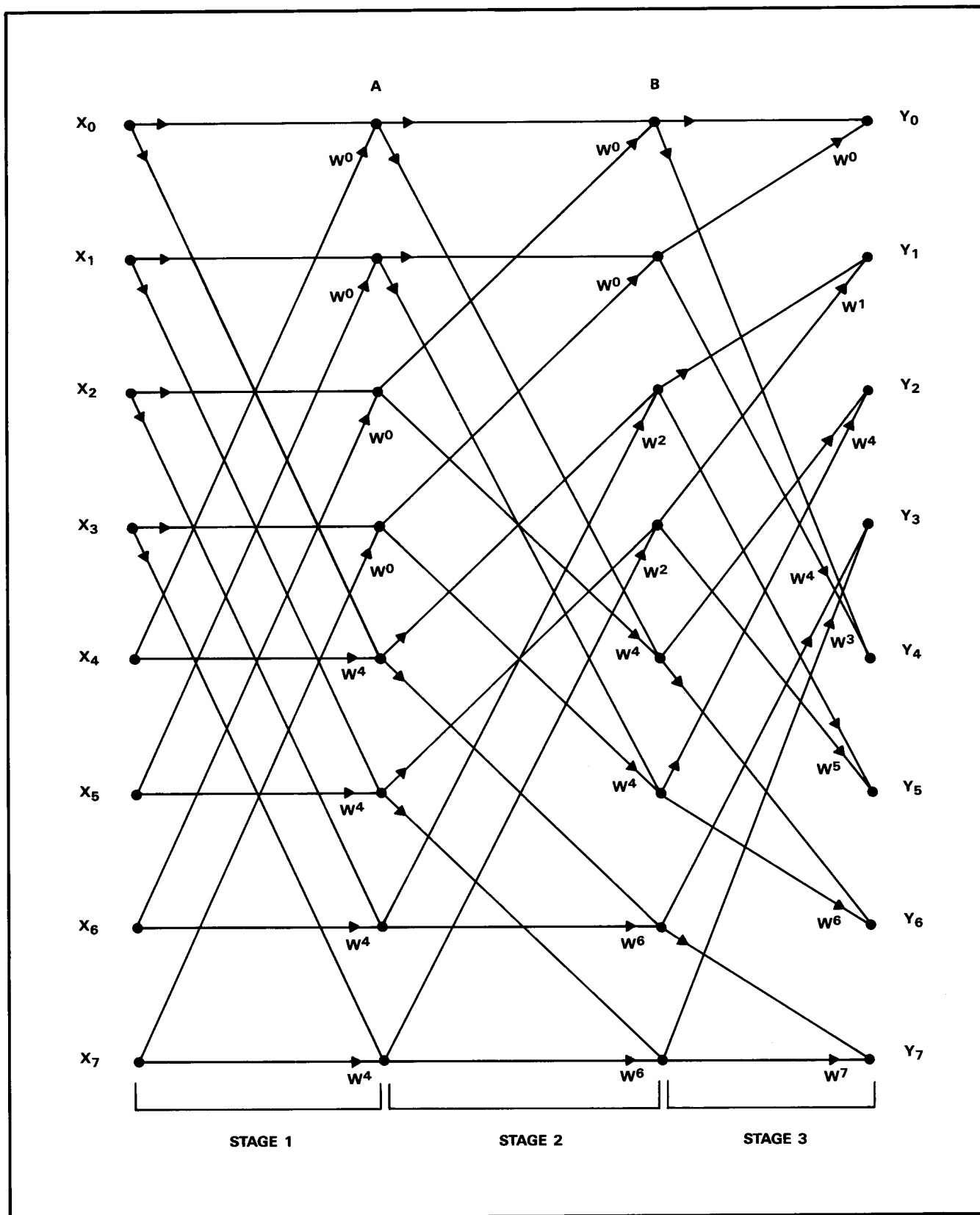


Figure 4. FFT Computation for N = 8 Points

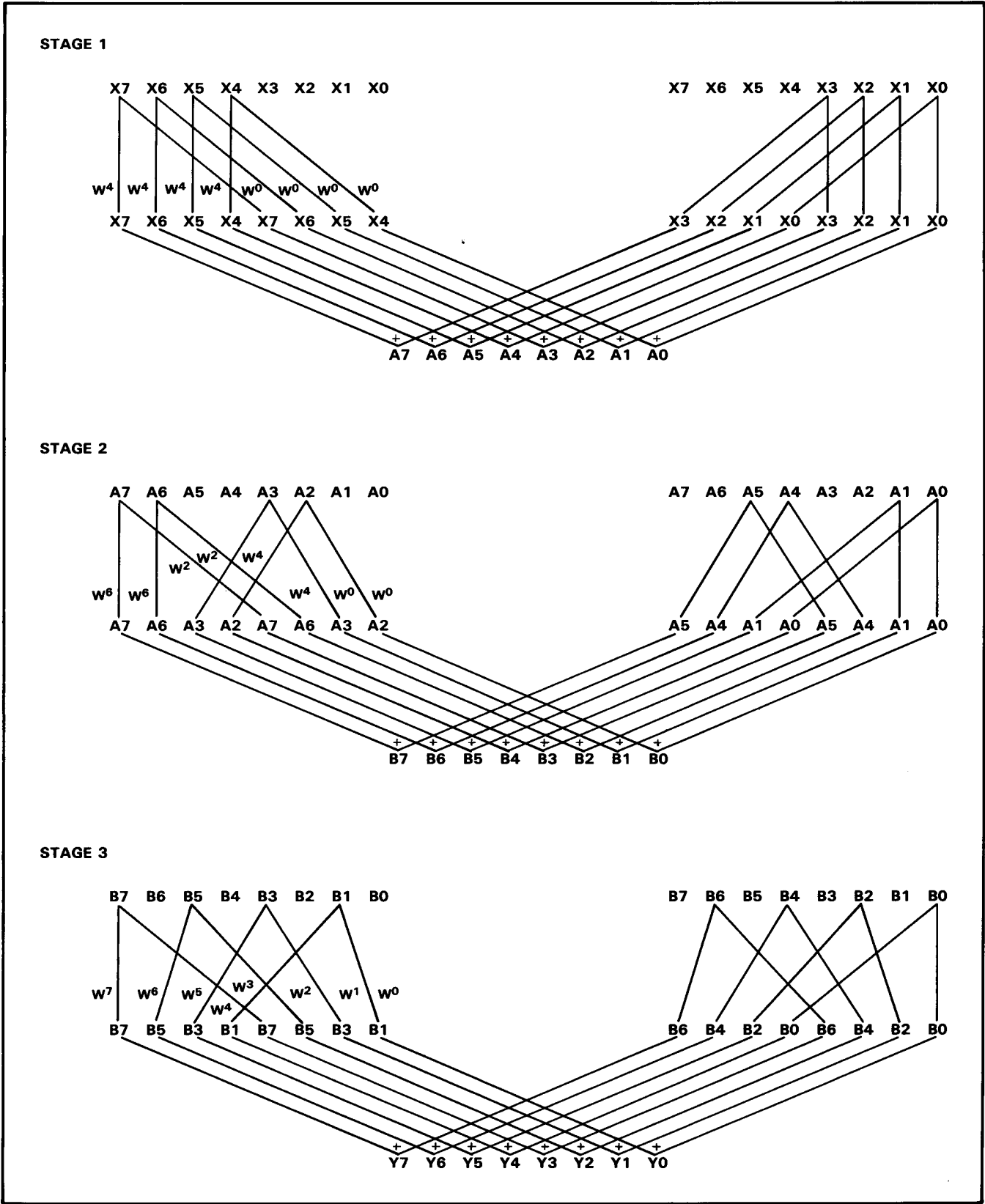


Figure 5. Permutations to be Performed for Figure 3 FFT Computation

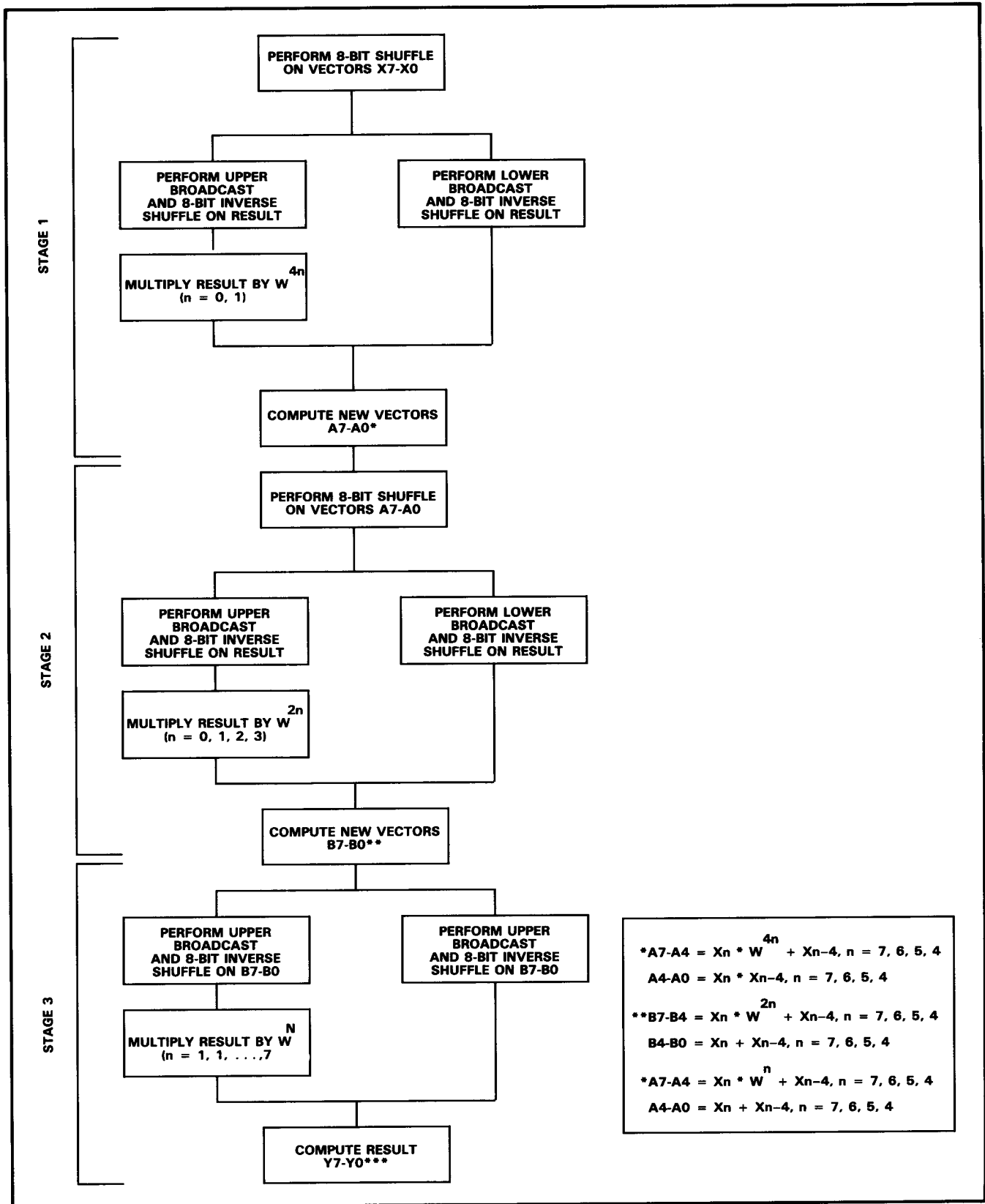


Figure 6. Flow Chart for Figure 3 FFT Computation

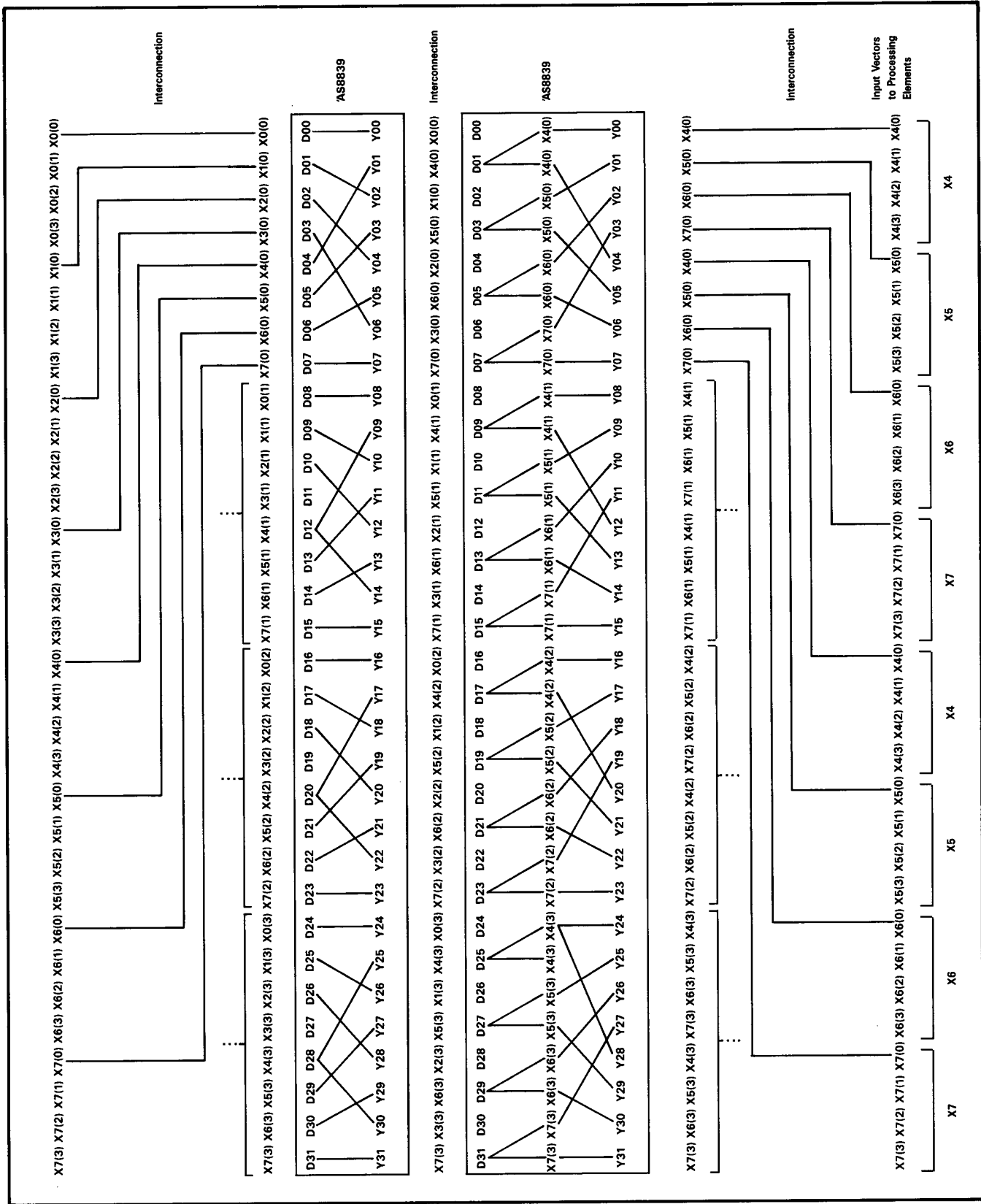


Figure 7. Connection Diagram for N = 4 Point FFT Computation

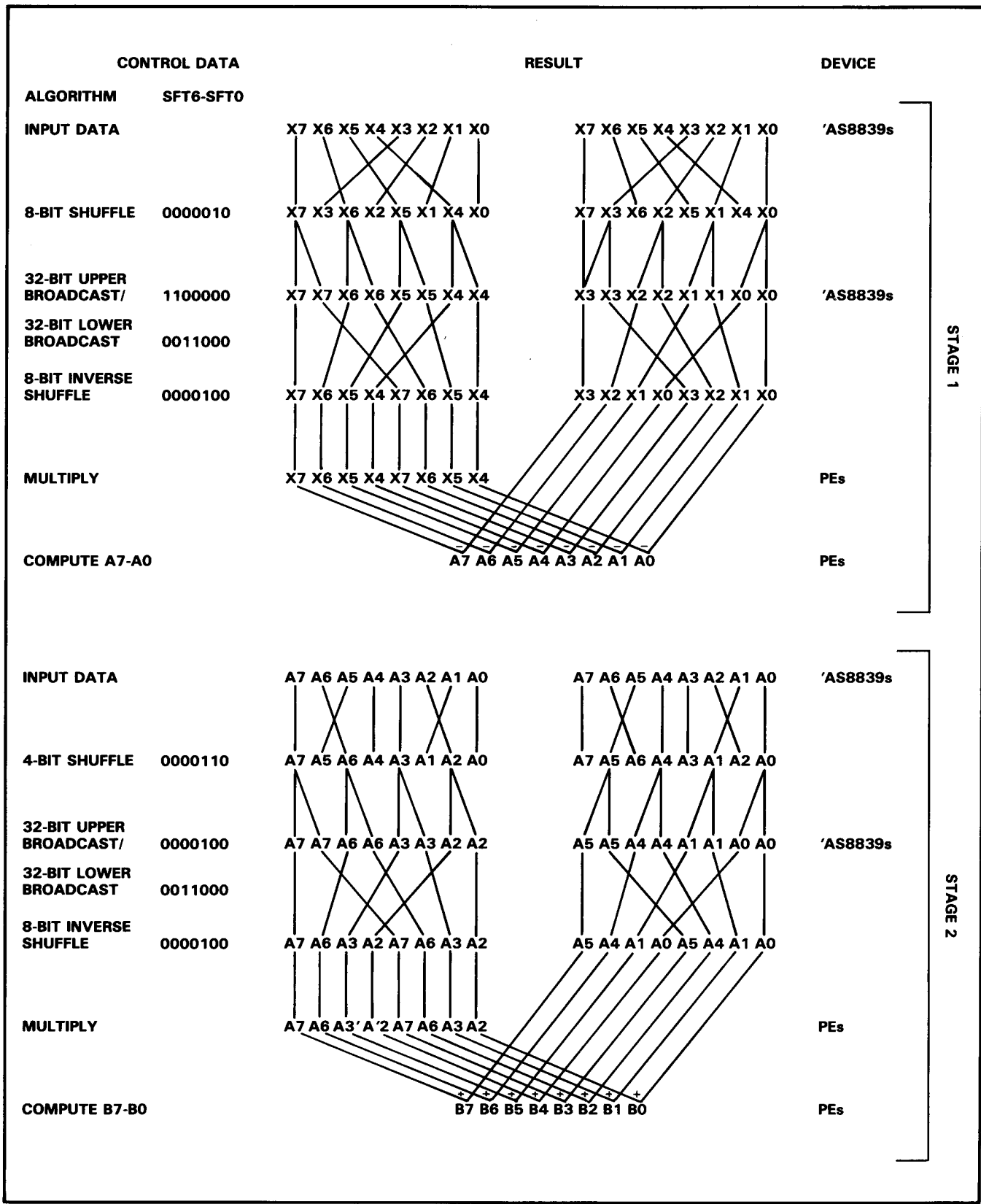


Figure 8. Data Flow for Figure 3 FFT Computation

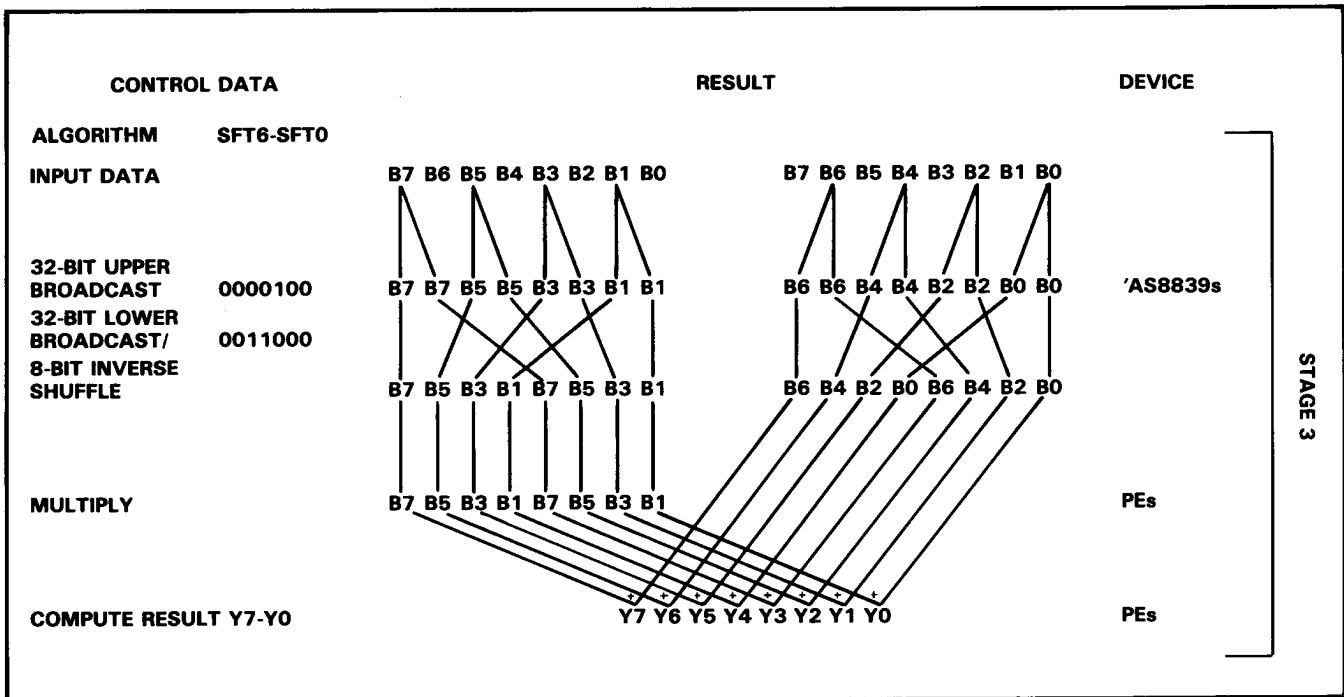


Figure 8. Data Flow for Figure 3 FFT Computation (Cont.)

Specifications

Table 6. Absolute Maximum Ratings Over Operating Temperature Range (unless otherwise noted)

Supply voltage, VCC1	7 V
Supply voltage, VCC2	3 V
Input voltage	7 V
Operating free-air temperature range: SN74AS8838	0°C to 70°C
Storage temperature range	-65°C to 150°C

Table 7. Recommended Operating Conditions

PARAMETER		SN74AS8838			UNIT
		MIN	NOM	MAX	
VCC1	I/O supply voltage	4.5	5	5.5	V
VCC2	STL internal logic supply voltage	1.9	2	2.1	V
VIH	High-level input voltage	2			V
VIL	Low-level input voltage			0.8	V
IOH	High-level output current			-2.6	mA
IOL	Low-level output current			24	mA
TC	Operating case temperature				°C
TA	Operating free-air temperature	0		70	°C

Table 8. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN74AS8839		UNIT
		MIN	MAX	
V _{IK}	V _{CC1} = 4.5 V, I _I = -18 mA		-1.2	V
V _{OH}	V _{CC1} = 4.5 V to 5.5 V, I _{IO} = -0.4 mA	V _{CC} -2		V
	V _{CC1} = 4.5 V, I _{OH} = -1 mA			
	V _{CC1} = 4.5 V, I _{OH} = -2.6 mA	2.4		
V _{OL}	V _{CC1} = 4.5 V, I _{OH} = 12 mA	0.4		V
	V _{CC1} = 4.5 V, I _{OL} = 24 mA	0.5		
I _{OZH}	V _{CC1} = 5.5 V, V _O = 2.7 V	20		μA
I _{OZL}	V _{CC1} = 5.5 V, V _I = 0.4 V	-0.4		mA
I _I	V _{CC1} = 5.5 V, V _I = 7 V	0.1		mA
I _{IH}	V _{CC1} = 5.5 V, V _I = 2.7 V	20		μA
I _{IL}	V _{CC1} = 5.5 V, V _I = 0.4 V	-0.4		mA
I _{O‡}	V _{CC1} = 5.5 V, V _O = 2.25 V	-30	-112	mA
I _{CC1}	V _{CC1} = 5.5 V	150		mA
I _{CC2}	V _{CC2} = 2.1 V	145		mA

‡The output conditions have been chosen to produce a current that closely approximates one-half the true short-circuit current, I_{OS}.

Table 9. Switching Characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V. C _L = 50 pF. R ₁ = 500 Ω. R ₂ = 500 Ω. T _A = 25°C			V _{CC} = 4.5 V to 5.5 V. C _L = 50 pF. R ₁ = 500 Ω. R ₂ = 500 Ω. T _A = 0°C to 70°C		UNIT
			SN74AS8839			SN74AS8839		
			MIN	TYP	MAX	MIN	MAX	
t _{pd}	SFT6-SFT0	Y31-Y0	18	23	25		ns	
	D31-D0	Y31-Y0	18	23	25			
t _{en}	YOEL	Y15-Y0	12	16	17		ns	
	YOEM	Y31-Y16	12	16	17			
t _{dis}	YOEL	Y15-Y0	6	8	10		ns	
	YOEM	Y31-Y16	6	8	10			

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of *The TTL Data Book Volume 3, 1984*.

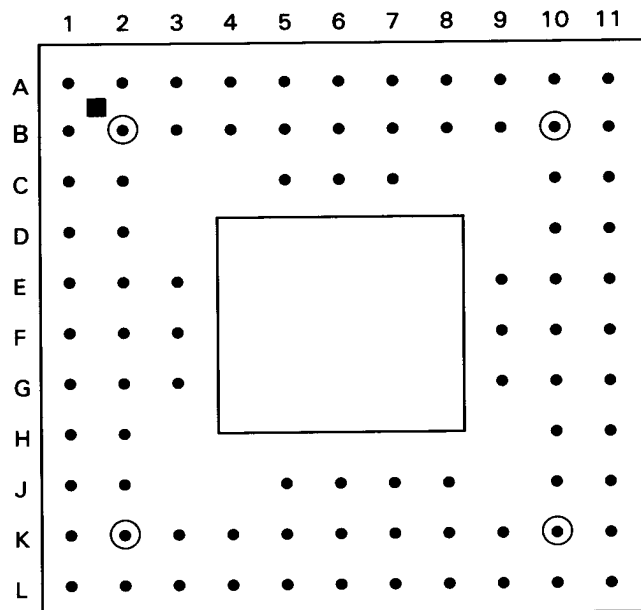
Table 10. Pin Functional Description

Pin I/O	Name	No.	Description	Pin I/O	Name	No.	Description	
D0	K7		Input data bits 0-31	VCC1	B10		5-Volt supply for TTL-compatible I/O	
D1	L7			VCC1	K1			
D2	J6			VCC2	A2		2-Volt supply for internal Schottky Transistor Logic (STL)	
D3	K6			VCC2	L10			
D4	L6			Output data bits 0 through 31	Y0	J10	0	
D5	L5				Y1	J11		
D6	K5				Y2	H10		
D7	J5				Y3	H11		
D8	L4				Y4	G9		
D9	K4				Y5	G10		
D10	L3				Y6	F11		
D11	K3				Y7	F10		
D12	L2				Y8	E11		
D13	K2				Y9	E10		
D14	J2	I			Y10	E9		
D15	J1				Y11	D11		
D16	H2				Y12	D10		
D17	H1				Y13	C11		
D18	G3				Y14	C10		
D19	G2				Y15	B11		
D20	G1				Y16	A10		
D21	F3				Y17	B9		
D22	F2				Y18	A9		
D23	F1				Y19	B8		
D24	E1				Y20	A8		
D25	E2				Y21	C7		
D26	E3				Y22	B7		
D27	D1				Y23	A6		
D28	D2				Y24	B6		
D29	C1				Y25	A5		
D30	C2				Y26	B5		
D31	B1		Y27		C5			
GND	A1		Y28		A4			
GND	A7		Y29		B4			
GND	A11		Y30		A3			
GND	B2		Y31	B3				
GND	G11							
GND	K9							
GND	L1							
NC	J8		Mechanical orientation pin					
SFT0	K11		Instruction inputs (See Tables 1-5)	\overline{YOEL}	F9	I	Control input for the Y15-Y0 output port. When \overline{YOEL} is low, Y15-Y0 are enabled.	
SFT1	K10			\overline{YOEM}	C6	I		Control input for the Y31-Y16 output port. When \overline{YOEM} is low, Y31-Y16 are enabled.
SFT2	L11							
SFT3	L9	I						
SFT4	K8							
SFT5	L8							
SFT6	J7							

Table 11. Pinout

PIN		PIN		PIN	
NO.	NAME	NO.	NAME	NO.	NAME
A1	GND	D1	D27	J6	D2
A2	VCC2	D2	D28	J7	SFT6
A3	Y30	D10	Y12	J8	N/C
A4	Y28	D11	Y11	J10	Y0
A5	Y25	E1	D24	J11	Y1
A6	Y23	E2	D25	K1	VCC1
A7	GND	E3	D26	K2	D13
A8	Y20	E9	Y10	K3	D11
A9	Y18	E10	Y9	K4	D9
A10	Y16	E11	Y8	K5	D6
A11	GND	F1	D23	K6	D3
B1	D31	F2	D22	K7	D0
B2	GND	F3	D21	K8	SFT4
B3	Y31	F9	YOEL	K9	GND
B4	Y29	F10	Y7	K10	SFT1
B5	Y26	F11	Y6	K11	SFT0
B6	Y24	G1	D20	L1	GND
B7	Y22	G2	D19	L2	D12
B8	Y19	G3	D18	L3	D10
B9	Y17	G9	Y4	L4	D8
B10	VCC1	G10	Y5	L5	D5
B11	Y15	G11	GND	L6	D4
C1	D29	H1	D17	L7	D1
C2	D30	H2	D16	L8	SFT5
C5	Y27	H10	Y2	L9	SFT3
C6	YOEM	H11	Y3	L10	VCC2
C7	Y21	J1	D15	L11	SFT2
C10	Y14	J2	D14		
C11	Y13	J5	D7		

Table 12. SN74AS8838
GB Pin-Grid-Array Package
(Top View)



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