

POWER FACTOR CORRECTOR

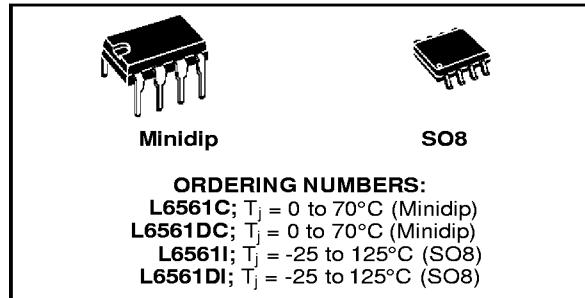
PRODUCT PREVIEW

- VERY PRECISE ADJUSTABLE OUTPUT OVERVOLTAGE PROTECTION
- MICRO POWER START-UP CURRENT (50 μ A TYP.)
- VERY LOW OPERATING SUPPLY CURRENT (4mA TYP.)
- INTERNAL START-UP TIMER
- CURRENT SENSE FILTER ON CHIP
- DISABLE FUNCTION
- INTERNAL 1% @ 25°C REFERENCE PRECISION
- TRANSITION MODE OPERATION
- TOTEM POLE OUTPUT CURRENT: ± 400 mA
- DIP8/SO8 PACKAGES

DESCRIPTION

L6561 is the improved version of the L6560 standard Power Factor Corrector. Fully compatible with the standard version, it has a superior performant multiplier making the device capable to work in the wide input voltage range applications (from 85V to 265V) with an excellent THD, further the start up current has been reduced at few tens of μ A and new function as disable has been implemented on the ZCD pin guaranteeing very low current consumption in stand by mode. Realised in mixed BCD technology, the chip gives the following benefits:

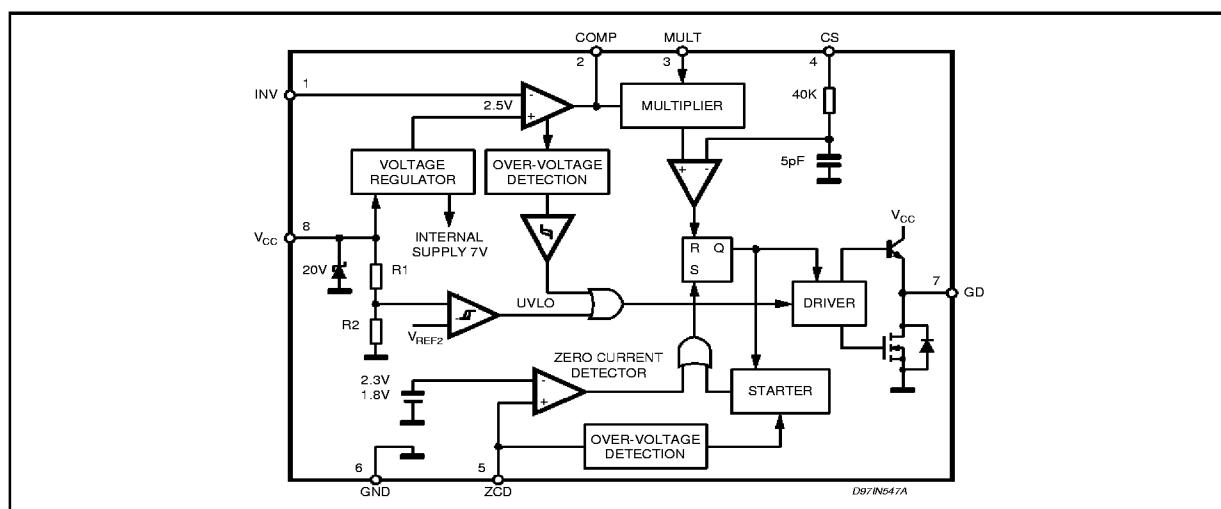
BLOCK DIAGRAM



- micro power start up current
- 1% precision internal reference voltage ($T_j 25^\circ\text{C}$)
- Soft Output Over Voltage Protection
- no need for external low pass filter on the current sense
- very low operating quiescent current minimises power dissipation

The totem pole output stage is capable of driving a Power MOS or IGBT with source and sink currents of ± 400 mA. The device is operating in transition mode and it is optimised for Electronic Lamp Ballast application, AC-DC adaptors and SMPS.

Due to the very limited power dissipation, in first approximation the junction temperature can be considered equal to the ambient temperature.



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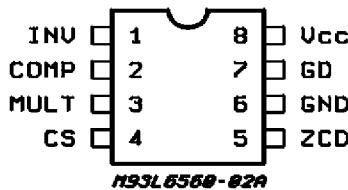
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This is preliminary information on a new product now in development. Details are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Symbol	Pin	Parameter	Value	Unit	
I_{VCC}	8	$I_{CC} + I_Z$	30	mA	
I_{GD}	7	Output Totem Pole Peak Current (2μs)	±700	mA	
INV, COMP MULT	1, 2, 3	Analog Inputs & Outputs	-0.3 to 7	V	
CS	4	Current Sense Input	-0.3 to 7	V	
ZCD	5	Zero Current Detector	50 (source) -10 (sink)	mA mA	
P_{tot}		Power Dissipation @ $T_{amb} = 50^{\circ}\text{C}$	(Minidip) (SO8)	1 0.65	W
T_j		Junction Temperature Operating Range		-25 to 150	°C
T_{stg}		Storage Temperature		-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO 8	MINIDIP	Unit
$R_{th j-amb}$	Thermal Resistance Junction-ambient	150	100	°C/W

PIN FUNCTIONS

N.	Name	Function
1	INV	Inverting input of the error amplifier. A resistive divider is connected between output regulated voltage and this point, to provide the voltage feedback.
2	COMP	Output of error amplifier. A feedback compensation network is placed between this pin and the INV pin.
3	MULT	Input of the multiplier stage. A resistive divider connects to this pin the rectified mains. A voltage signal, proportional to the rectified mains, appears on this pin.
4	CS	Input to the comparator of the control loop. The current is sensed by a resistor and the resulting voltage is applied to this pin.
5	ZCD	Zero current detection input. If it is connected to GND, the device is disabled.
6	GND	Ground of the control section.
7	GD	Gate driver output. A push pull output stage is able to drive the Power MOS with peak current of 400mA (source and sink).
8	Vcc	Supply voltage of driver and control circuits.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 14.5V$; $T_{amb} = 0$ to $70^{\circ}C$ for L6561C; $T_{amb} = -25^{\circ}C$ to $125^{\circ}C$ for L6561I; unless otherwise specified)

SUPPLY VOLTAGE SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	8	Operating Range	after turn-on	11		18	V
$V_{CC\ ON}$	8	Turn-on Threshold		11.5	13	14.5	V
$V_{CC\ OFF}$	8	Turn-off Threshold		9	10	11	V
Hys	8	Hysteresis		2.5	3	3.8	V

SUPPLY CURRENT SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{START-U}$	8	Start-up Current	before turn-on at: $V_{CC} = 10V$	20	50	100	μA
I_{CC}	8	Operating Supply Current	$C_L = 0nF @ 70KHz$		3.5	5	mA
			$C_L = 1nF @ 70KHz$		4	6	mA
			in OVP condition $V_{pin1} = 2.7V$		1.2	2	mA
V_Z	8	Zener Voltage	$I_{CC} = 25mA$	18	20	22	V

ERROR AMPLIFIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INV}	1	Voltage Feedback Input Threshold	$T_{amb} = 25^{\circ}C$	2.465	2.5	2.535	V
			$12V < V_{CC} < 18V$	2.44		2.56	
		Line Regulation	$V_{CC} = 11$ to $18V$		1	4	mV
I_{INV}	1	Input Bias Current			0.1	1	μA
G_V		Voltage Gain	Open loop	60	80		dB
I_{COMP}	2	Source Current ($V_1 < V_{ref}$)	$V_{COMP} = 5V$	-2	-4	-8	mA
		Sink Current ($V_1 > V_{ref}$)		3	4.5		mA

MULTIPLIER SECTION

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{MULT}	3	Operating Voltage		0 to 2.5	0 to 3.5		V
$\frac{\Delta V_{CS}}{\Delta V_{mult}}$		Output Max. Slope	$V_{MULT} = \text{from } 0V \text{ to } 1V$ $V_{COMP} = 6V$		1.6		
K		Gain	$V_{MULT} = 1V$ $V_{COMP} = 5V$	0.45	0.65	0.85	1/V

CURRENT SENSE COMPARATOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CS}	4	Voltage Threshold	$V_{MULT} = 2.5V$ $V_{COMP} = 6V$	1.5		2	V
I_{CS}	4	Input Bias Current	$V_{OS} = 0$		0.05	0.5	μA
$t_d(H-L)$	4	Delay to Output			200	400	ns



ELECTRICAL CHARACTERISTICS (continued)
ZERO CURRENT DETECTOR

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{ZCD}	5	Input Threshold Voltage Rising Edge		1.8		2.3	V
		Hysteresis		0.3	0.5	0.7	V
V_{ZCD}	5	Clamp Voltage	$I_{ZCD} = 3\text{mA}$	5	5.7	6.4	V
V_{ZCD}	5	Clamp Voltage	$I_{ZCD} = -3\text{mA}$	0.4	0.7	1	V
I_{ZCD}	5	Sink Bias Current	$1\text{V} \leq V_{ZCD} \leq 5\text{V}$		2		μA
I_{ZCD}	5	Source Bias Current			3		mA
V_{DIS}	5	Disable threshold			200		mV

OUTPUT SECTION

V_{GD}	7	Dropout Voltage	$I_{GDsource} = 200\text{mA}$		1.2	2	V
			$I_{GDsource} = 20\text{mA}$		0.7	1	V
			$I_{GDSink} = 200\text{mA}$			1.5	V
			$I_{GDSink} = 20\text{mA}$			0.3	V
t_r	7	Output Voltage Rise Time	$CL = 1\text{nF}$		50	120	ns
t_f	7	Output Voltage Fall Time	$CL = 1\text{nF}$		40	100	ns
$UVLO_{SAT}$		UVLO Saturation	$V_{CC} = 3\text{V} \text{ to } V_{CCON}, I_{sink} = 10\text{mA}$		0.1	0.3	V

OUTPUT OVERVOLTAGE SECTION

I_{OVP}	2	OVP Triggering Current		36	40	44	μA
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RESTART TIMER

t_{START}		Start Timer		70	150	400	μs
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OVER VOLTAGE PROTECTION OVP

The output voltage is expected to be kept by the operation of the PFC circuits close to its reference value that is set by the ratio of the two external resistors R_1 and R_2 (see fig. 2), taking into consideration that the non inverting input of the error amplifier is biased inside the L6561 at 2.5V. In steady state conditions, the current through R_1 and R_2 is:

$$I_{sc} = \frac{\Delta V_{outsc} - 2.5}{R_1}$$

$$\text{or } I_{sc} = \frac{2.5}{R_2}$$

and, if the external compensation network is made only with a capacitor C , the current through C is equal zero.

When the output voltage increases abruptly the current through R_1 becomes:

$$I_{R1} = \frac{V_{out} - 2.5}{R_1}$$

$$I_{R1} = \frac{V_{outsc} + \Delta V_{OUT} - 2.5}{R_1} = I_{sc} + \Delta I.$$

Since the current through R_2 doesn't change, the

ΔI current must flow through the capacitor C and enter in the error amplifier.

This current is mirrored inside the L6561, and compared with a precise internal reference of $40\mu\text{A}$. Whenever such $40\mu\text{A}$ limit is exceed, the OVP protection is triggered (Dynamic OVP), and the external power transistor is switched off, until the overvoltage situation disappears. However if the overvoltage persists, before that the transient condition of dynamic circuit exhausts, an internal comparator (Static OVP) latches the OVP condition keeping the external power switch turned off (see fig. 1).

The OVP value is therefore set by the equation:

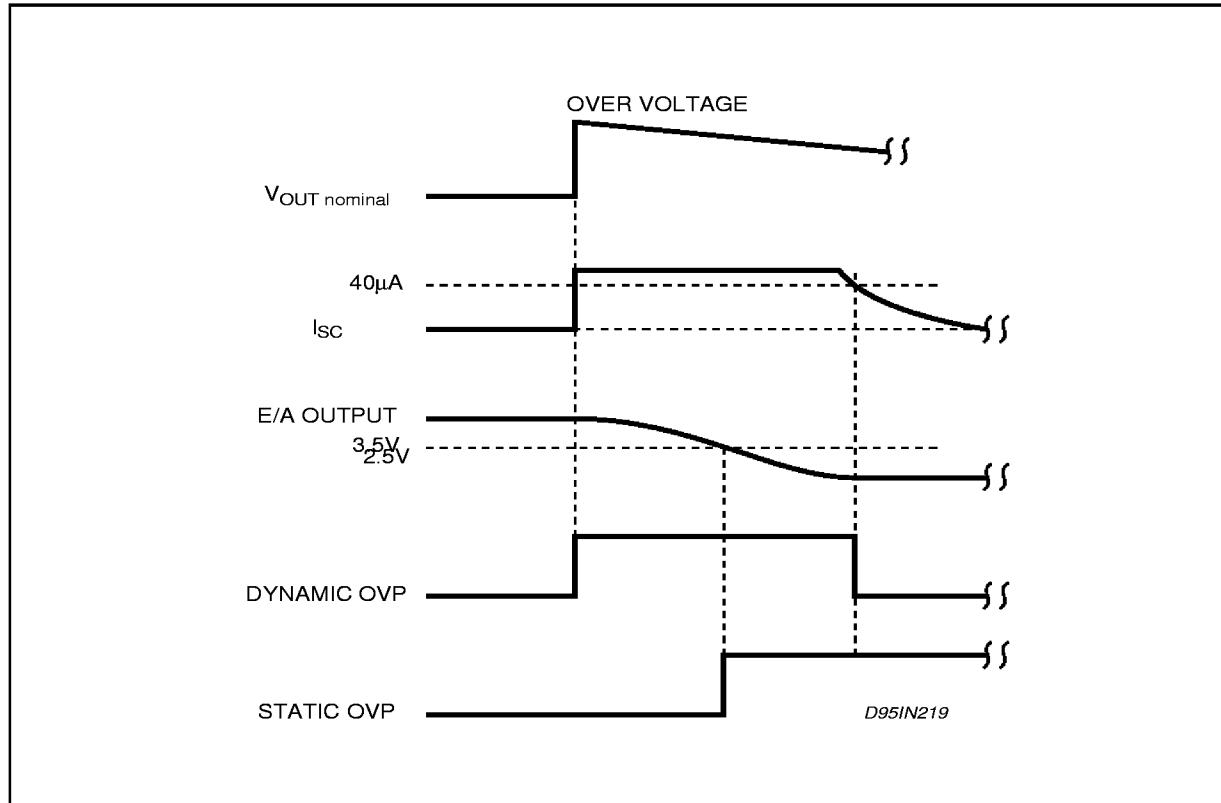
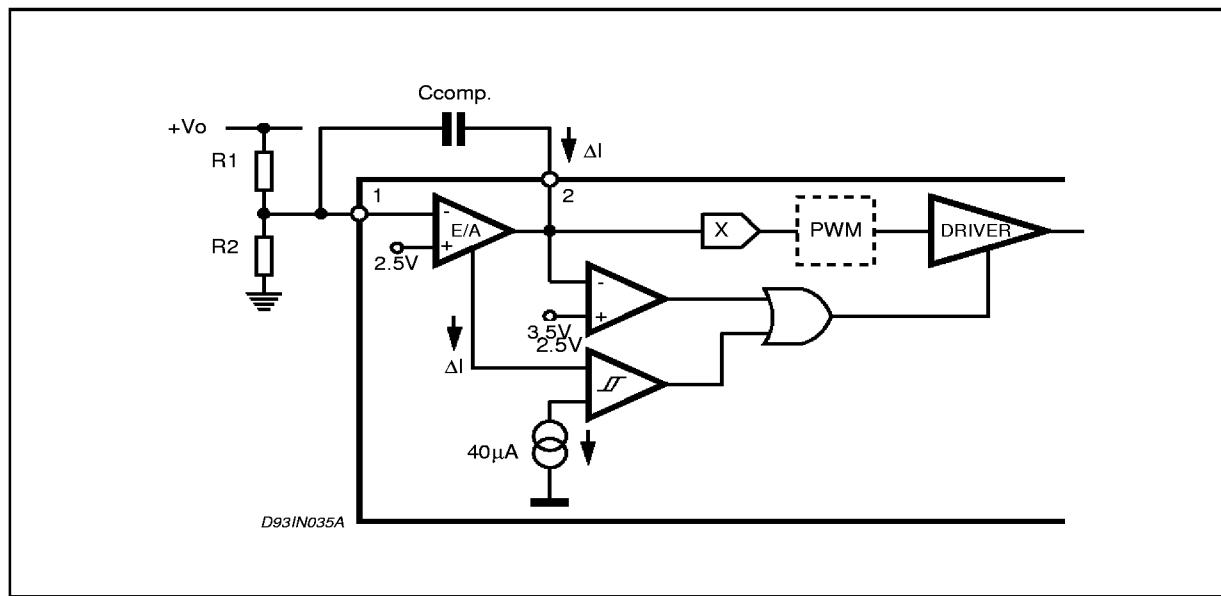
$$OVP = \Delta V_{out} = R_1 \cdot 40\mu\text{A}.$$

Typical values for R_1 , R_2 and C are reported in the application circuit. The overvoltage can be set independently from the average output voltage. The precision in setting the overvoltage threshold is 7% of the overvoltage value (for instance $\Delta V = 60\text{V} \pm 4.2\text{V}$).

Disable function

The zero current detector (ZCD) pin can be used for device disabling as well. Grounding the ZCD voltage the device is disabled reducing the supply current consumption at 1.2mA typical (@ 14.5V supply voltage).

Releasing the ZCD pin the internal start-up timer will restart the device.

Figure 1.**Figure 2. Overvoltage Protection Circuit**

L6561

Figure 3. Typical Application Circuit (80W, 110VAC)

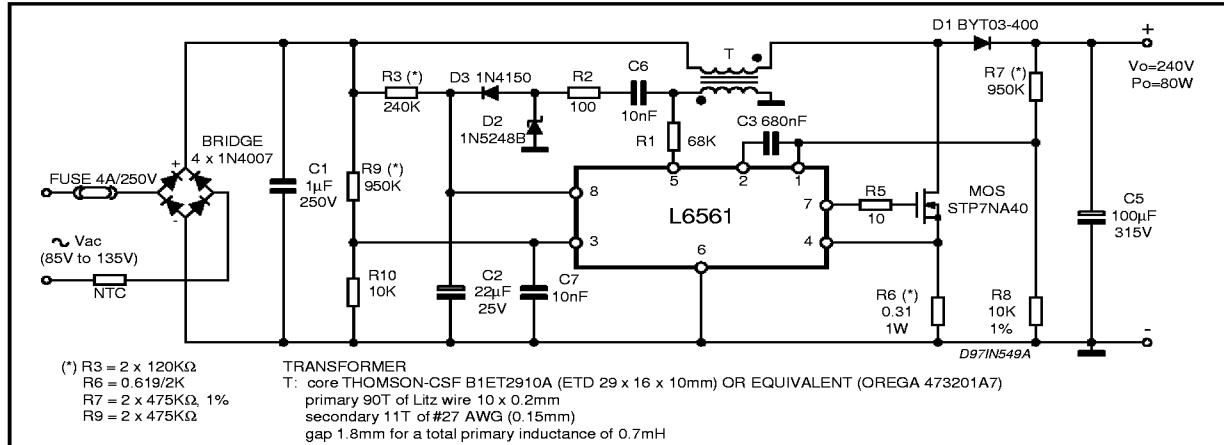


Figure 4. Typical Application Circuit (120W, 220VAC)

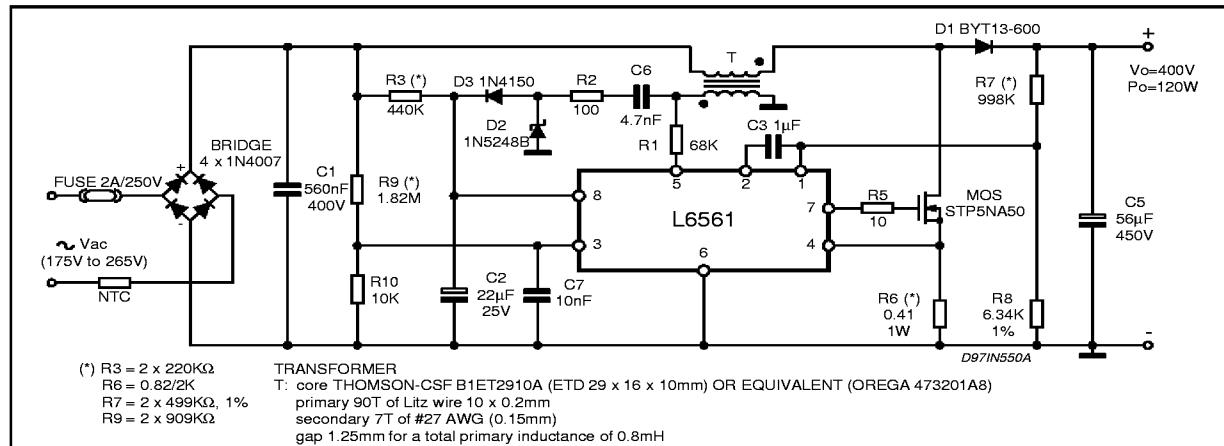


Figure 5. Wide-Range Application (80W)

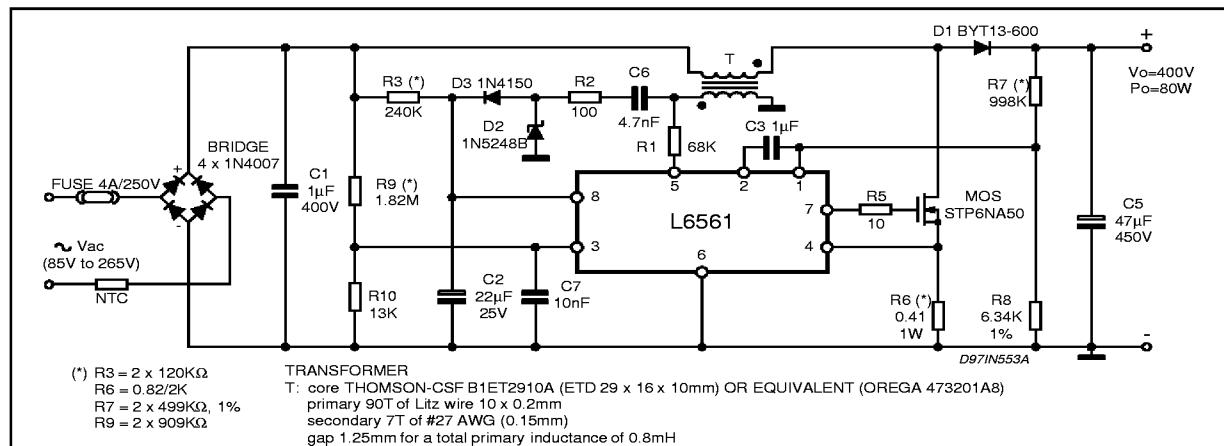


Figure 6. P.C. Board and Components Layout of the Figg. 3, 4 and 5 (1:1.25 scale)

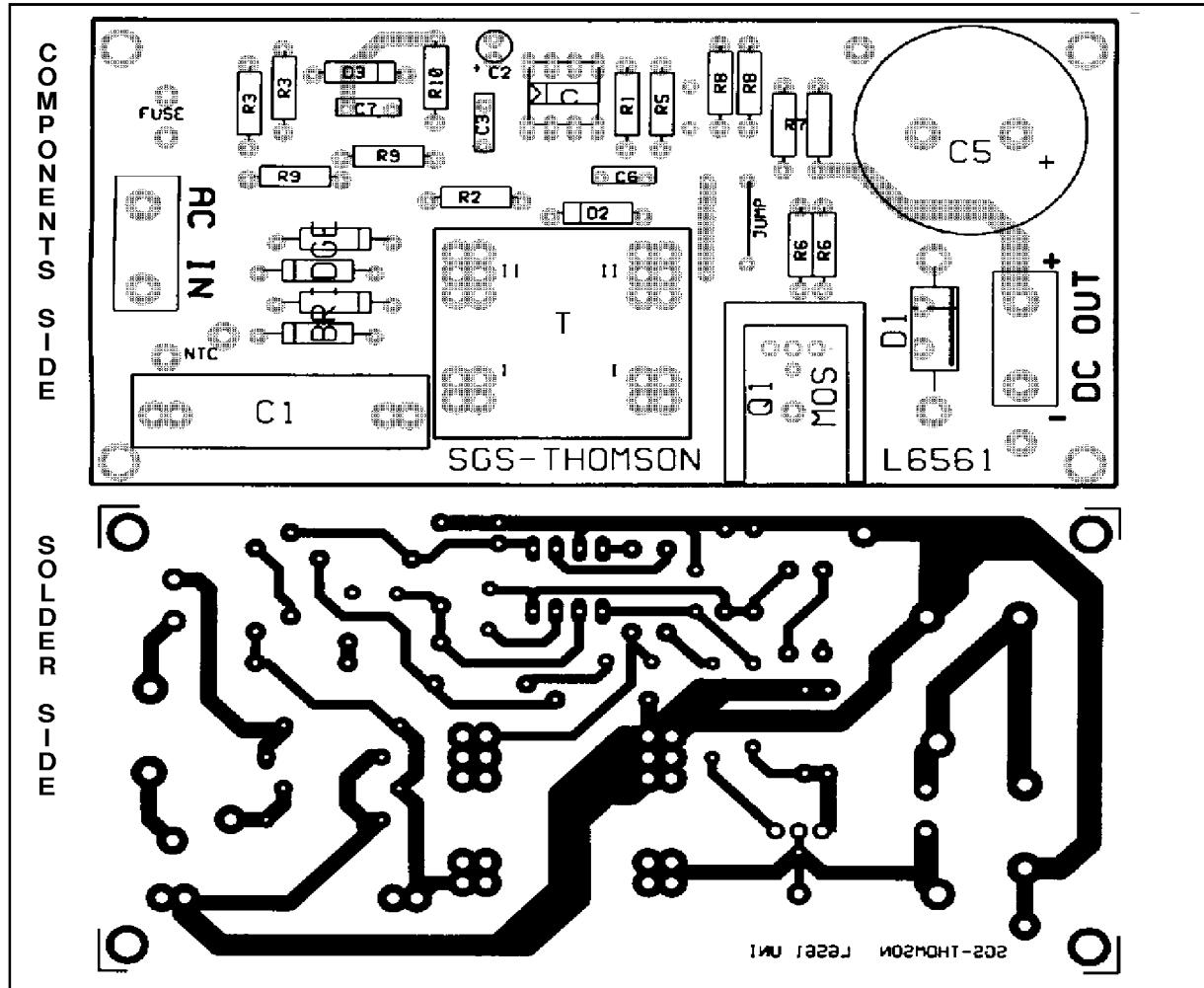


Figure 7. OVP Current Threshold vs. Temperature

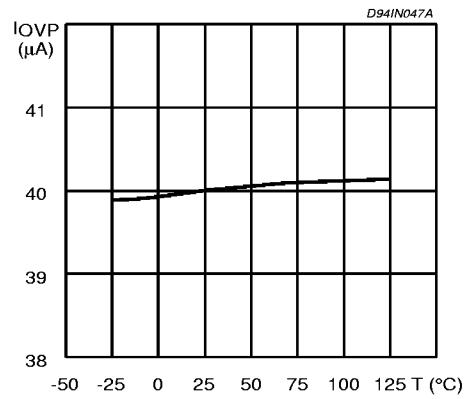


Figure 8. Undervoltage Lockout Threshold vs. Temperature

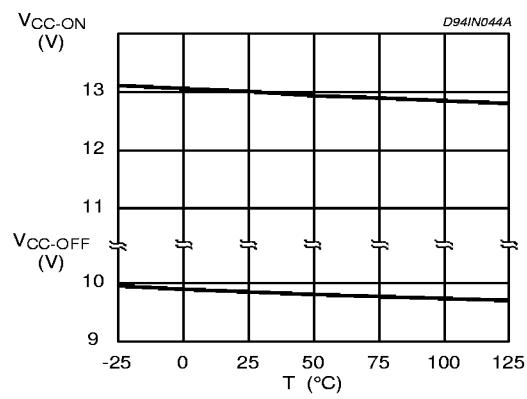


Figure 9. Supply Current vs. Supply Voltage

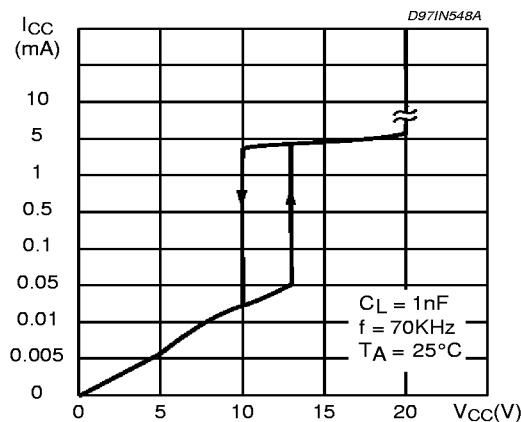


Figure 10. Voltage Feedback Input Threshold vs. Temperature

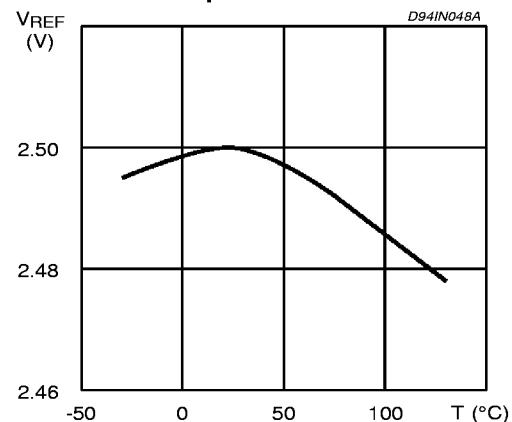


Figure 11. Output Saturation Voltage vs. Sink Current

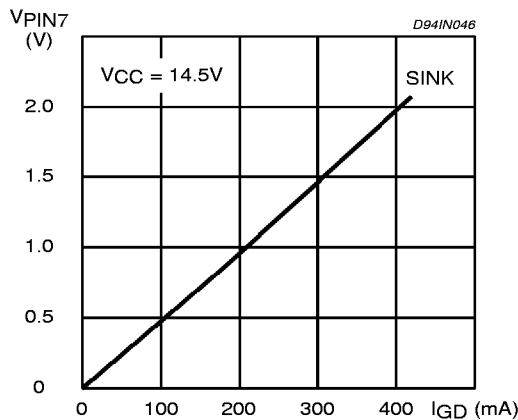


Figure 12. Output Saturation Voltage vs. Source Current

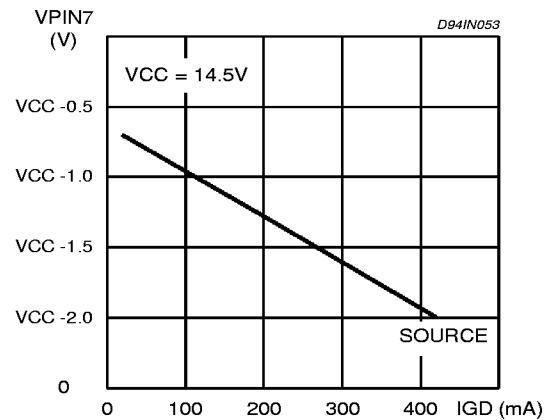
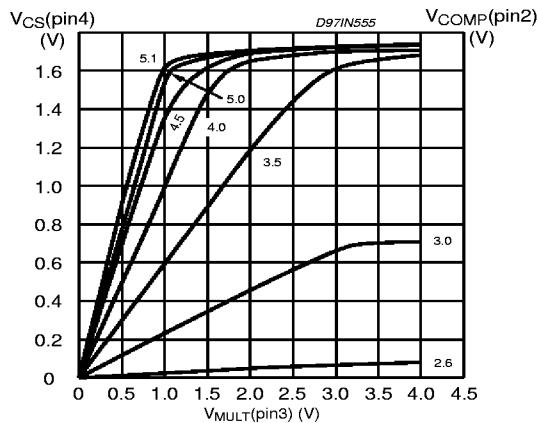
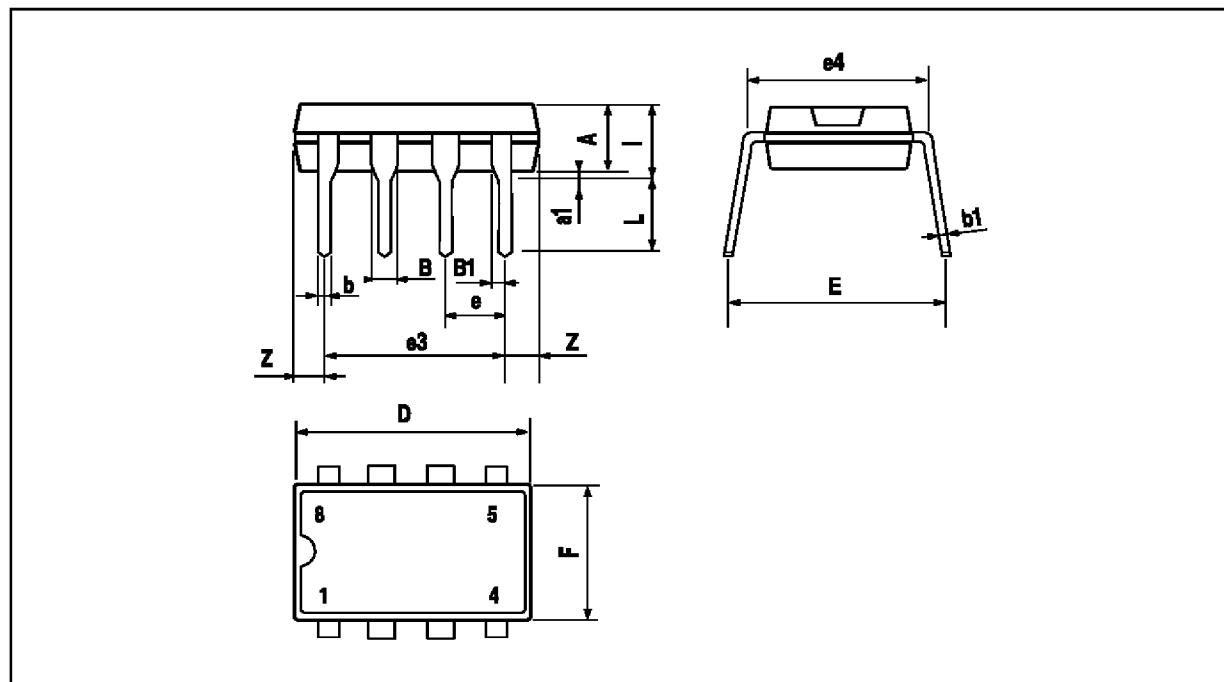


Figure 13. Multiplier Characteristics Family



MINIDIP PACKAGE MECHANICAL DATA

DIM	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



SO8 PACKAGE MECHANICAL DATA

DIM	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

