ADC0804/D, ADC0804/W
8-Bit μP-Compatible A/D Converters

GENERAL DESCRIPTION

The Intersil ADC0804 is a CMOS 8-bit successive approximation A/D converter which uses a modified potentiometric ladder and is designed to operate with the 8048 control bus via three-state outputs. The converter appears to the processor as a memory location or I/O port, hence no interfacing logic is required.

The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

ORDERING INFORMATION

Part Number	Temperature	Form
ADC0804/D	+25°C	Dice
ADC0804/W	+25°C	Wafer

FEATURES

- **80C48 and 80C80/85 Bus Compatible—No Interfacing Logic Required**
- **Conversion Time < 100 μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works With Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single +5V Supply)**
- **No Zero-Adjust Required**

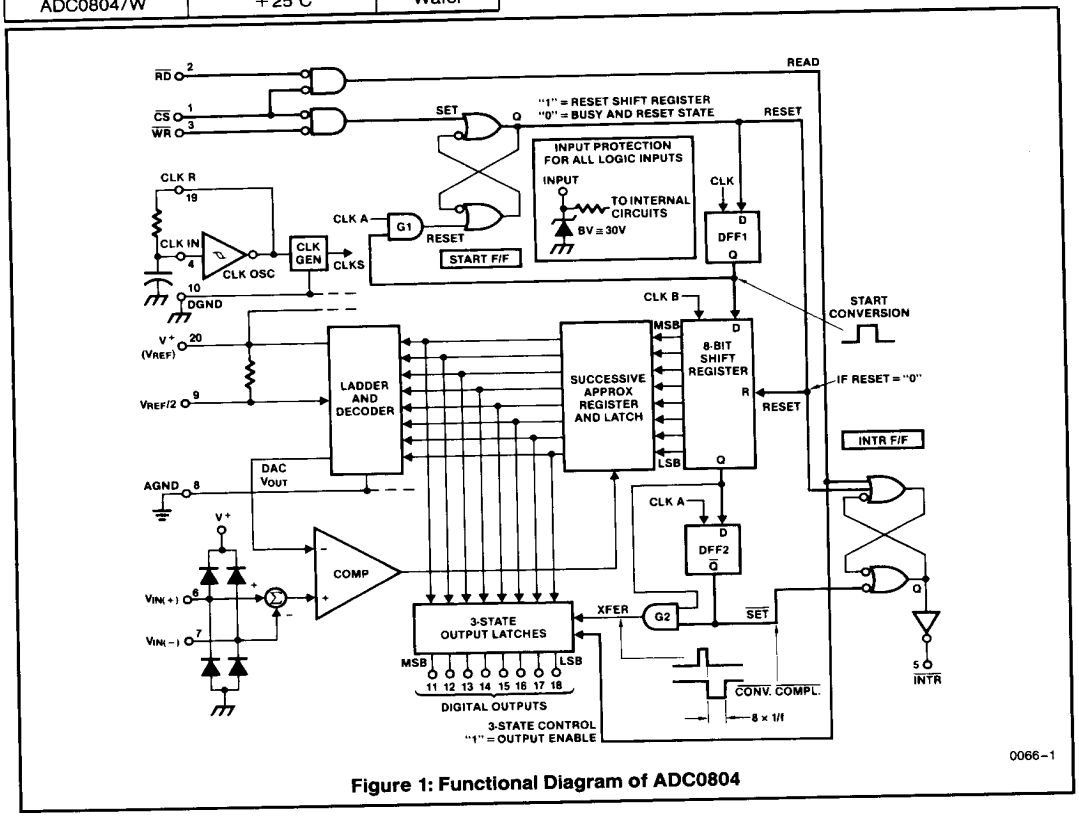

Figure 1: Functional Diagram of ADC0804

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NOTE: All typical values have been characterized but are not tested.

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ADC0804/D, ADC0804/W

ABSOLUTE MAXIMUM RATINGS

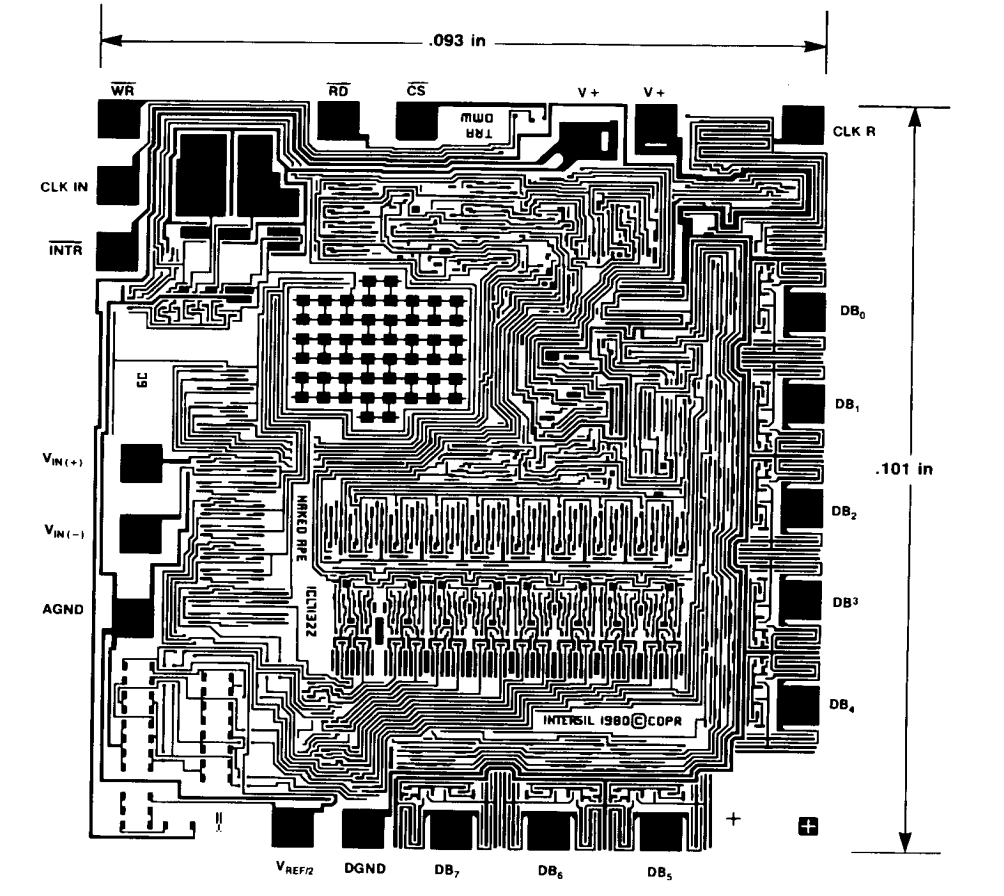
Supply Voltage 6.5V
Voltage at Any Input ..... −0.3V to (V^+ + 0.3V)

OPERATING RATINGS

Supply Voltage Range ..... 4.5V to 6.3V

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

CHIP TOPOGRAPHY



Pad size = 0.005 x 0.005 in.

Figure 2

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ELECTRICAL CHARACTERISTICS (Notes 1 and 5)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_A = 25°C$, and $f_{CLK} = 640$ kHz unless otherwise stated

Parameter	Test Conditions	Min	Max	Units
ADC0804: Total Unadjusted Error	Completely Unadjusted		±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	0.8		kΩ

DC ELECTRICAL CHARACTERISTICS

Digital Levels and DC Specifications: $V^+ = 5V$, $T_A = 25°C$, unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
CONTROL INPUTS (Note 4)					
V^+_{CLK}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.5	V
V^-_{CLK}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	2.1	V
V_H	CLK IN (Pin 4) Hysteresis $(V^+_{CLK})-(V^-_{CLK})$		0.6	2.0	V
I^+	Supply Current (Includes Ladder Current)	$f_{CLK} = 640$ kHz, $T_A = +25°C$ and $\overline{CS}$ = HI		2.5	mA
DATA OUTPUTS AND $\overline{INTR}$					
V_{OL}	Logical "0" Output Voltage	$I_O = 1.6$ mA, $V^+ = 4.75V$		0.4	V
V_{OH}	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V^+ = 4.75V$	2.4		V
I_{LO}	3-State Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−3	3	μA μA
I_{SOURCE}	Output Short Circuit Current	V_{OUT} Short to GND, $T_A = +25°C$	4.5		mA
I_{SINK}	Output Short Circuit Current	V_{OUT} Short to V^+, $T_A = 25°C$	9.0		mA

NOTE 1: All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

2: For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.

3: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

4: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

5: None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this.

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