ICM7170/D, ICM7170/W
μP-Compatible Real-Time Clock

PRELIMINARY
Specifications Subject To Change Without Notice

INTERSIL

GENERAL DESCRIPTION

The ICM7170 real-time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silcon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $1/100$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{acc}) of 300 ns eliminates the need for any microprocessor wait states or software overhead. Furthermore, the ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts. The first type is the periodic interrupt (i.e., 100 Hz, 10 Hz, etc.) which can be programmed by the internal interrupt control register to provide 7 different output signals. The second type is the alarm interrupt. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power-Down Detector eliminates the need for external components to support the battery back-up function. When a power-down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Input/output and read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

FEATURES

- **8-Bit μP Bus Compatible —Multiplexed or Direct Addressing**
- **Binary Time Data Format Lowers Software Overhead**
- **Time From $1/100$ Seconds to 99 Years**
- **Software Selectable 12/24 Hour Format**
- **Latched Time Data Ensures No Roll-Over During Read**
- **Full Calendar With Automatic Leap Year Correction**
- **On-Chip Battery Backup Switchover Circuit**
- **Access Time Less Than 300 ns**
- **4 Programmable Crystal Oscillator Frequencies**
- **On-Chip Alarm Comparator and RAM**
- **Interrupts From Alarm and 6 Selectable Periodic Intervals**
- **Standby Micro-Power Operation: 2 μA Typ. at 3.0V with 32 kHz Crystal**

APPLICATIONS

- **Portable and Personal Computers**
- **Industrial Control Systems**
- **Data Logging**
- **Point of Sale**

ORDERING INFORMATION

Part Number	Temperature	Form
ICM7170/D	+25°C	Dice
ICM7170/W	+25°C	Wafer

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 8V

Input Voltage (Any Terminal)
(Note 2) ..... V_{DD} + 0.3V to V_{SS} − 0.3V

Operating Temperature ..... −40°C to +85°C

Storage Temperature ..... −65°C to +150°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

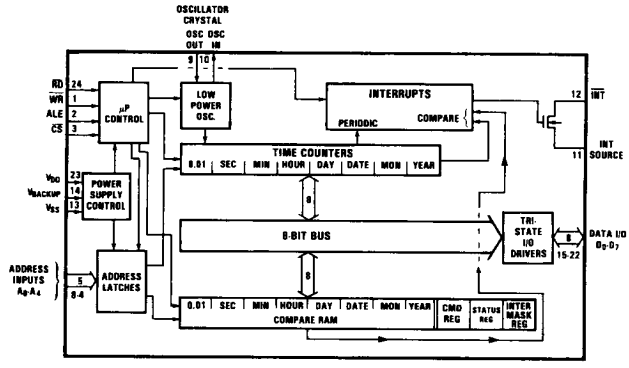

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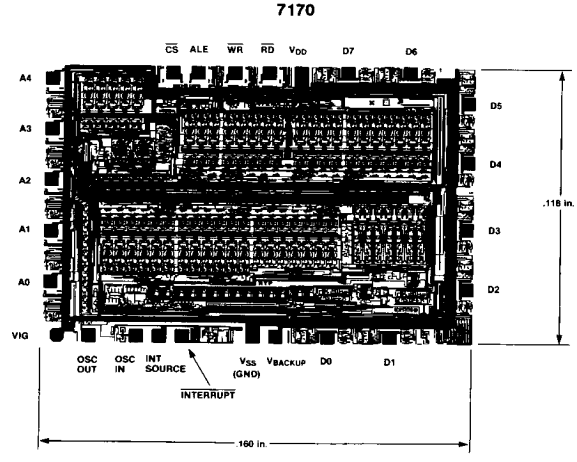
Figure 1: Functional Diagram

CHIP TOPOGRAPHY



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Pad size = 5 x 5 mils.

Figure 2

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS $T_A = 25°C$, $V_{DD} = +5V \pm 10\%$, $V_{BACKUP} = V_{DD}$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Test Conditions		Specification			Units
				Min	Typ	Max	
V_{DD}	V_{DD} Supply Range (32 kHz/4 MHz)			2.6		5.5	V
$I_{STBY\ (1)}$	Standby Current	F_{XTAL} = 32 kHz Pins 1–8, 15–22 & 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0V$			2.0	20	μA
$I_{STBY\ (2)}$	Standby Current	F_{XTAL} = 4 MHz Pins 1–8, 15–22 & 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0V$			20	150	μA
$I_{DD\ (1)}$	Operating Supply Current	F_{XTAL} = 32 kHz Read/Write Operation at 100 Hz			0.3	1.2	mA
$I_{DD\ (2)}$	Operating Supply Current	F_{XTAL} = 32 kHz Read/Write Operation at 1 MHz			1.0	2.0	mA
V_{IL}	Input Low Voltage	V_{DD} = 4.5V				0.8	V
V_{IH}	Input High Voltage	V_{DD} = 4.5V		3.5			V
V_{OL}	Output Low Voltage Except $\overline{INTERRUPT}$	I_{OL} = 1.6 mA				0.4	V
V_{OH}	Output High Voltage Except $\overline{INTERRUPT}$	I_{OH} = 400 μA		2.4			V
I_L	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
I_{OL}	Tristate Leakage Current (D_0–D_7)	$V_0 = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
$V_{BATTERY}$	Backup Battery Voltage	F_{XTAL} = 1, 2, 4 MHz		2.6		3.2	V
$V_{BATTERY}$	Backup Battery Voltage	F_{XTAL} = 32 kHz			2.0	3.2	V
V_{OL}	Output Low Voltage $\overline{INTERRUPT}$	I_{OL} = 1.6 mA	INT SOURCE Connected to V_{SS}			0.4	V
I_{OL}	Leakage Current $\overline{INTERRUPT}$	$V_0 = V_{DD}$ or V_{SS}			10		μA

NOTE: All typical values have been characterized but are not tested.

ICM7170/D, ICM7170/W

INTERSIL

AC CHARACTERISTICS

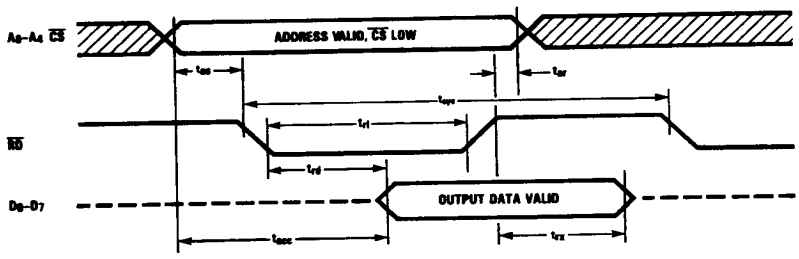
$T_A = 25°C$, $V_{DD} = +5V \pm 10\%$, D_0–D_7 $V_{BACKUP} = V_{DD}$, Load Capacitance = 150 pF, $V_{IL} = 0.4V$, $V_{IH} = 3.5V$ unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
READ CYCLE TIMING					
t_{rd}	READ to DATA Valid		170	260	ns
t_{acc}	ADDRESS Valid to DATA Valid		200	300	ns
t_{cyc}	READ Cycle Time	400			ns
t_{rx}	$\overline{RD}$ High to Bus Tristate		85	120	ns
t_{as}	ADDRESS to READ Set Up Time*		100		ns
t_{ar}	ADDRESS HOLD Time after READ*	0			ns
t_{rl}	READ pulse width, low*	0.25		9,000*	μs
WRITE CYCLE TIMING					
t_{ad}	ADDRESS Valid to WRITE Strobe	100			ns
t_{wa}	ADDRESS Hold Time for WRITE	0			ns
t_{wl}	WRITE Pulse Width, Low	100			ns
t_{dw}	DATA IN to WRITE Set Up Time	100			ns
t_{wd}	DATA IN Hold Time After WRITE	30	10		ns
t_{cyc}	WRITE Cycle Time	400			ns
MULTIPLEXED MODE TIMING					
t_{ll}	ALE Pulse Width, High	50			ns
t_{al}	ADDRESS to ALE Set Up Time	30			ns
t_{la}	ADDRESS Hold Time after ALE	30			ns

*Guaranteed parameter by design (not 100% tested).

NOTE: All typical values have been characterized but are not tested.

Read Cycle Timing for Non-Multiplexed Bus (ALE = "1", $\overline{WR}$ = 1)



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Write Cycle Timing for Non-Multiplexed Bus (ALE = "1", $\overline{RD}$ = 1)

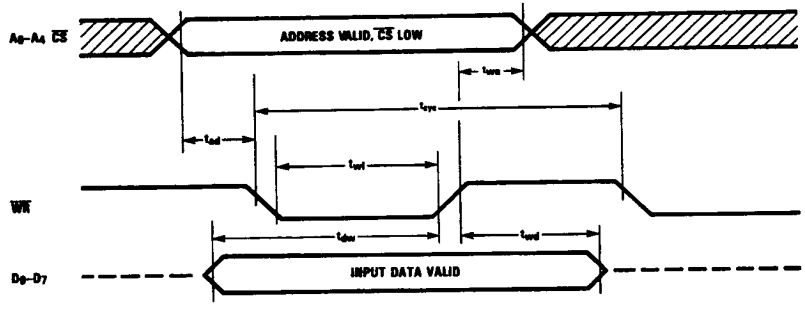

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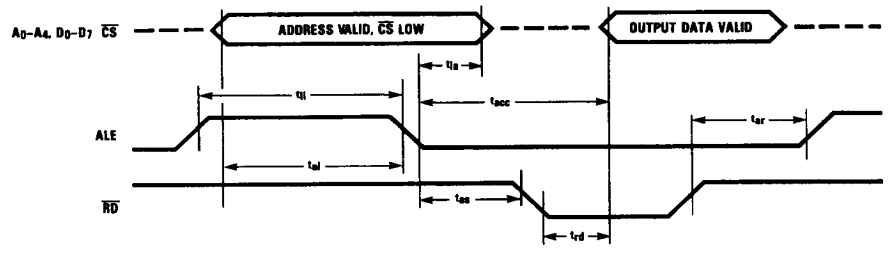
Figure 3: Timing Diagrams—Non-Multiplexed Bus

NOTE: All typical values have been characterized but are not tested.

Read Cycle Timing for Multiplexed Bus ($\overline{WR}$ = 1)



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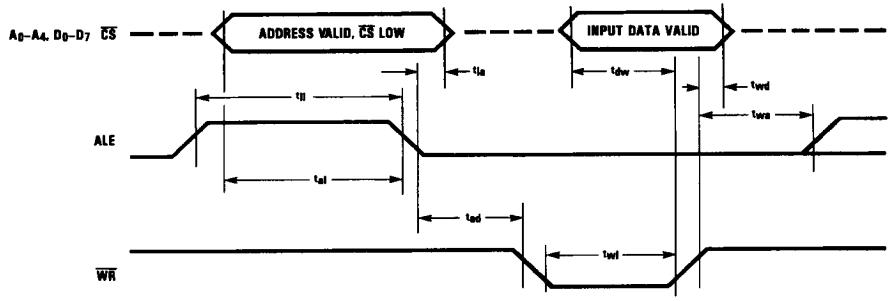
Write Cycle Timing for Multiplexed Bus ($\overline{RD}$ = 1)



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NOTE: The A0 to A4 address inputs may be connected to the D0 to D4 data lines when a multiplexed bus is used.

Figure 4: Timing Diagrams—Multiplexed Bus

NOTE: All typical values have been characterized but are not tested.