GSM/DCS1800/PCS1900 Voiceband Baseband Codec

AD6421

FEATURES

Complete Analog/Digital Interface for
- **Voiceband Input/Output-Signals**
- **Baseband Input/Output-Signals**
- **Auxiliary/Control-Signals**

Voiceband Codec
- **Complete Linear Coded Codec**
- **Two Channel 16-Bit A/D Converter with Filter**
- **Two Channel 16-Bit D/A Converter with Filter**
- **Dedicated Buzzer Output**
- **32Ω Speaker Drive Capability**
- **Programmable Gain on Input and Output**
- **Serial Voice Port**

Baseband Codec
- **Differential I and Q Inputs/Outputs**
- **On-Chip Burst Store**
- **GMSK Modulator**
- **Two 10-Bit D/A Converters**
- **Two 15-Bit A/D Converters**
- **On-Chip FIR-Filter**
- **Serial Baseband Port**

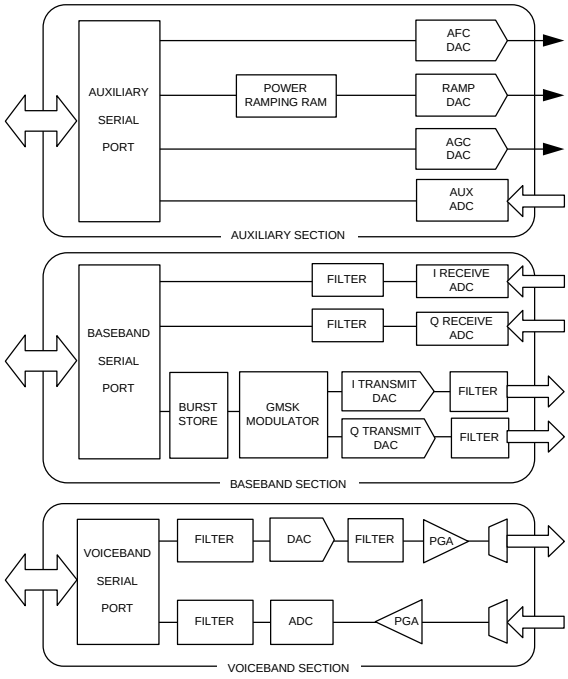
Auxiliary Section
- **Support for AGC, AFC and Power Ramping**
- **10-Bit AGC D/A Converter**
- **13-Bit AFC D/A Converter**
- **10-Bit RAMP D/A Converter with 4X Interpolator**
- **On-Chip RAMP-RAM**
- **Four Channel 10-Bit A/D-Converter**
- **Serial Auxiliary Port**

Individual Power Down Features
JTAG Interface
2.7V to 3.3V Operation
64-Lead TQFP

APPLICATIONS
GSM/ DCS1800/ PCS1900 Mobile Radios

GENERAL DESCRIPTION

The AD6421 is a monolithic Voiceband Baseband Codec (VBC) that combines on a single chip all A/D and D/A converters that are necessary to build a complete GSM, DCS1800 or PCS1900 mobile radio. It contains complete codecs for voiceband and baseband signals as well as D/A converters to control the radio subsystem and an auxiliary A/D converter for monitoring purposes.
The voiceband codec is a complete analog front-end which can interface directly with a microphone and speaker. For interfacing with external car-kits, separate input and output channels are provided. Input and output gains are user programmable for maximum flexibility.



Functional Block Diagram

The baseband codec is a complete low power, two channel, input/output port with signal conditioning. The transmit path consists of an on-chip burst store, a GMSK modulator and two high speed DACs with output reconstruction filters. The receive path consists of two 15 bit Sigma Delta A/D converters which include high performance digital filters for RF-channel selection.

The auxiliary section of the VBC consists of D/A converters for Automatic Frequency Control (AFC), Automatic Gain Control (AGC) and control of the transmit-burst envelope (RAMP). Additionally, the VBC provides an auxiliary A/D converter which can be used to monitor four analog signals.

Various power down options as well as the low supply voltage allow the design of mobile radios having minimal power consumption.

ORDERING GUIDE

Model	Temperature Range	Package
AD6421AST	-40°C to +85°C	64-Lead TQFP

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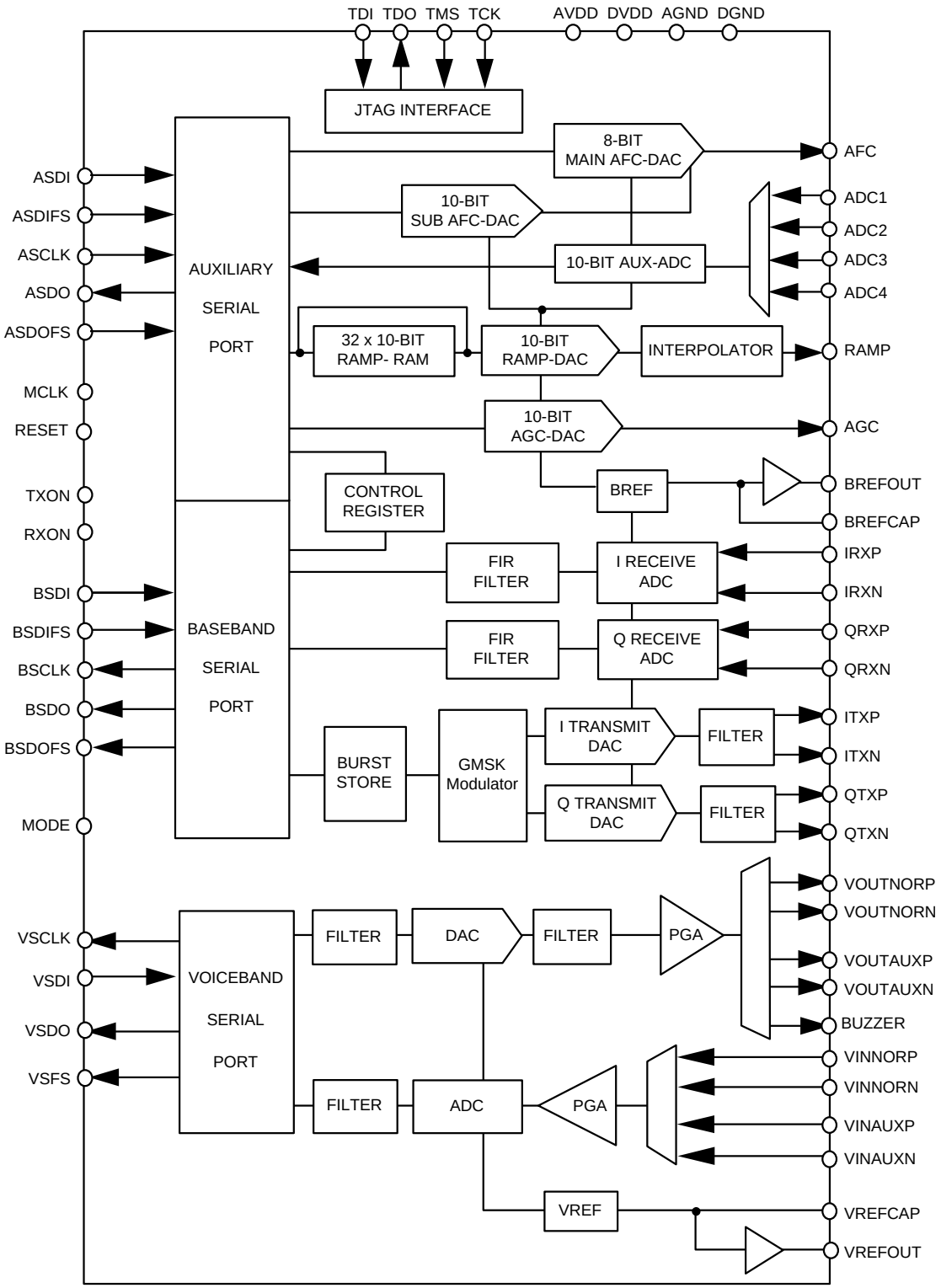

Figure 1. Detailed Block Diagram

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PIN FUNCTIONALITY

Pin Group Name	Pins	I/O	Function
Control	**5**		
MCLK	1	I	Master clock input
TXON	1	I	Baseband transmit section power-on input. When powering up/down is controlled by the bit TXON in BCRA, the pin TXON should be tied low.
RXON	1	I	Baseband receive section power-on input. When powering up/down is controlled by the bit RXON in the BCRA, the pin RXON should be tied low.
MODE	1	I	Proprietary Test Mode input. Should be tied low for normal operation
RESET	1	I	Active low reset signal input
Baseband Serial Port	**5**		
BSDI	1	I	Baseband serial port data input
BSDIFS	1	I	Baseband serial port input-data framing signal input
BSCLK	1	O	Baseband serial port clock output
BSDO	1	O	Baseband serial port data output.
BSDOFS	1	O	Baseband serial port output-data framing signal
Auxiliary Serial Port	**5**		
ASDI	1	I	Auxiliary serial port data input
ASDIFS	1	I	Auxiliary serial port input-data framing signal input (level sensitive, active low)
ASCLK	1	I	Auxiliary serial port clock input
ASDO	1	O	Auxiliary serial port data output. Tri-state when inactive.
ASDOFS	1	I	Auxiliary serial port output-data framing signal input (level sensitive, active low)
Voiceband Serial Port	**4**		
VSDI	1	I	Voiceband serial port data input
VSCLK	1	O	Voiceband serial port clock output
VSDO	1	O	Voiceband serial port data output. Tri-state when inactive.
VSFS	1	O	Voiceband serial port framing signal output
Analog Baseband Interface	**10**		
BREFCAP	1	O	Baseband reference voltage output
BREFOUT	1	I/O	Buffered baseband reference output / external bias voltage input
IRXP, IRXN	2	I	Differential analog input for in-phase receive signal
QRXP, QRXN	2	I	Differential analog input for quadrature receive signal
ITXP, ITXN	2	O	Differential analog output for in-phase receive signal
QTXP, QTXN	2	O	Differential analog output for quadrature receive signal

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Pin Group Name	Pins	I/O	Function
Analog Auxiliary Interface	**7**		
ADC1	1	I	Auxiliary A/D Converter Input 1
ADC2	1	I	Auxiliary A/D Converter Input 2
ADC3	1	I	Auxiliary A/D Converter Input 3
ADC4	1	I	Auxiliary A/D Converter Input 4
AFC	1	O	Automatic Frequency Control signal output
RAMP	1	O	Power Ramping Control signal output
AGC	1	O	Automatic Gain Control signal output
Analog Voiceband Interface	**11**		
VREFCAP	1	O	Voiceband reference voltage output
VREFOUT	1	O	Buffered voiceband reference output
VOUTNORP, VOUTNORN	2	O	Differential voiceband normal output
VOUTAUXP, VOUTAUXN	2	O	Differential voiceband auxiliary output
VINNORP, VINNORN	2	I	Differential voiceband normal input
VINAUXP, VINAUXN	2	I	Differential voiceband auxiliary input
BUZZER	1	O	Buzzer output
JTAG Interface	**4**		
TDI	1	I	Test data input
TDO	1	O	Test data output
TMS	1	I	Test mode select
TCK	1	I	Test clock
Power Supplies	**13**		
AVDD1	1		Baseband Analog Power Supply
AVDD3	1		Voiceband Analog Power Supply
AVDD4	1		Auxiliary Analog Power Supply
DVDD2, DVDD3	2		Baseband / Auxiliary Digital Power Supply
DVDD4	1		Voiceband Digital Power Supply
AGND1	1		Baseband Analog Ground
AGND2	1		Analog Substrate
AGND3	1		Voiceband Analog Ground
AGND4	1		Auxiliary Analog Ground
DGND2, DGND3	2		Baseband / Auxiliary Digital Ground
DGND4	1		Voiceband Digital Ground

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CONTROL

Control Registers

The AD6421 has a set of 37 Registers (10 bits wide each), shown in Table 1, which control the operation of the entire chip.

The functionality of all registers will be explained in the individual chapters; a brief overview is provided below.

- TXDATA is the input register for baseband transmit data.
- IRXOFFSET and QRXOFFSET hold the offset values for user calibration.
- TXDELAY1, TXDELAY2 and TXDELAY3 are programmable delays for the transmit phase.
- RXDELAY1 and RXDELAY2 are programmable delays for the receive phase.
- ARDADDR and BRDADDR are read address registers used to read the content of the control registers via the ASPORT or BSPORT.
- RAMPDAC is the input register for the RAMP-DAC.
- AGCDAC is the input register for the AGC-DAC.
- SUBDAC is the input register for the Sub AFC-DAC.
- AFCDAC is the input register for the Main AFC-DAC. Only the 8 LSBs of this register are used as input for the Main AFC-DAC.
- AUXADC1, AUXADC2, AUXADC3 and AUXADC4 are the output registers of the Auxiliary ADC's 4 channels.
- ACRA and ACRB are the two control registers for the auxiliary section.
- BCRA and BCRB are the two control registers for the baseband section.
- VCRA, VCRB and VCRC are the three control registers for the voiceband section.
- BSCLKRATE and VSCLKRATE control the clock frequency of the baseband serial port and the voiceband serial port.
- ITXOFFSET and QTXOFFSET hold the offset values for user calibration of the transmit section.
- ITXDAC and QTXDAC hold the values of the transmit DACs.

Table 1. Control Registers

Name	R/W	Address	Reset
TXDATA	R/W	00 0000 (0)	BRESET
Reserved		00 0001 (1)	
Reserved		00 0010 (2)	
IRXOFFSET	R/W	00 0011 (3)	BRESET
QRXOFFSET	R/W	00 0100 (4)	BRESET
TXDELAY1	R/W	00 0101 (5)	BRESET
TXDELAY2	R/W	00 0110 (6)	BRESET
RXDELAY1	R/W	00 0111 (7)	BRESET
RXDELAY2	R/W	00 1000 (8)	BRESET
ARDADDR	R/W	00 1001 (9)	RESET
BRDADDR	R/W	00 1010 (10)	RESET
RAMPDAC	R/W	00 1011 (11)	ARESET
AGCDAC	R/W	00 1100 (12)	ARESET
SUBDAC	R/W	00 1101 (13)	ARESET
AFCDAC	R/W	00 1110 (14)	ARESET
AUXADC1	R	00 1111 (15)	ARESET
AUXADC2	R	01 0000 (16)	ARESET
AUXADC3	R	01 0001 (17)	ARESET
ACRA	R/W	01 0010 (18)	ARESET
ACRB	R/W	01 0011 (19)	ARESET
BCRA	R/W	01 0100 (20)	BRESET
BCRB	R/W	01 0101 (21)	BRESET
VCRA	R/W	01 0110 (22)	VRESET
VCRB	R/W	01 0111 (23)	VRESET
VCRC	R/W	01 1000 (24)	VRESET
Reserved		01 1001 (25)	
BSCLKRATE	R/W	01 1010 (26)	RESET
VSCLKRATE	R/W	01 1011 (27)	RESET
ITXOFFSET	R/W	01 1100 (28)	BRESET
QTXOFFSET	R/W	01 1101 (29)	BRESET
Reserved		01 1110 (30)	
ITXDAC	R	01 1111 (31)	BRESET
QTXDAC	R	10 0000 (32)	BRESET
Reserved		10 0001 (33)	
Reserved		10 0010 (34)	
TXDELAY3	R/W	10 0011 (35)	BRESET
AUXADC4	R	10 0100 (36)	ARESET

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Writing and Reading Control Registers

Writing to and reading from control registers is possible via the auxiliary serial port or the baseband serial port (ASPORT or BSPORT). It involves the transfer of 16 bit words, 10 bits of data and 6 bits of address. The write format is shown in Figure 2, bit 15 being the first input bit of the frame. The destination of the 10 bit data is determined by the 6 bit destination address. Note that some registers are read only and hence, cannot be written to.
To read the contents of a register, the address of the appropriate register is written to the read address register, ARDADDR or BRDADDR, as shown in Figure 3. The time interval between writing to the read address register and the serial port frame synchronization signal becoming active equals 4 MCLK cycles. The frame synchronization signal can be asserted one SCLK cycle after the user has completed writing to the read address register. The read address register is 6 bits wide and bits 11 to 6 of the input frame are used to write to this register, bits 12 to 15 being don't cares. The frame format for reading is identical to that for writing i.e. 10 bits of data followed by 6 address bits corresponding to the source address of the data .

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0

Figure 2. Write / Read Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	A5	A4	A3	A2	A1	A0	0	0	1	0	0	1

Figure 3. Write to the Read Address Register (ARDADDR shown here)

Reset

To reset the AD6421, the RESET pin should be pulled low for a fraction of 1 MCLK cycle. The internal logic is edge sensitive and the low signal is latched and held low for 2 MCLK cycles after the signal goes high again. This allows time for the internal reset to be completed.
A system reset requires 8 MCLK cycles.

On reset, all control registers except BSCLKRATE are set to zero.

- BSCLKRATE is set to 4 so that the frequency is 1.625 MHz (MCLK / 8).
- The register VSCLKRATE is set to 0, leading to a frequency of 2.6 MHz (MCLK / 5) for the voiceband clock.

Additionally, the control registers can be reset by dedicated reset bits in certain registers.

- The auxiliary registers can be reset by setting bit ARESET in Auxiliary Control Register A (ACRA) to 1.
- The baseband registers can be reset by setting bit BRESET in Baseband Control Register A (BCRA) to 1.
- Finally the voiceband registers are reset by setting bit VRESET in Voiceband Control Register B (VCRB) to 1.
- The registers ARDADDR, BRDADDR, BSCLKRATE and VSCLKRATE can only be reset using the reset pin.

Timing Conventions

In a GSM mobile terminal, all timings are related to one master clock of nominal 13 MHz. The AD6421 receives its MCLK signal either directly from the master oscillator or from the AD6422. All timing in the AD6421 are derived from the MCLK period T_{MCLK}.

$$T_{MCLK} = \frac{1}{13\ \text{MHz}} \approx 76.9\ \text{ns}$$

To allow an easier interpretation of the AD6421 timing specifications, time is sometimes expressed in two system related values: T_{BIT} is the period of one transmitted signal-bit and Q_{BIT} is one quarter of T_{BIT}.

$$T_{BIT} = 48 \times T_{MCLK} \approx 3.692\ \mu\text{s}$$

$$Q_{BIT} = 12 \times T_{MCLK} \approx 0.923\ \mu\text{s}$$

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BASEBAND SECTION

Baseband Control Register

The baseband section of the AD6421 has two control registers, BCRA and BCRB as shown in Table 2 and Table 3.
BCRA contains the control bits for the activation of:

- Transmit and receive autocalibration,
- External Receive autocalibration,
- Bypass of the RAMP-RAM,
- Transmit and Receive section,
- Reset of the baseband section.

BCRB contains the control bits for the on-chip baseband reference.
All control bits reset to 0. "Reserved" bits must never be changed to 1 for proper operation.

Table 2. Baseband Control Register A (BCRA)

Bit	Name	Function
BCRA0	TXAUTOCAL	Selects Tx-Auto-Calibration when set to 1 and User-Calibration when set to 0
BCRA1	RXAUTOCAL	Selects Rx-Auto-Calibration when set to 1 and User-Calibration when set to 0
BCRA2	RXEXTCAL	When set to 1, the Rx Calibration operates in external mode. The analog inputs remain connected to the pins during the autocal routine
BCRA3		Reserved (0)
BCRA4	RBBYPASS	When this bit is set to 1 the ramping RAM is bypassed and data written to address 11 goes directly to the RAMPDAC
BCRA5	TXON	Power on for the transmit section when set to 1
BCRA6	RXON	Power on for the receive section when set to 1
BCRA7	BRESET	Baseband Reset when set to 1
BCRA8		Reserved (0)
BCRA9		Reserved (0)

Table 3. Baseband Control Register B (BCRB)

Bit	Name	Function
BCRB0		Reserved (0)
BCRB1	BRS	Baseband Reference Select. When set to 0 BREFOUT = 1.2V, when set to 1 BREFOUT = 1.35V
BCRB2	BRU	BREFOUT use; When set to 1, the output buffer for the pin BREFOUT is active;
BCRB3	BLP	Baseband Reference Low Power. When set to 1, keeps the baseband reference powered up, when baseband section is powered down.
BCRB4		Reserved (0)
BCRB5		Reserved (0)
BCRB6		Reserved (0)
BCRB7	REFOUTDIS	If set to 1 BREFOUT becomes an input
BCRB8		Reserved (0)
BCRB9		Reserved (0)

Baseband Transmit Section

The transmit section of the AD6421 generates GMSK I and Q output signals in accordance with the GSM (Phase 2) specification 05.05. This is accomplished by a digital GMSK (Gaussian Minimum Shift Keying) modulator, followed by 10-bit DACs for the I and Q channels and on-chip reconstruction filters. The GMSK modulator generates I and Q signals in response to the transmit data stream.

The entire baseband transmit section may be powered up/down by setting bit 5 in Baseband Control Register A (BCRA5) or by using the TXON-pin; see Table 4 for details.

Table 4. Activation of Transmit Section

TXON Pin	TXON (BCRA5)	Transmit Section
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

When the powering up/down of the transmit section is being controlled by the TXON-pin, the TXON-bit should equal zero.

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Burst Store

To support effective communication between the AD6421 and other components like the AD6422 GSM Processor, a burst store is included. The burst store can hold 160 data bits and is filled by making 16 writes to address 0 of the control register (TXDATA). Bit D0 of the first word written to the burst store will be the first bit to be transmitted. Bit D9 of the last word written to the burst store will be the last bit to be transmitted. When the burst store has been read, the part automatically continues to transmit ones until TXON is taken low.

GMSK Modulator

The GMSK Modulator is implemented using digital logic and ROM look up tables. The transmit data is first differentially encoded, then fed to the GMSK pulse shaping ROM. The output data of the ROM goes to cosine- (I data) and sine- (Q data) lookup tables which output 10-bit data samples to the transmit DACs. GMSK coding implements a four-bit impulse response, BT = 0.3.

Transmit Offset Calibration

Included in the transmit section is a circuit by which transmit signal offsets may be calibrated out. Each transmit channel has an offset register which contains a value representing the DC offset of the analog circuitry in the transmit channel.
In normal operation, the value stored in the register is subtracted from the GMSK modulator output data before it is fed to the DAC. Auto-calibration or user-calibration can be selected. Auto-calibration will remove internal offsets only while user-calibration allows the user to write to the offset register in order to remove external offsets. The offset registers are 10-bits wide and represent two's complement values. When auto-calibration is disabled, the offset registers will retain their contents until another auto-calibration is performed or a new value is written to the offset registers.

Auto-Calibration

If transmit auto-calibration is selected by setting bit 0 of the Baseband Control Register A (BCRA0), the AD6421 will initiate an auto-calibration routine each time the transmit path is brought out of power-down. After TXON is asserted, 340 quarter bit periods (Q_{BIT}) are allowed for the circuitry to settle and for calibration to be performed. During the calibration, the analog outputs are at V_{BIAS}. The input offset of the I and Q channel are measured and stored in the ITXOFFSET and QTXOFFSET registers.

User-Calibration

When user-calibration is selected, the transmit offset register can be written to, allowing offsets in the radio section to be calibrated out also. However, the user is now responsible for calibrating out transmit offsets belonging to the AD6421. When the transmit path enters low-power mode, the registers remain valid. TXDELAY1 must be programmed to a minimum value of 108 quarter bit periods to permit the circuitry to settle.

Output Timing

The output timing can be divided into 5 separate periods listed in Table 5 and shown in Figure 4.

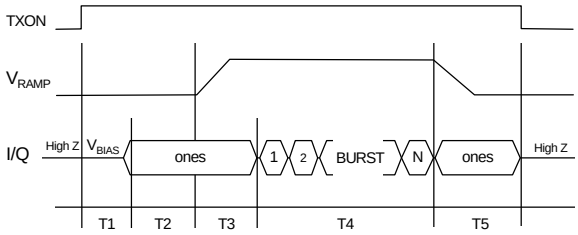

Figure 4. Transmit Timing

Upon asserting TXON, the output leaves the high impedance state and the period T1 begins. During T1, the output is held at V_{BIAS} almost to the end. Approximately 32 Q_{BIT} before the end of T1, the modulator begins to modulate consecutive ones. When autocalibration is selected, T1 is equal to 340 Q_{BIT}; when user-calibration is selected T1 is equal to 0.

When T1 is completed, an internal timer is started which times out a period T2 equal to TXDELAY1. During this interval, the modulator continues to modulate consecutive ones. When user-calibration is selected, TXDELAY1 must be programmed to a minimum value of 108 Q_{BIT} to allow analog circuitry to settle. After T2, the power ramp starts by feeding the RAMP-DAC with the values from the RAMP RAM. The time when the modulator begins to modulate the bits in the burst store can be further delayed by the period T3 equal to TXDELAY3. If TXDELAY3 has a value of 0, the power ramping and the modulation of the burst bits commences simultaneously.

Table 5. Transmit Timing

	Name	Q_{BIT}	µs
T1	$T_{AUTOCALIBRATE}$ $T_{USERCALIBRATE}$	340 0	313.8 0.0
T2	$TXDELAY1_{AUTOCAL}$ $TXDELAY1_{USERCAL}$	0 - 1023 108 - 1023	0 - 944.2 99.7 - 944.2
T3	TXDELAY3	0 - 1023	0 - 944.2
T4	TXDELAY2	0 - 1023	0 - 944.2
T5	depends on TXON	0 - ∞	0 - ∞

After T3 has expired, the burst bits are modulated for the period T4 equal to TXDELAY2. To ensure proper timing operation of the ramp up sequence during data transmission, the sum of registers TXDELAY3 and TXDELAY2 must be restricted to an even number of Q_{BIT}s.
After T4, the modulator begins to modulate consecutive ones again. This continues until TXON is deasserted and the analog outputs assume the high impedance state. TXON should not be deasserted until the end of the ramp down sequence.

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Transmit DACs & Output Filters

The AD6421 contains two 10-bit DACs which have been optimized for matched gain, group delay and phase between the two channels. Analog reconstruction filters smooth the DAC output signals providing continuous time I and Q waveforms at the output pins. These are Butterworth low-pass filters with a cut-off frequency of approximately 300 kHz. The filters are designed to have a linear phase response in the passband and the phase mismatch between the I and Q transmit channels is kept to a minimum.

Output Bias Voltage

The common mode voltage of the analog outputs is normally equal to $V_{BREFOUT}$. The value of this voltage can be programmed by setting bit 1 of the BCRB. Two values are selectable: 1.2V or 1.35V.
Alternatively, an external reference can be used to alter the bias voltage, Vbias. This is done by setting bit REFOUTDIS in register BCRB (see Table 3) to disable the baseband reference output pin, BREFOUT. After disabling BREFOUT, it becomes an input pin to which an external reference may be connected. The input range for this pin is nominal 1.2V to AVDD - 1.35 V. The bias voltage then becomes equal to the value of the external reference. The analog signal range, however, continues to be determined by $V_{BREFCAP}$; i.e. the external reference only affects the bias voltage to the Tx analog outputs. The input resistance to this pin is in the range of 10 kΩ to 20 kΩ.

Output Interface

The ITX and QTX outputs are designed to be dc or ac coupled to the external circuits. Figure 5 shows a simplified circuit providing a differential output with ac coupling. The capacitor (C_{OUT}) of this circuit is optional. An external lowpass filter may be required to meet GSM Phase 2 requirements. See section APPLICATION NOTES at the end of the datasheet.

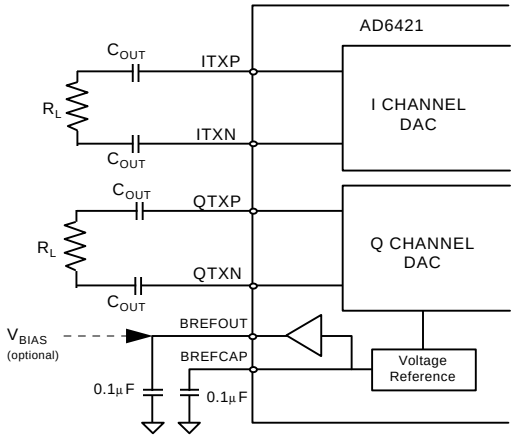

Figure 5. Circuit for Differential Output

Baseband Receive Section

The receive section consists of I and Q receive channels, each comprised of a switched-capacitor filter followed by a 15-bit sigma-delta ADC. On-chip digital filters, which are part of the sigma-delta ADCs, also perform substantial neighbor channel selection. The receive section also has a low power sleep mode drawing only minimal current.

The entire baseband receive section may be activated or powered down by setting the bit 6 in the Baseband Control Register A (BCRA6) or by using the RXON-pin; see Table 6 for details.

Table 6. Activation of Receive Section

RXON Pin	RXON (BCRA6)	Receive Section
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

When the powering up/down of the receive section is being controlled by the RXON-pin, the RXON-bit should equal zero. Similarly, when the powering up/down is controlled by the RXON-bit, the RXON-pin should be tied low.

Analog Input & Switched Capacitor Filter

The AD6421 provides differential analog inputs for the I and Q receive signals. Figure 6 shows the recommended circuit.

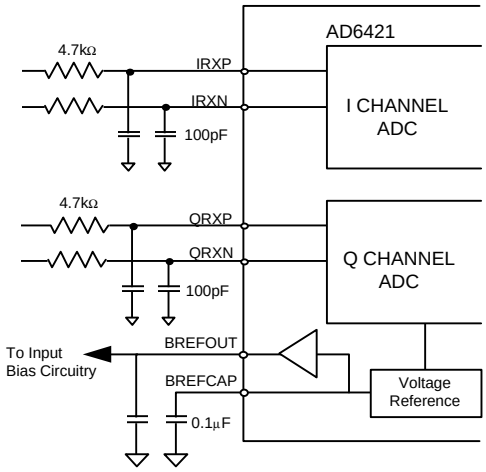

Figure 6. Circuit for Differential Input

The AD6421 provides a high degree of flexibility to adapt to different input and bias voltages as shown in Table 7.
The analog inputs are sampled at 13 MHz by a switched capacitor filter. The filter has a zero at 6.5 MHz as shown in Figure 8a. The receive channel also contains a digital low-pass filter which operates at a clock frequency of 6.5 MHz. Due to the sampling nature of the digital filter, the passband is repeated

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about the operating clock frequency and at multiples of the clock frequency (Figure 8b). Because the first null of the switched-capacitor filter coincides with the first image of the digital filter, this image is attenuated by an additional 30 dB (Figure 8c), further simplifying the external anti-aliasing requirements. The circuitry of Figure 6 implements first-order low-pass filters with a 3 dB point at 338 kHz. These are the only filters that must be implemented externally to prevent aliasing of the sampled signal.

Table 7. Input Signal Ranges

Parameter	Range
AVDD	3.0V ± 10%
$V_{BREFCAP}$	1.2V ± 5%
ADC overall Signal Range	2 $V_{BREFCAP}$
VBIAS Differential Input	$V_{BREFCAP}/2$ to AVDD - $V_{BREFCAP}/2$
Input Signal Range Differential	$V_{BIAS} \pm V_{BREFCAP}/2$

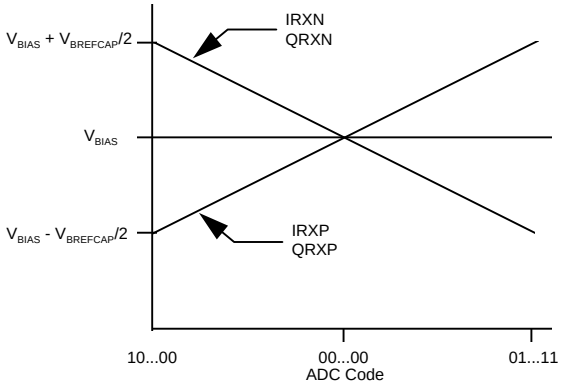

Figure 7. ADC Transfer Function Differential Input

Sigma-Delta ADC

The AD6421 receive channels employ a sigma-delta conversion technique, which provides a high resolution 15-bit output for both I and Q channels with system filtering being implemented on-chip.

The output of the switched-capacitor filter is continuously sampled at 6.5 MHz, by a charge-balanced modulator, and is converted into a digital pulse train. Due to the high oversampling rate, which spreads the quantization noise from 0 to 3.25 MHz, the noise energy contained in the band of interest is reduced. To reduce the quantization noise still further, a high-order modulator is employed to shape the noise spectrum so that most of the noise energy is shifted out of the band of interest. The digital filter that follows the modulator removes the large out of band quantization noise, while converting the digital pulse train into parallel 15-bit wide binary data.

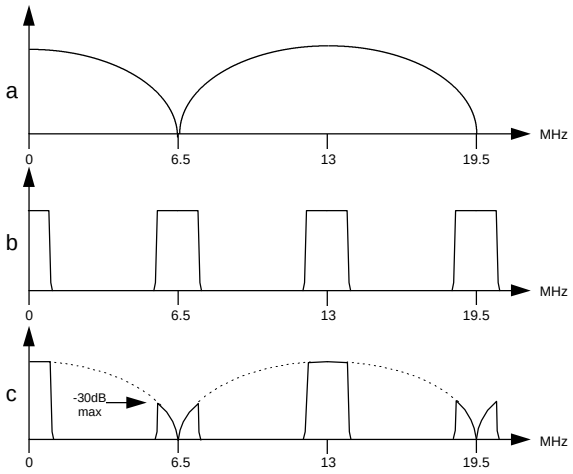

Figure 8. Receive Channel Frequency Response
a) Switched Capacitor Filter
b) Digital FIR Filter
c) Combined

Digital Filter

The digital filters used in the AD6421 receive section carry out two important functions. Firstly, they remove the out-of-band quantization noise. Secondly, they ease the design of the radio section by providing substantial neighbor-channel suppression. The digital filter is a 288-tap FIR filter with a 3dB point at 96 kHz. The filter is clocked at 6.5 MHz and has a settling time of 44.3 µs.

Even though digital filters have several advantages over analog filters, they cannot remove noise superimposed on the analog signal before it reaches the ADC.

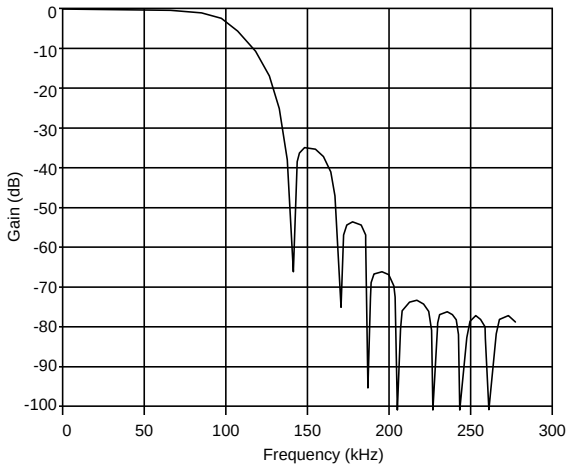

Figure 9. Digital Filter Frequency Response

Therefore, noise peaks riding on signals near full-scale have the potential to saturate the analog modulator, even though the

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average value of the signal is within limits. To alleviate this problem, the AD6421 has overrange headroom built into the sigma-delta modulator and digital filter which allows overrange excursions of 100 mV.

Receive Offset Calibration

Each channel of the digital low pass filter has an offset register. In normal operation, the value stored in the offset register is subtracted from the filter output data before the data appears on the serial output. By so doing, dc offsets in the I and Q channels get calibrated out. Auto-calibration or user-calibration can be selected. Auto-calibration will remove internal offsets only while user-calibration allows the user to write to the offset register in order to remove external offsets also.

The 10-bit offset registers can hold any dc offset between ±150 mV (1/8th of the input range) however the performance of the Sigma Delta ADCs will degrade if full-scale signals with more than 75mV of offset are experienced. The values in the offset registers are coded in two's complement. The LSB of the offset register corresponds to bit 3 of the Rx words, while the MSB of the offset register corresponds to bit 12 of the Rx words (see Table 8).

Table 8. Position of 10-bit Offset Word

Rx Data	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Register				9	8	7	6	5	4	3	2	1	0			

Auto-calibration is selected by setting bit 1 of the Baseband Control register A (BCRA1 = RXAUTOCAL) to 1.
If RXAUTOCAL is set to 0, no calibration occurs (see Figure 10). Two types of Auto-calibration can be selected by setting bit 2 of the Baseband Control Register A (BCRA2 = RXEXTCAL).

Autocalibration

If auto-calibration is selected by setting the RXAUTOCAL bit in control register BCRA to 1, the AD6421 will perform an auto-calibration routine each time the receive section is brought out of the low-power mode. Two modes of autocalibration can be selected. In internal autocalibration mode, the differential inputs are disconnected from the input pins and shorted together to measure the ADC offset. In external autocalibration mode, the inputs remain connected to the pins, allowing system offset along with the internal offsets to be evaluated. This is averaged sixteen times to reduce noise and the result is placed in the offset register. The input to the ADC is then switched back for normal operation and the circuitry is permitted to settle.

User Calibration

When user calibration is selected by setting RXAUTOCAL to 0, the receive offset register can be written to, allowing offsets in the IF-demodulation circuitry to be calibrated out also. However, the user is now responsible for calibrating out receive offsets belonging to the AD6421. When the receive path enters the low power mode, the registers remain valid. After powering up, the first I/Q sample pair is output once time has elapsed for circuitry to settle and also for the output of the digital filter to settle.

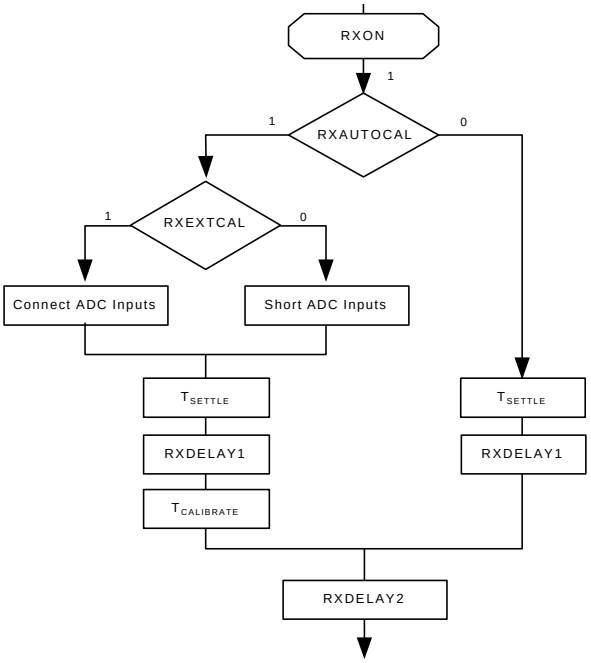

Figure 10. Receive Offset Calibration Flowchart

Receive and Offset Calibration Timing

The timing of the receive and offset calibration process can be divided into 4 periods T0 - T3 as shown in Figure 11 and Table 9. RXDELAY1 and RXDELAY2 reset to zero and can be user programmed for periods from 0 to 255 T_{BIT}.

Table 9. Receive Offset Calibration Timing

Period	Name	T_{BIT}	µs
T0	T_{SETTLE}	36	132.9
T1	RXDELAY1	15 - 255	55.38 - 941.5
T2	$T_{CALIBRATE}$	40	147.7
T3	RXDELAY2	0 - 255	0 - 941.5

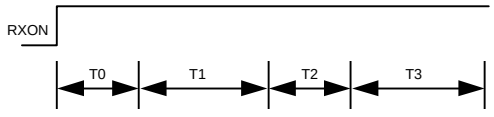

Figure 11. Receive Offset Calibration Timing

After RXON is asserted, the RXAUTOCAL bit determines the path in the flow diagram shown in Figure 10.

If user-calibration is selected, the fixed period T0 (36 T_{BIT} periods) transpires. After T0 has expired, the period T1 starts which

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is a programmable period RXDELAY1. To allow time for the analog and digital circuitry to settle, RXDELAY1 must be programmed to a minimum value of 15 T_{BIT} , value 0x00F. After T1 has expired, a second programmable period, T3 equal to RXDELAY2, is inserted. After T3 has expired, the first valid output word appears at the output.
If autocalibration is selected, the RXEXTCAL bit determines whether external or internal autocalibration is selected.
Again, the calibration process starts with the period T0 followed by T1 programmed to a minimum 15 T_{BIT} delay. After T1 has expired, the autocalibration period T2 equal to 40 T_{BIT} begins. After T2, the programmable delay T3 is inserted before the first valid word appears at the output.

Output Timing

After the receive section is activated by the RXON bit or RXON pin and the calibration procedure has been performed, Rx data is automatically output on the BSDO pin.

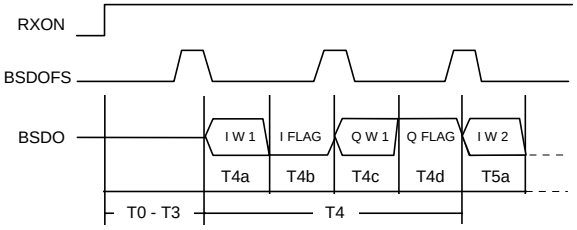

Figure 12. Output Format of Rx Data

The data format is I followed by Q. The AD6421 will output 16 bits of data, the 15-bit I or Q word, which is in two's complement format, and a flag bit. This flag bit (LSB) distinguishes between I and Q words, the bit being 0 for an I word and 1 for a Q word.

Table 10. Output Timing of Rx Data

Period	Function	T_{BIT}	µs	Transf. Bits (13Mbit/s)
T0 - T3	see Table 9			none
T4a	I Word	1/3	1.231	16 (15+1)
T4b	I Flag	1/6	0.615	8
T4c	Q Word	1/3	1.231	16 (15+1)
T4d	Q Flag	1/6	0.615	8
T4		1	3.692	48
T5a	I Word	1/3	1.231	16

The serial clock has a frequency of 13 MHz, irrespective of the value of the clock rate register. When the AD6421 is ready to output Rx data, it generates an output frame synchronization signal (BSDOFS) and the Rx data is outputted automatically on the BSDO pin; see Figure 12 and Table 10 for details. To adapt the data rates of the ADC samples (2 × 270 k words/sec) to the data rate of the serial port (13 Mbit/s) the flag bits are extended by 8 bit-periods (13 Mbit/s).

BASEBAND REFERENCE

The baseband reference of the AD6421 is a bandgap reference, which provides a low noise, temperature compensated reference for the converters in the baseband as well as in the auxiliary section. The reference voltage has a nominal value of 1.2V and is referred to as $V_{BREFCAP}$ in the description of the baseband and auxiliary section. This internal reference is connected to the pin BREFCAP, where a bypass capacitor of 0.1µF should be connected.

Additionally, the AD6421 provides a buffered copy of the internal baseband reference, which is connected to pin BREFOUT. Also here, a bypass capacitor of 0.1µF should be connected. The output voltage of this pin is referred to as $V_{BREFOUT}$ and can be used as a bias voltage for other analog circuitry in the radio section. The output buffer which drives the BREFOUT pin can be disabled by setting bit BRU in the control register BCRB to 0.
In order to provide more flexibility, the voltage $V_{BREFOUT}$ is selectable between two values depending on bit 1 of control register BCRB (BCRB1). If BCRB1 is equal to 0, $V_{BREFOUT}$ is 1.2V; if BCRB1 is equal to 1, $V_{BREFOUT}$ is 1.35V.

The baseband reference output pin (BREFOUT) can be disabled by setting the bit REFOUTDIS in BCRB to 1. After disabling BREFOUT, it becomes an input pin and an external reference can be connected to this pin. The input resistance is in the range of 10 kΩ to 20 kΩ. Note however, that the external reference changes only the value of $V_{BREFOUT}$ and not the value of $V_{BREFCAP}$. I.e. all expressions relating to $V_{BREFCAP}$ remain unchanged.

When all baseband and auxiliary converters in the AD6421 are powered down, the reference will automatically power down also. Once any one of the baseband or auxiliary converters is powered up, the baseband reference will also power up automatically. Alternatively, by setting bit 3 of control register BCRB (BLP) to 1, the reference always remains powered up. This is useful when external circuitry requires a continuously active reference. Also, the power up time for the converters is reduced since the reference does not require time to power up and settle.

The baseband reference can further be placed in a low power standby mode by setting bit 1 (BREFSB) of control register ACRB to 1. In this mode, only the AFC-DAC may drive an output.

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AUXILIARY SECTION

The AD6421 contains three auxiliary DACs which may be used to generate analog control signals for Automatic Gain Control (AGC) of the IF receive section, for Automatic Frequency Control (AFC) of the master clock oscillator, and for RF power amplifier control (RAMP). Additionally, it contains a universal ADC with four multiplexed input channels for monitoring analog values in the mobile radio.

Auxiliary Control Register

The auxiliary section of the AD6421 has two control registers as shown in Table 11 and Table 12.
ACRA contains the control bits to power on the auxiliary ADC and all three auxiliary DACs, as well as the start convert signal for the auxiliary ADC and its channel selection.
ACRB contains the reset control bit for all auxiliary converters. All control bits reset to 0. The "Reserved" bits must never be changed to 1 for proper operation.

RAMP Control

To avoid the emission of unwanted spectral components during the transmission of a burst, the envelope of the burst must follow a precisely defined curve with particular care placed on the up and down ramps. In addition, GSM allows the reduction of the RF output power depending on the quality of the air interface. Both functions are supported by the RAMP-DAC with a 4X interpolator and an associated RAMP-RAM.

Table 11. Auxiliary Control Register (ACRA)

Bit	Name	Function
ACRA0	AUXADCON	Power on for Auxiliary ADC when set to 1
ACRA1	RAMPDACON	Power on for RAMPDAC when set to 1
ACRA2	AGCDACON	Power on for AGCDAC when set to 1
ACRA3	AFCDACON	Power on for AFCDAC when set to 1
ACRA4		Reserved (0)
ACRA5		Reserved (0)
ACRA6	AFCDACLP	AFC-DAC Low Power when set to 1
ACRA7	AUXADCCS	Auxiliary ADC start convert. Writing a 1 to this bit starts conversion.
ACRA8	AUXADCCS0	Auxiliary ADC channel select bit 0
ACRA9	AUXADCCS1	Auxiliary ADC channel select bit 1

Table 12. Auxiliary Control Register B (ACRB)

Bit	Name	Function
ACRB0	ARESET	Resets all Auxiliary Converters when set to 1
ACRB1	BREFSB	BREFCAP Standby. When set to 1, the baseband reference is in low power standby mode.
ACRB2	AFCUPD	AFC-DAC update When set to 1, the Main- and Sub-DAC are updated simultaneously after a SUBDAC write
ACRB3		Reserved (0)
ACRB4		Reserved (0)
ACRB5		Reserved (0)
ACRB6		Reserved (0)
ACRB7		Reserved (0)
ACRB8		Reserved (0)
ACRB9		Reserved (0)

RAMP-RAM

The AD6421 has a 32 × 10 bit wide RAM, which holds the ramping coefficients - 16 words are used for ramp-up and 16 for ramp-down.
Writing to the RAMP-RAM is performed by making 32 consecutive writes to address 11 of the control register. The first 16 words must define the ramp up envelope and the second 16 must define the ramp down envelope. At a 540 kHz update rate, this corresponds to 8 T_{BIT} of ramp up and 8 T_{BIT} of ramp down. It is possible to write to the RAMP-RAM at any time other than T3, T4 and T5. The contents of the RAMP-RAM will be retained under all circumstances - even during RESET.
The RAMP-RAM can be bypassed by setting bit 4 in the control register BCRA to 1. In this case, data written to address 11 of the AD6421 control register goes directly to the RAMP-DAC for conversion.

RAMP-DAC and Interpolator

The 10-bit RAMP-DAC fetches new values from the RAMP-RAM with a rate of 540 kHz. To reduce the high frequency components of the analog output signal, the output of the RAMP-DAC is interpolated between each update increasing the effective output rate to 4 x 540 kHz = 2.16 MHz. I.e. every N+4th output sample is determined by the RAMP-RAM, while the three output samples in between (N+1, N+2 and N+3) are interpolated between the Nth and N+4th value. The frequency response of the interpolated output can be seen in Figure 13. For smoothing, a single-pole RC filter with a corner frequency of 300 kHz should be placed at the DAC output - recommended values 10K/50pF.

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The output voltage of the RAMP-DAC for a 10-bit word (W) can be calculated by the formula:

$$V_{OUT} = 2 \times V_{BREFCAP} \times (1/32 + W/1024)$$

For W = 0x000 this gives an output voltage of $2/32 \times V_{BREFCAP}$; for W = 0x3FF this gives an output voltage of approximately $(2+2/32) \times V_{BREFCAP}$ (75 mV to 2.473V).

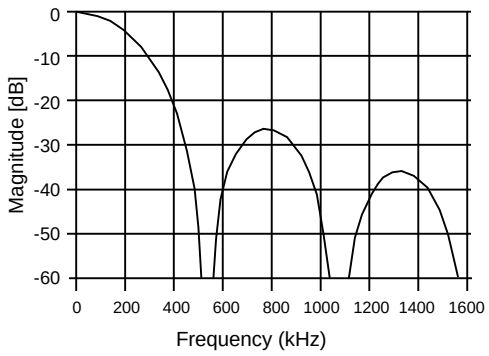

Figure 13. Interpolator Frequency Response

RAMP Timing

The timing of the RAMP-DAC output can be seen in relation to the timing of the baseband DAC output described in Table 5 and Figure 4. Note however, that the period T3 (TXDELAY3) in Table 13 and Figure 14 is set equal to Ramp Up, or 32 Q_{BIT}.

Table 13. RAMP Timing

	Name	Q_{BIT}	µs
T1	$T_{AUTOCALIBRATE}$	340	313.8
T2	TXDELAY1	0 - 1023	0 - 944.2
T3	Ramp Up	32	29.5
T4	TXDELAY2	0 - 1023	0 - 944.2
T5	Ramp Down	32	29.5
T6	depends on TXON	0 - ∞	0 - ∞

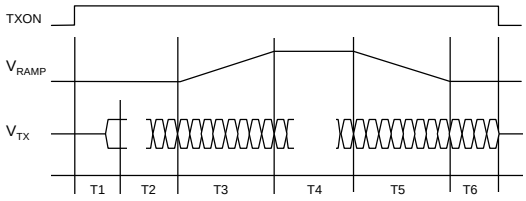

Figure 14. Ramp Timing

The whole ramp process is described in Figure 14 and Table 13. During the periods T1 and T2, the RAMP-DAC can be brought out of power down mode by setting bit 1 in the control register ACRA. After power up, 10 µs are required for the RAMP-DAC to settle. Once T2 has expired, the ramping process starts with the RAMP-RAM sequentially updating the RAMP-DAC. The period T3 is equal to 8 T_{BIT} , or 16 updates at the 540 kHz update rate. During the period T4, the RAMP-DAC holds the output constant, equal to the 16th value of the RAMP-RAM. When T4 has expired, the ramping down begins by sending the second 16 values, starting with word 17, from the RAMP-RAM to the RAMP-DAC. This period T5 is equal to the period T3. After ramping down is completed, the RAMP-DAC may be powered down again.
In power down, the RAMP-DAC register will retain its last contents. When the RAMP-DAC is reset, the RAMP-DAC register contains all zeros.

AGC Control

The 10-bit AGC-DAC can be used to generate an analog output signal which controls the gain of an IF amplifier in the radio section. The AGC-DAC is powered on by setting bit 2 in the control register ACRA to 1. After power up, 10 µs are required for the AGC-DAC to settle. The AGC-DAC is loaded by writing to control register 12.
The output voltage of the AGC-DAC for a 10-bit word (W) can be calculated by the formula:

$$V_{OUT} = 2 \times V_{BREFCAP} \times (1/32 + W/1024)$$

For W = 0x000, this output voltage equals $2/32 \times V_{BREFCAP}$; for W = 0x3FF, this gives an output voltage of approximately $(2+2/32) \times V_{BREFCAP}$ (75 mV to 2.473V).

In power down, the AGC-DAC register will retain its last contents. When the AGC-DAC is reset, the AGC-DAC register will contain all zeros.
To reduce high frequency components, a 100 kHz lowpass filter at the DAC output is recommended. A single-pole RC filter with values of 10KΩ/160pF is sufficient.

AFC Control

A combination of two DACs, forming the AFC-DAC, allow coarse and fine adjustment of the master clock frequency of the mobile radio. The Main-DAC is 8 bits wide while the Sub-DAC is 10 bits wide with bit 5 of the Sub-DAC having the same weighting as the LSB of the Main AFC DAC. Both DACs together form a common DAC with 13 bits of resolution.

Main-DAC	7	6	5	4	3	2	1	0			
Sub-DAC				9	8	7	6	5	4	3	2	1	0

To conserve power, the AFC-DAC has been designed to generate stable output signals even when the clock input signal is removed. This feature is enabled by setting bit ACRA6 (AFCDACLP). An update of the AFC-DAC output, however, is only possible with active clock input signal. To perform a conversion, the AFC-DAC is firstly powered up by setting bit 3 in the control register ACRA to 1. After power up, 50 µs is required for the circuitry to settle. The AFC-DAC is loaded by writing to control registers 13 and 14 (SUBDAC and

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AFCDAC). The 8-bit value for the Main-DAC is located in the 8 LSBs of the AFCDAC register.

The Main-DAC and Sub-DAC can be updated simultaneously when bit 2 in the control register ACRB is set to 1. When ACRB2 is set, both DACs are updated simultaneously when SUBDAC is written to. When ACRB2 equals 0, conversion begins once either of the two DACs has been written to. In power down, the AFC-DAC registers will retain its last content. Upon system or auxiliary reset, the AFC-DAC registers will contain all zeros.

The output voltage of the AFC-DAC for a 8-bit Main-DAC word (M) and a 10 bit Sub-DAC word (S) can be calculated by the formula:

$$V = 2 \times V_{BREFCAP} \times (1/32 + M/256 + 1/8 \times S/1024)$$

For M = 0x00 and S = 0x000, this gives an output voltage of $2/32 \times V_{BREFCAP}$ = 75 mV.

For M = 0xFF and S = 0x3FF, this gives an output voltage of $(2/32 + 2 + 2/8) \times V_{BREFCAP}$ = 2.765V.

This theoretical output voltage exceeds the minimum supply voltage of 2.7V. The maximum output voltage for the specified linearity is guaranteed only up to a maximum code of M = 0xDF and S = 0x3FF, which gives an output of 2.46V.

To stabilize the control loop, a low-pass filter at the AFC-DAC output is recommended. A simple RC filter as shown in Figure 15 is sufficient.

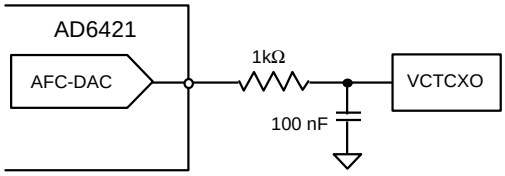

Figure 15. AFC-DAC Output Filter

In a typical mobile radio application, the AFCDAC must be active most of the time while the other converters can be set into power down for certain periods. To support lowest possible power consumption for AFCDAC operation, the AD6421 provides a low power standby mode for the baseband reference. The reference is placed in the standby mode by setting bit 1 in control register ACRB (BREFSB) but only while the AFCDAC is activated and programmed. However, at full-scale code, deviations from AFCDAC active to low power standby mode (BREFSB + AFCDACLP) will typically vary by a mean of –1 mV with standard deviation, 1.6 mV.

Auxiliary ADC

In a typical mobile radio, some analog values must be monitored - battery voltage or temperature for example. The AD6421 includes a general purpose 10-bit auxiliary ADC with four multiplexed input channels. Selection of the input channel is done by writing to the bits 8 and 9 of the Auxiliary Control Register A according to Table 14.

Table 14. AUXADC Channel Selection

AUXADC CS0	AUXADC CS1	Channel Selected
0	0	ADC1
0	1	ADC2
1	0	ADC3
1	1	ADC4

On power up, the AUXADC is reset using bit 0 of the Auxiliary Control Register B (ACRB0 = ARESET). See Table 12 or the RESET pin of the AD6421. The AUXADC requires 10 µs to settle. To start a conversion, bit 7 of the Auxiliary Control Register A (ACRA7 = AUXADCSC) must be set to 1 (see Table 11). A conversion requires 128 MCLK cycles. This is the time until the AUXADC resets ACRA7 to 0. The user can then start another conversion by writing again to ACRA7. If this bit is set to 0 by the user during a conversion, the conversion will be abandoned. The conversion result can be read via the auxiliary or baseband serial port.

Auxiliary Serial Port

The direction of the ASPORT signals are shown in Table 15. ASCLK has a maximum frequency of 6.5 MHz and can be asynchronous to MCLK.

Table 15. Directions of ASPORT Signals

Signal	Function
ASCLK	Input
ASDI	Input
ASDIFS	Input
ASDO	Output
ASDOFS	Input

The ASPORT framing signal inputs (ASDIFS and ASDOFS) are level sensitive and active low.
While ASDIFS is low, data is clocked into the ASPORT. After N × 16 ASCLK cycles, the content of the input register is placed upon the internal data bus. If ASDIFS remains low after 16 ASCLK cycles, invalid data will be clocked into the input register which will be placed on the data bus after the next 16 ASCLK cycles. Therefore, ASDIFS should return high after 16 ASCLK cycles and before 32 ASCLK cycles.
Reading a control register, by writing via the ASPORT to the Read Address Register (ARDADDR) and then taking ASDOFS low, will generate data at the output pin ASDO as long as ASDOFS remains low and the ASCLK pin receives clock pulses. The data bits at the output appear continuously in the same order (D9, D8, ... D0, A5, ... A0, D9, D8, ...). The ASDO pin will be driven until ASDOFS is taken high again; then ASDO will be tri-stated.

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VOICEBAND SECTION

Voiceband Control Registers

The voiceband control registers configure the voiceband codec for various modes of operation including input and output gain settings, multiplexer selection, and power down.

Table 16. Voiceband Control Register A (VCRA)

VCRA	Name	Function
VCRA0	OD	Disables all outputs when set to 1
VCRA1	OG0	Output gain select bit 0
VCRA2	OG1	Output gain select bit 1
VCRA3	OG2	Output gain select bit 2
VCRA4	PUV	Power up voiceband section VSPORT Enable (1 = power up, port enable 0 = power down, port disable)
VCRA5		Reserved (0)
VCRA6	OS0	Output Select Bit 0
VCRA7	OS1	Output Select Bit 1
VCRA8	VDACMUTE	Mutes outputs when set to 1
VCRA9	IMS	Input multiplexer select: IMS = 0 : Normal input, IMS = 1 : Auxiliary input

Table 17. Voiceband Control Register B (VCRB)

VCRB	Name	Function
VCRB0		Reserved (0)
VCRB1	IGS0	Input Gain Select Bit 0
VCRB2	VCLKDIS	Disables voiceband master clock if set to 1
VCRB3	VRESET	Voiceband Section reset. Reset when set to 1
VCRB4	VRU	VREFOUT use. When set to 1 the output buffer for the pin VREFOUT is active.
VCRB5	VLP	when set to 1, keeps the voiceband reference VREF powered up, when the voiceband section is powered down.
VCRB6	VR2VEN	Enables VREFOUT = 2.2V
VCRB7	IGS1	Input Gain Select Bit 1
VCRB8	IGS2	Input Gain Select Bit 2
VCRB9	IGS3	Input Gain Select Bit 3

Table 18. Voiceband Control Register C (VCRC)

Bit	Name	Function
VCRC0		Reserved (0)
VCRC1	DAIMODE	When set to 1, the VSPORT operates in 13-bit DAI Mode.
VCRC2	VSDOFF	When set to 1, VSDO is tri-stated
VCRC3 to VCRC9		Reserved (0)

VCRA contains control bits for selection of the input and output channel, the output gain, and powerdown of the voiceband section. VCRB contains control bits for selection of the input gain and the on-chip voiceband reference and a control bit to switch off the master clock of the whole voiceband section. VCRC contains a control bit for VSPORT 13-bit DAI Mode (DAIMODE) and a bit to tri-state VSDO (VSDOFF). All control bits reset to 0. The “Reserved” bits must not be set to 1 for proper operation.
The voiceband control registers can be written to via the ASPORT or via the BSPORT.

Voiceband Reference

The voiceband reference of the AD6421 is a bandgap reference, which provides a low noise, temperature compensated reference for the converters in the voiceband section. The reference voltage has a nominal value of 1.2V and is referred to as $V_{VREFCAP}$ in the description of the voiceband section. This internal reference is connected to the pin VREFCAP, where a bypass capacitor of 0.1µF should be connected.

Additionally the AD6421 provides a buffered copy of the internal voiceband reference, which is connected to the pin VREFOUT. The output voltage of this pin is referred to as $V_{VREFOUT}$ and can be used as a bias voltage for other analog circuitry in the audio section. The value of VREFOUT can be programmed by VR2VEN (VCRB6) according to Table 19. This feature provides a minimum 2V supply option to provide power for active microphones.

Table 19. Programming VREFOUT

VR2VEN	VREFOUT
0	1.2 V
1	2.2 V

The output buffer which drives the VREFOUT pin can be disabled by setting the bit VRU in the control register VCRB to 0.
When the voiceband section of the AD6421 is powered down, the reference will also automatically power down. Once the voiceband section is powered up, the voiceband reference will also power up automatically. Alternatively, by setting bit 5 of

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control register VCRB (VLP) to 1, the reference always remains powered up. This is useful when external circuitry requires a constant active reference. Also, the power up time for the converters is reduced since the reference does not require time to settle.

ADC Section

The A/D conversion circuitry consists of an input multiplexer, a programmable gain amplifier and a sigma-delta A/D converter with integral digital filters.

Analog Inputs

The VB analog inputs may be either AC or DC coupled in either the single-ended or differential configuration. In order to utilize the high provided gain of up to +39 dB, AC coupling is recommended. Figure 16 illustrates two approaches for biasing an AC coupled circuit for differential inputs. The normal channel receives its DC bias from the microphone circuit through VINNORN (either input may be used). The auxiliary channel receives its DC bias (to either side) via VREFOUT. Figure 17 shows the interface for single-ended inputs. An application example of a microphone interface is shown in Figure 37.

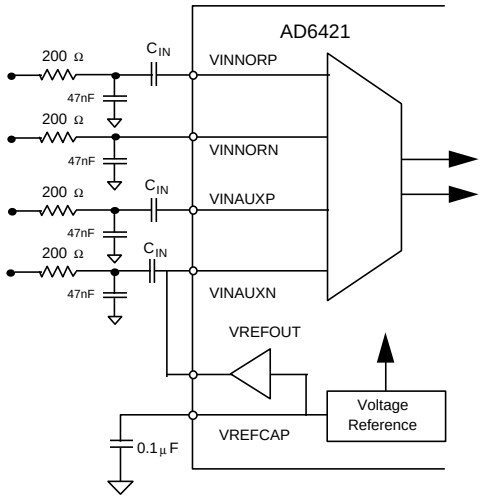

Figure 16. Differential Input

An analog multiplexer selects either the normal or the auxiliary channel as the input to the sigma-delta modulator. The input channel of the multiplexer can be selected by setting bit 9 of the Voiceband Control Register A (VCRA9 = IMS). If the multiplexer setting is changed while an input signal is being processed, the encoder's output must be allowed time to settle to ensure that the output data is valid.

The gain of the input PGA can be selected by programming bits 1, 7, 8 and 9 of register VCRB according to Table 20.

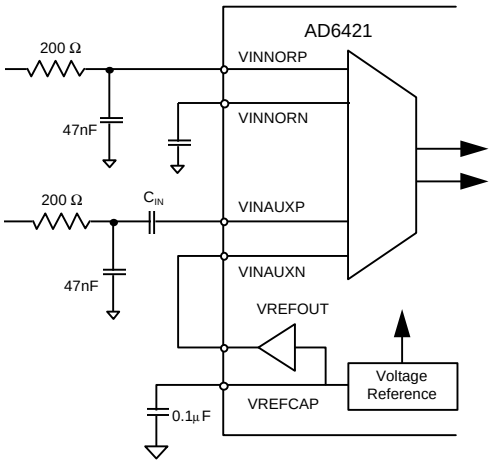

Figure 17. Single-Ended Input

Table 20. Input PGA Gain Settings

IGS3	IGS2	IGS1	IGS0	Gain
0	0	0	0	+0 dB
0	0	0	1	+3 dB
0	0	1	0	+6 dB
0	0	1	1	+9 dB
0	1	0	0	+12 dB
0	1	0	1	+15 dB
0	1	1	0	+18 dB
0	1	1	1	+21 dB
1	0	0	0	+24 dB
1	0	0	1	+27 dB
1	0	1	0	+30 dB
1	0	1	1	+33 dB
1	1	0	0	+36 dB
1	1	0	1	+39 dB
1	1	1	0	Reserved
1	1	1	1	Reserved

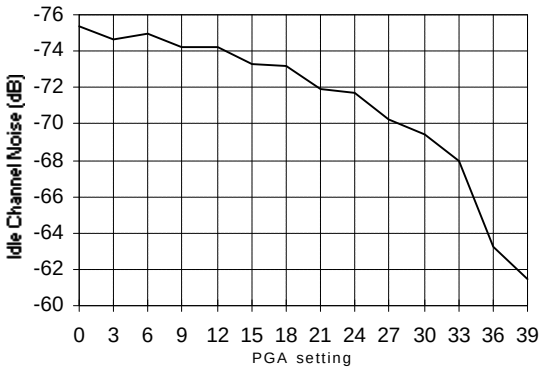

Figure 18. Encoder ICN versus Gain (Typical Values)

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ADC

The ADC consists of an analog sigma-delta modulator, a decimation filter and a combined high-pass/low-pass filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a 500 kHz rate. This bitstream is fed to the decimation filter and then to the high-pass/low-pass filter.

Filter

The same filter is used in the ADC and the DAC of the voiceband section. It is a combination of a 4-th order elliptic IIR high-pass and a 8th-order elliptic IIR low-pass filter. Its combined characteristic is shown in Figure 19.

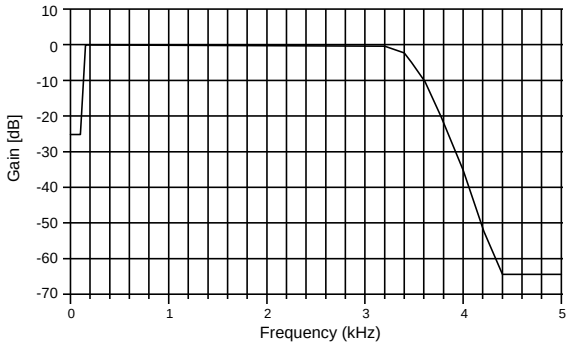

Figure 19. Digital Voiceband Filter

A detailed description of the digital highpass filter is given in Table 21 and Figure 20.

Table 21. Digital Highpass Filter Specifications

Filter Type	4-th order elliptic IIR
Passband cutoff	150.0 Hz
Passband ripple	± 0.2 dB
Stopband cutoff	100.0 Hz
Stopband ripple	-25 dB

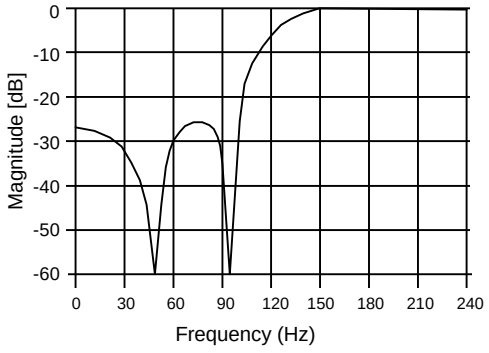

Figure 20. Digital Highpass Filter

A detailed description of the digital lowpass filter is given in Table 22 and Figure 21.

Table 22. Digital Lowpass Filter Specifications

Filter Type	8th-order elliptic IIR
Passband cutoff	3300 Hz
Passband ripple	± 0.05 dB
Stopband cutoff	4400 Hz
Stopband ripple	-65 dB

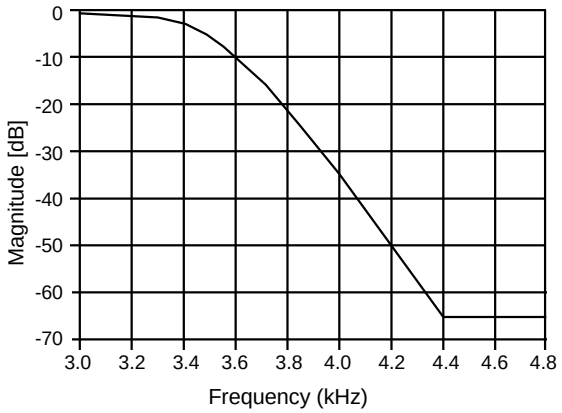

Figure 21. Digital Lowpass Filter

DAC Section

The DAC section consists of a sigma-delta digital-to-analog converter with integral digital filters, an analog smoothing filter, a programmable gain amplifier and selectable output amplifiers.
The voiceband codec´s sigma-delta DAC implements digital filters and a sigma-delta modulator with the same characteristics as the filters and modulator of the ADC.

Analog Smoothing Filter and PGA

The voiceband codec´s analog smoothing filter consists of a continuous-time filter preceded by a switched-capacitor filter. The output gain can be selected by programming bits 1, 2 and 3 of register VCRA according to Table 24.

Output Amplifiers

The voiceband codec has two differential analog outputs (VOUTNOR and VOUTAUX) and one single ended Buzzer output. The output channel can be selected by setting control bits OS0 and OS1 (VCRA6 and VCRA7) according to Table 23. Only one output can be active at any given time. The output signal is dc-biased to the on-chip voiceband reference.
Before switching the output channel and prior to power-up or power-down, it is recommended to mute the outputs by setting the control bit VDACMUTE (VCRA8) to 1. This sets the output gain to minimum and prevents any noise from being generated by the switching process.

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Table 23. Voiceband Output Select

OS1	OS0	Selected Output
0	0	none
0	1	Normal Output
1	0	Auxiliary Output
1	1	Buzzer Output

Secondly, it is suggested to deselect any currently active channel before selecting a new active channel. E.g. changing from the normal to the auxiliary channel should be done as follows: set VDACMUTE (VCRA8) to 1, set OS0 to 0, then set OS1 to 1, and finally set VDACMUTE to 0.

The control bit OD (VCRA0) deactivates all outputs and powers down the PGA and output drivers.

Table 24. Output PGA Gain Settings

OG2	OG1	OG0	Gain
0	0	0	+ 6 dB
0	0	1	+ 3 dB
0	1	0	0 dB
0	1	1	- 3 dB
1	0	0	- 6 dB
1	0	1	- 9 dB
1	1	0	- 12 dB
1	1	1	- 15 dB

The gain of all three outputs is determined by a single PGA. Gains from -15dB up to +6 dB can be selected by setting the control bits OG2, OG1 and OG0 (VCRA3, VCRA2 and VCRA1) according to Table 24.

The normal and the auxiliary outputs are able to drive low impedance speakers (32 Ω) directly. For maximum output swing, a differential configuration is suggested as shown for the normal output in Figure 22. However, also a single-ended configuration can be chosen as shown for the auxiliary output. Either configuration can be used for either approach.

The buzzer output is a single-ended output with limited drive capability. An external transistor buffer is suggested to drive the buzzer directly from the battery. When the buzzer output is not selected (OS0 or OS1 ≠ 1), the BUZZER pin will assume high impedance.

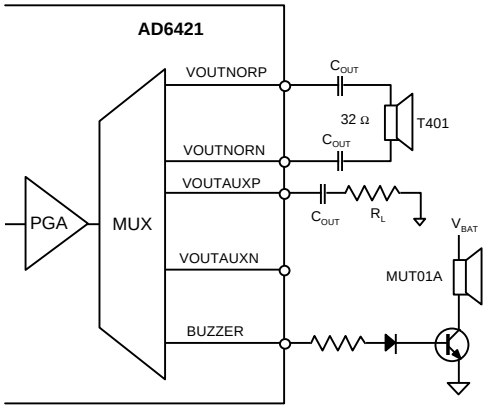

Figure 22. Voiceband Outputs

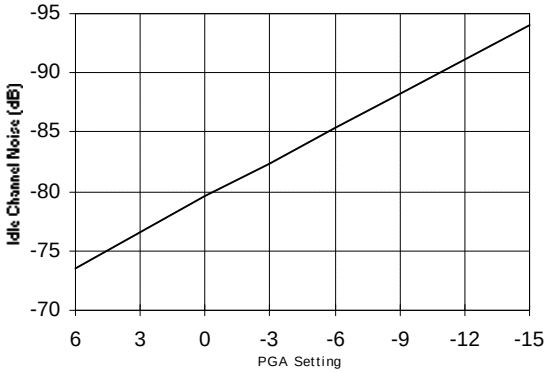

Figure 23. Decoder ICN versus Gain (Typical Values)

Voiceband Serial Port

The voiceband codec of the AD6421 communicates via a bi-directional synchronous serial port. This serial port is activated when PUV, bit VCRA4 is set. The VSPORT has two modes of operation: Normal Mode, allowing 16-bit transfers and, DAI Mode, allowing 13-bit transfers. In all transfers, the MSB is transferred first. Data bits are transferred at a serial clock rate VSCLK. VSCLK equals the master clock frequency divided by an integer number specified by the VSCLKRATE register:
VSCLK = MCLK / (5 × (1+VSCLKRATE)).
The permitted values for VSCLKRATE range from 0 to 16 in Normal Mode and include 24 in DAI Mode.

Normal Mode

In order to receive or transmit data via the VSPORT, VCLKDIS must be set to 0. Setting VCLKDIS to 1 freezes the state of the ADC and DAC including the digital filters. There is a short startup time before VSFS is raised and transmission begins. During data transmission across the serial port, the VSFS is asserted at word-rate. Each word transfer begins on serial clock cycle after VSFS is asserted.

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The output of data via the VSPORT can be prevented by setting bit 2 in VCRC (VSDOFF) to 1. Thus the pin VSDO is tri-stated.

Data input transfers are initiated in the same way as for data outputs. VSFS is internally asserted, the 16-bit word transfer begins one serial clock cycle after VSFS is asserted. Data should be stable shortly after the rising edge of the next VSCLK and is clocked into the AD6421 on the falling edge of VSCLK in that cycle. Each bit of the data word is thus clocked into the AD6421 on the falling edge of VSCLK (MSB first).

DAI Mode

The Digital Audio Interface (DAI) as described in GSM 11.10 provides a direct digital connection for a GSM tester to the digital audio signals within a terminal. It is used to test the speech codec in isolation and also to test the acoustic properties of the terminal´s microphone and earpiece sections in isolation. The VSPORT is configured for 13-bit transfers by setting the DAIMODE bit in the VCRC to 1. The data content of the 13-bit word is the same as the upper 13 bits (MSBs) of a normal 16-bit word.

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SPECIFICATION TERMINOLOGY

The list of specifications given in this datasheet contains several parameters, which are specific to the application of the AD6421.

Baseband Codec

Absolute Group Delay
Absolute group delay (given in time), which describes the rate of change of phase versus frequency. $T_{GD} = d\phi / df$.

Dynamic Range
Dynamic range of a DAC is the ratio of the maximum output signal to the smallest output signal the converter can produce, expressed logarithmically, in decibels ($dB = 20 \log_{10}$ (ratio)). For an N-bit converter, the dynamic range is theoretically 6.02 x N dB. However, this value is degraded by converter noise and inaccuracies in the LSB weight.
For an ADC, the dynamic range is the ratio of the full scale signal to a signal where the signal to noise ratio (SNR) is 0 dB.

Gain Match Between Channels
This is the gain matching between the ITx and QTx channel expressed in dB.

GMSK Phase Trajectory Error
The phase error between the transmitted phase of an ideal GMSK modulator and the transmitted phase of the AD6421 when transmitting a random sequence of data bits. It is specified as a peak phase error and also as an rms. phase error.

Group Delay Linearity
The group delay linearity or differential group delay is the group delay over the full band relative to the group delay at one particular frequency. The reference frequency for the AD6421 is 1 kHz.

Group Delay Between Channels
This is the difference between the group delay of the I and Q channels and is a measure of the phase matching characteristics of the two.

Maximum Phase Effect Instance
This is the time at which a transmitted data bit will have its maximum phase change at the ITx and QTx outputs. This time includes the delay in the GMSK modulator and in the analog low pass filters. Maximum phase effect instance is measured from the Tx clock edge, which latches the data bit, to the ITx and QTx analog outputs.

Phase Matching Between Channels
This is a measure of the phase matching characteristics of the I and Q channels. It is obtained by transmitting all ones and then measuring the difference between the actual phase shift between the I and Q outputs and the ideal phase shift of 90°.

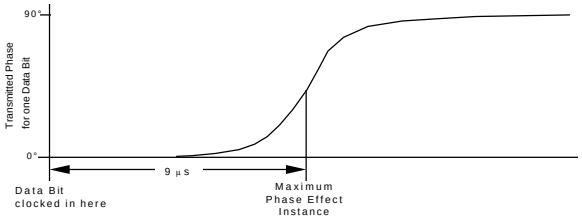

Figure 24. Maximum Phase Effect Instance

Relative Output Power (GMSK Spectrum)
This is the total power of the filtered I and Q analog outputs measured in a bandwidth centered at frequency f_{OFFSET}, relative to twice the power in the 0-15 kHz band (see Figure 25). The bandwidth is 30 kHz for $f_{OFFSET} < 1800$ kHz and 100 kHz for $f_{OFFSET} \geq 1800$ kHz. These measurements are averaged over a random data sequence of 23 kbit long.

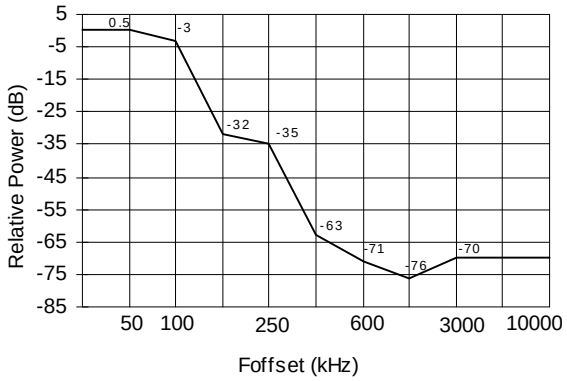

Figure 25. Relative Output Power

Settling Time
This is the digital filter settling time in the receive section. On initial power-up or after returning from the power down mode, it is necessary to wait this amount of time to get useful data.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the receive channel. The signal is the rms. amplitude of the fundamental. Noise is the rms. sum of all nonfundamental signals up to half the sampling frequency, excluding dc. The ratio is dependent upon the number of quantization levels. The theoretical signal to (noise + distortion) ratio for a sine wave is given by: (6.02N + 1.76) dB.

Voiceband Codec

Absolute Gain
Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured differentially with a 1 kHz sine wave at 0 dBm0.

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Gain Tracking Error
Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 0 dBm0 at 1 kHz. Gain tracking error at the absolute signal level is 0 dB by definition.

SNR + THD
Signal-to-noise ratio plus total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the psophometric frequency response, including harmonics but excluding dc.

Idle Channel Noise
Idle channel noise is defined as the total signal energy measured at the output of the device when the inputs are tied together to a bias voltage VREFCAP (measured psophometrically).

Crosstalk
Crosstalk is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of the same signal which couples onto the adjacent channel.

Power Supply Rejection
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

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SPECIFICATIONS

General

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Min	Typ	Max	Units	Test Conditions
Supply Voltage					
AVDD, Analog Supply	2.7		3.3	Volts	
DVDD, Digital Supply	2.7		3.3	Volts	
Difference between any AVDD			200	mV	
Difference between any DVDD			200	mV	
f_{MCLK}, Clock Input Frequency		13		MHz	
Ambient Operating Temperature (T_A)	-40		+85	°C	
Logic Inputs					
V_{INH} , Input High Voltage	V_{DD} - 0.8			Volts	
V_{INL} , Input Low Voltage			0.8	Volts	
I_{INH} , Input Current		10		µA	
C_{IN} , Input Capacitance		10		pF	
Logic Outputs					
V_{OH} , Output High Voltage	V_{DD} - 0.4				$\lvert I_{OUT} \rvert \le 100$ µA
V_{OL} , Output Low Voltage			0.4		$\lvert I_{OUT} \rvert \le 100$ µA
I_{OZL} , Low Level Output 3-State Leakage Current		10		µA	
I_{OZH} , High Level Output 3-State Leakage Current		10		µA	

Absolute Maximum Ratings

(T_A= +25°C unless otherwise stated)

AVDD, DVDD to GND ..... -0.3V to + 4.6V
AGND to DGND ..... -0.3 to +0.3V
Digital I/O Voltage to DGND ..... -0.3V to DVDD + 0.3V
Analog I/O Voltage to AGND..... -0.3V to AVDD + 0.3V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature..... +150°C
TQFP Q_{JA} Thermal Impedance ..... 84 °C/W

Lead temperature, Soldering
Vapor Phase (60 sec)..... +215°C
Infrared (15 sec) ..... +220°C

Notes: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD6421 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges. The AD6421 features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

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SPECIFICATIONS

Baseband Receive Section

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
BASEBAND REFERENCE			
$V_{BREFCAP}$	1.20 ± 5 %	V min/max	
$V_{BREFOUT}$	1.20 ± 5 % ; 1.35 ± 10 %	V min/max	BCRB1 = 0 ; BCRB1 = 1
$I_{BREFOUT}$ Maximum Load Current	100	µA typ	
$V_{BREFOUT}$ TC	50	ppm / °C typ	
RECEIVE CHANNEL			
Resolution	15	Bits	Two's Complement Coding
ADC Signal Range	2 $V_{BREFCAP}$	V_{pp}	
V_{BIAS}			
For both positive and negative analog inputs	$V_{BREFCAP}$/ 2 to (AVDD - $V_{BREFCAP}$ / 2)	Volts	
For positive analog inputs; negative inputs = VBIAS	$V_{BREFCAP}$ to (AVDD - $V_{BREFCAP}$)	Volts	
Signal Range Differential	V_{BIAS} ± $V_{BREFCAP}$ / 2	Volts min/max	
Input Sample Rate	13	MSPS	
Output Word Rate	270.83	kHz	
DC Accuracy			
Pre Calibration Offset Error	± 75	mV max	
Post Calibration Offset Error	-2.5 / + 7.5	mV max	
Post Calibration Offset TC	50	µV/°C typ	TC = Temperature Coefficient
Input Resistance (dc)	1.23	Mω typ	
Input Capacitance	10	pF typ	
Dynamic Specifications			Specified for differential signals only
Dynamic Range	66	dB typ	Input frequency = 67.7 kHz
Signal to (Noise + Distortion)	62	dB min	Input frequency = 67.7 kHz
Gain Error	±0.5	dB max	Input frequency = 67.7 kHz; w.r.t. $V_{BREFCAP}$
Gain Match Between Channels	±0.25	dB max	
Filter Settling Time	47	µs typ	
Frequency Response 0 - 70 kHz	±0.05	dB max / min	Guaranteed by design
85 kHz	-1.0	dB max	Does not include Input Anti-Alias RC Circuit
96 kHz	-3.0	dB max	
135 kHz	-55	dB max	
>170 kHz	-55	dB max	
Absolute Group Delay	23	µs typ	
Group Delay Between Channels	5	ns typ	(0 - 96 kHz)

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SPECIFICATIONS

Baseband Transmit Section

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
Resolution	10	Bits	Two's Complement Coding
V_{BIAS}	$V_{BREFOUT}$ - 60 mV	Volts typ	Internal Reference (REFOUTDIS = 0)
Output Signal Span	$V_{BIAS} \pm 3/7\ V_{BREFCAP}$	Volts	ITxP, ITxN, QTxP, QTxN
Full Scale	$\pm 6/7\ V_{BREFCAP}$	Volts	$12/7V_{BREFCAP}\ V_{PP}$ Differential (ITxP - ITxN, QTxP - QTxN)
Output Signal Full Scale Accuracy	-0.6 / +0.1	dB min/max	w.r.t. $3/7\ V_{BREFCAP}$
Pre Calibration Offset Error	± 50	mV typ	
Post Calibration Offset Error	± 15	mV max	
Post Calibration Offset Error TC	50	µV/°C typ	TC = Temperature Coefficient
Dynamic Specifications			Specified for differential signals only
ITx and QTx Gain Matching	± 0.2	dB max	
Absolute Group Delay	10	µs typ	
Group Delay Linearity	100	ns typ	(0 - 100 kHz)
Phase Matching Between Channels	± 0.05	° typ	
Relative Output Power			No external filtering used
≥ 50 kHz	+0.5	dB max	Bandwidth = 30 kHz
≥ 100 kHz	-3	dB max	Bandwidth = 30 kHz
≥ 200 kHz	-32	dB max	Bandwidth = 30 kHz
≥ 250 kHz	-35	dB max	Bandwidth = 30 kHz
≥ 400 kHz	-63	dB max	Bandwidth = 30 kHz
≥ 600 kHz	-71	dB max	Bandwidth = 30 kHz
≥ 1.8 MHz	-76	dB max	Bandwidth = 30 kHz
≥ 3.0 MHz	-70	dB max	Bandwidth = 30 kHz
≥ 6.0 MHz ≤ 10 MHz	-70	dB typ	Bandwidth = 30 kHz
GMSK Phase Trajectory Error	1 3	° rms max ° peak max	No external filtering used
Maximum Phase Effect Instance	9	µs typ	
Minimum Load Resistance, R_L	5	kΩ min	
Maximum Load Capacitance, C_L	50	pF max	

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SPECIFICATIONS

AGC-DAC, RAMP-DAC

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
AGC DAC			
Resolution	10	Bits	Binary Coding
Output Range (Code 000 to 3FF)	2/32 $V_{BREFCAP}$ to (2 + 2/32) $V_{BREFCAP}$	Volts	
Offset Error (at Code 000)	± 30	mV max	
Gain Error (at Code 3FF)	± 50	mV max	
Integral Nonlinearity	± 2	LSB max	
Differential Nonlinearity	± 2	LSB max	
Update Rate	540	kHz	
Load Resistance	10	kΩ min	
Load Capacitance	50	pF max	
I_{SINK}	50	µA typ	
Full Scale Settling Time	4	µs typ	
LSB Settling Time	2	µs typ	
RAMP DAC			
Resolution	10	Bits	Binary Coding
Output Range (Code 000 to 3FF)	2/32$V_{BREFCAP}$ to (2 + 2/32) $V_{BREFCAP}$	Volts	
Offset Error (at Code 000)	± 30	mV max	
Gain Error (at Code 3FF)	± 30	mV max	
Integral Nonlinearity	± 3	LSB max	
Differential Nonlinearity	± 3	LSB max	
Output Rate	2.16	MHz	interpolated from 540 kHz Update Rate
Load Resistance	2	kΩ min	
Load Capacitance	50	pF max	
I_{SINK}	50	µA typ	
Settling Time			
1/4 Full Scale	2	µs typ	
1 LSB	2	µs typ	
Ramp RAM	2 x 16 x 10	Bits	16 locations each for Ramp Up and Down

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SPECIFICATIONS

AFC-DAC, Auxiliary ADC

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
AFC DAC			
Main DAC (M) Resolution	8	Bits	Binary Coding
Sub DAC (S) Resolution	10	Bits	Binary Coding
Output Range			
from M = 00, S = 000	2/32 $V_{BREFCAP}$	Volts	Linearity is guaranteed only for output voltage from 75mV up to 2.46V
to M = DF, S = 3FF	2.0544 $V_{BREFCAP}$	Volts	
Offset Error (M = 00, S = 000)	± 30	mV max	
Gain Error (M = DF, S = 3FF)	± 30	mV max	
Integral Nonlinearity			
Main DAC	± 0.5	LSB max	Main-DAC LSB
Sub DAC	± 2	LSB max	Sub-DAC LSB (= 1/32 of Main DAC LSB)
Differential Nonlinearity			
Main DAC	± 0.5	LSB max	Main-DAC LSB
Sub DAC	± 2	LSB max	Sub-DAC LSB (= 1/32 of Main DAC LSB)
Update Rate	45	kHz	
Load Resistance	47	kΩ min	
Load Capacitance	50	pF typ	
I_{SINK}	50	µA typ	
Full Scale Settling Time	50	µs max	
LSB Settling Time	25	µs max	
AUXILIARY ADC			
Number of Input Channels	4		
Resolution	10	Bits	
Analog Input Range	0 to $V_{BREFCAP}$	Volts	
Integral Nonlinearity	± 4	LSB typ	Guaranteed no missing codes
Differential Nonlinearity	± 4	LSB typ	
Gain Error	-7 ± 2	LSB typ	
Offset Error	-4.5 ± 1.5	LSB typ	
On Channel Input Resistance R_{IN}	1	kΩ typ	R_{IN} and C_{IN} are in Series
On Channel Input Capacitance C_{IN}	5	pF typ	
Input Leakage Current	1	µA typ	
Conversion Time	12	µs typ	
Power Up Settling Time	10	µs typ	

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SPECIFICATIONS

Voiceband Section

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
Voiceband Reference			
$V_{VREFCAP}$	1.2 ± 5 %	V min/max	
$V_{VREFCAP}$ TC	50	ppm / °C typ	
$V_{VREFOUT}$			unloaded; output impedance 68Ω typ.
	1.2 ± 10 %	V min/max	VR2VEN = 0
	2.2 ± 10 %	V min/max	VR2VEN = 1
Maximum Load Current	1.2	mA	Vrefout only
Maximum Load Capacitance	100	pF max	Vrefout only
Buzzer Output			High Impedance if not selected
Max. Output Swing	1.578	Vpp typ	PGA = 6 dB
Output Bias Voltage	$V_{VREFCAP}$	V nominal	
Signal to Noise + Distortion	62	dB typ	Signal at nominal reference level - (dBm0), PGA = 0 dB
Minimum Load Resistance R_L	2	kΩ min	
Maximum Load Capacitance	50	pF max	

ADC and DAC Filter	Value		Units	Comment
Frequency Response	Min	Max		Filter specifications are
<50 Hz	- ∞	-25	dB	guaranteed by design, but
100 Hz	- ∞	-25	dB	not production tested.
150 Hz	- 0.3	+ 0.3	dB	
200 Hz	- 0.3	+ 0.3	dB	
300 Hz	- 0.2	+ 0.2	dB	
1000 Hz	- 0.2	+ 0.2	dB	
2000 Hz	- 0.3	+ 0.3	dB	
3000 Hz	- 0.8	+ 0.2	dB	
3300 Hz	- 1.1	+ 0.0	dB	
3400 Hz	- 3.4	- 1.6	dB	
4000 Hz	- 45	- 35	dB	
> 4400 Hz	- ∞	- 63	dB	
Group Delay		1.0	ms max	

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SPECIFICATIONS

Voiceband ADC

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
ADC SPECIFICATION			**Tested in Normal Mode (16-bit)** **Specified for Differential Inputs**
Maximum Input Voltage Range	1.578	Vpp max	
	-2.85	dBm	
Nominal Reference Level (0 dBm0)	1.0954	Vpp	
	-6.02	dBm	
Input PGA Gain	0 to +39	dB	14 Steps of 3dB
Absolute Gain			1.0 kHz, 0 dBm0
PGA = 0 dB to 39 dB	-0.75 / +1.0	dB min/max	
Gain Tracking Error	± 0.1	dB typ	1.0 kHz, +3 to -50 dBm0 input
Signal to (Noise + Distortion) PGA = 0 dB to 33 dB	62	dB min	Output Signal at Nominal Reference Level (0 dBm0);
PGA = 36 dB	62	dB typ	Measured Psophometrically
PGA = 39 dB	60	dB typ	
Idle Channel Noise PGA = 0 dB to 33 dB	-64	dBm0 max	Referred to Nominal Reference Level (0 dBm0); Measure Psophometrically For PGA = 27dB to 39 dB see Figure 18.
PGA = 36 dB	-63	dBm0 typ	
PGA = 39 dB	-61	dBm0 typ	
Crosstalk	-65	dB max	ADC input: 1.0 kHz, 0 dBm0; DAC input at Idle
Power Supply Rejection	-55	dB typ	Input at AVDD, DVDD pins: 1.0 kHz, 100 mV_{PP} sine wave
Input Resistance (PGA: 0dB → 39dB)	11 → 0.23	MΩ typ	depending on PGA setting
Coding	Two's Complement		

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SPECIFICATIONS

Voiceband DAC

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

Parameter	Value	Units	Test Conditions / Comments
DAC SPECIFICATION			**Tested in Normal Mode (16-bit)** **Specified for Differential Outputs**
Max. Output Swing (Single Ended)	1.578 -2.85	Vpp max dBm	PGA = 6 dB
Max. Output Swing (Differential)	3.156 3.17	Vpp max dBm	PGA = 6dB
Nominal Output Swing (Single Ended)	1.0954 -6.02	Vpp dBm	PGA = 6 dB
Nominal Output Swing (Differential)	2.1909 0	Vpp dBm	PGA = 6 dB
Output Bias Voltage	$V_{VREFOUT}$	V typ	
Absolute Gain	- 0.5 / +1.0	dB min/max	1.0 kHz, 0 dBm0
Gain Tracking Error	± 0.1	dB typ	1.0 kHz, +3 to -50 dBm0
Signal to (Noise + Distortion) PGA = -15 dB to 6 dB	 60	 dB min	Signal at Nominal Reference Level (0 dBm0); Measured Psophometrically
Idle Channel Noise PGA = -15 dB to +3 dB PGA = +6 dB	 -72 -73	 dBm0 max dBm0 typ	Referenced to Nominal Reference Level (0 dBm0); Measured Psophometrically
Crosstalk	-65	dB max	ADC input: AGND; DAC output: 1.0 kHz, 0 dBm0
Power Supply Rejection	-55	dB typ	Input at AVDD, DVDD pins: 1.0 kHz, 100 mV_{PP} sine wave
Group Delay	1	ms typ	300 - 3000 Hz
Output DC Offset PGA = -15 dB to 0 dB PGA = 3 dB, 6 dB	 100 180	 mV max mV max	
Minimum Load Resistance RL Single Ended Differential	 330 32	 Ω min Ω min	 should be ac coupled
Maximum Load Capacitance CL Single Ended Differential	 500 100	 pF max pF max	
Coding	Two's complement		
Output PGA Gain	-15 to +6	dB	8 Steps of 3 dB

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POWER CONSUMPTION

To support lowest possible power consumption, each section of the AD6421 can be powered down individually (see Figure 26 for details). When each section is again powered up, the specified times must be allowed for the references to power up and for the analog and digital circuitry to settle.

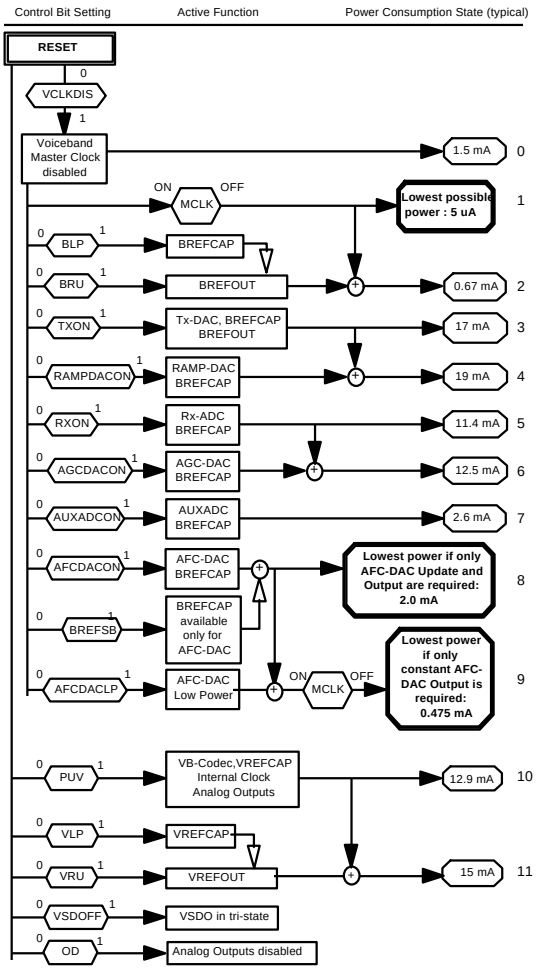

Figure 26. Power Down Options

Baseband & Auxiliary Section Powerdown

The baseband and auxiliary section power down options are independent from the voiceband section.

Reference

For proper operation, all converters in the baseband and auxiliary section require an active baseband reference (BREFCAP). This means that whenever at least one converter in this section is not in power down, BREFCAP is automatically active. When the buffered version of BREFCAP (BREFOUT) is needed to drive external circuitry in the radio section, setting the control bit BLP to 1 prevents BREFCAP from being switched off when all converters are in power down. Keeping BREFCAP active also decreases the settling time of the converters when powered up again.
When only the AFC-DAC needs to be active, BREFCAP can be put into a standby mode in which BREFCAP draws minimum current but is only able to drive the AFC-DAC.

When no reference for external circuitry is required, the output buffer which drives BREFOUT can be switched off by setting the control bit BRU to 0. Note however, that the TxDACs require a bias voltage (V_{BIAS}), which is normally $V_{BREFOUT}$ unless V_{BIAS} is provided from an external source. I.e. unless BREFOUT is disabled by setting REFOUTDIS to 1, TXON automatically activates BREFOUT regardless of the status of BRU.

Converters

All converters in this section can be set into power down mode individually. Setting the control bits TXON, RXON, AUXADCON, RAMPDACON, AGCDACON or AFCDACON to 0 puts the TxDACs, RxADCs, AUXADC, RAMP-DAC, AGC-DAC or the AFC-DAC in power down mode.

Clock

To further reduce power consumption, it is also possible to stop the external master clock signal driving the MCLK input.
In this situation, none of the converters are functional on the AD6421. If the bit AFCDACLP is set to 1 prior to removing the clock, the AFC-DAC will be able to maintain a stable output. It should be noted that once the master clock input has been stopped, the clock output signals of the BSPORT and VSPORT (BSCLK and VSCLK) stop. The phase of the clock output signals are maintained at the instant the master clock was stopped. After providing an active clock input again, the bit AFCDACLP should be reset to 0.

Voiceband Section Powerdown

The whole voiceband section of the AD6421 can be powered down by setting the control bit PUV to 0. This shuts off the voiceband codec, the voiceband reference VREFCAP and the internal clock of the voiceband section. Also the VSPORT can be deactivated by setting the bit VSDOFF to 1 which will set the VSDO pin into tri-state.
If no communication over the VSPORT is required, the VSPORT clock signal can be switched off by setting VCLKDIS (VCRB2) to 1, thereby saving power.

The output amplifier can be powered down independently by setting the bit OD to 1.
When the voiceband section is powered down, VREFCAP can be enabled continuously by setting the control bit VLP to 1. This is useful when external circuitry requires a continuously active reference. This also reduces the settling time of the voiceband codec when powered up again. The buffer which drives VREFOUT can be switched off separately when no reference voltage is required by external circuitry.

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SPECIFICATIONS

Power Consumption

General conditions for power consumption specifications

- **The digital outputs have a capacitive load of 20 pF maximum**
- **All digital input pins are either at 0V or DVDD. (Inputs at threshold levels may result in higher power consumption)**
- **All analog outputs are specified with maximum load**
- **Reference voltage outputs (BREFOUT and VREFOUT) are specified with no dc-load (0.1 µF to GND only)**
- **All AUX and Baseband DACs have the maximum specified digital code**
- **All Baseband and Auxiliary measurements are performed with VSCLK = OFF (VCRB2 = VCLKDIS = 1)**

Conditions for typical power consumption specifications: AVDD = DVDD = 3.0V, TA = 25°C

Conditions for maximum power consumption specifications AVDD = DVDD = 2.7V to 3.3V, TA = -40°C to +85°C

State	Functions ON See also	Comments	MCLK	AIDD typ (mA)	DIDD typ (mA)	Total typ (mA)	Total max (mA)
0	None	RESET, VCLKDIS=1	ON	0.1	1.4	1.5	2.0
1	None	RESET	OFF	1µA	4µA	5µA	0.05
2	BREFCAP + BREFOUT	BRU = 1, BLP = 1, AFCDACLP = 0	OFF	0.655	0.01	0.665	0.95
3	Tx-DAC + BREFCAP + BREFOUT	BLP = 1, REFOUTDIS = 0, BSCLK = 270 kHz	ON	15.0	2.0	17.0	22.5
4	Tx-DAC + BREFCAP + BREFOUT + RAMP-DAC	BLP = 1, REFOUTDIS = 0, BSCLK = 270 kHz	ON	16.9	2.1	19.0	25.5
5	Rx-ADC + BREFCAP	BLP = 1, BRU = 0, BSCLK = 13 MHz	ON	4.9	6.5	11.4	14.5
6	Rx-ADC + BREFCAP + AGC-DAC	BLP = 1, BRU = 0, BSCLK = 13 MHz	ON	5.8	6.7	12.5	16.0
7	Auxiliary ADC + BREFCAP	BLP = 1, BRU = 0	ON	1.2	1.4	2.6	3.5
8	AFC-DAC + BREFCAP [1]	BLP = 0, BRFSB = 1	ON	0.5	1.5	2.0	2.6
9	AFC-DAC + BREFCAP [1]	BLP = 0, BRFSB = 1, AFCDACLP = 1	OFF	0.4	0.075	0.475	0.75
10	VB Codec [2] + VREFCAP	PUV = 1, VLP = 1, VRU = 0, VSDOFF = 0, OD = 0, VSCLK = 2.6 MHz	ON	5.9	7.0	12.9	17.8
11	VB Codec [2] + VREFCAP + VREFOUT	PUV = 1, VLP = 1, VRU = 1, VSDOFF = 0, OD = 0, VSCLK = 2.6 MHz	ON	8.0	7.0	15.0	20.3

Notes :
1) BREFCAP is in low power standby mode
2) VB Codec includes active analog outputs

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TIMING CHARACTERISTICS

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

All timing parameters are guaranteed by design but not production tested

Parameter	Comment	Min	Max	Units
t_1	MCLK Period (see Figure 27)	76		ns
t_2	MCLK Width Low	30.4		ns
t_3	MCLK Width High	30.4		ns
t_4	ASCLK Period (see Figure 28)	153		ns
t_5	ASCLK Width Low ($t_4 \times 0.4$)	60.8		ns
t_6	ASCLK Width High ($t_4 \times 0.4$)	60.8		ns
t_7	BSCLK Period (see Figure 28)	76		ns
t_8	BSCLK Width Low ($t_7 \times 0.4$)	30.4		ns
t_9	BSCLK Width High ($t_7 \times 0.4$)	30.4		ns
t_{10}	VSCLK Period ($t_1 \times 5$) (see Figure 28)	380		ns
t_{11}	VSCLK Width Low ($t_{10} \times 0.55$)	209		ns
t_{12}	VSCLK Width High ($t_{10} \times 0.35$)	133		ns

Master Clock

The master clock MCLK should be set to 13 MHz for proper operation of all converters and internal digital filters. However, MCLK can be stopped for lowest system power consumption if the AD6421 is not needed to be operating.

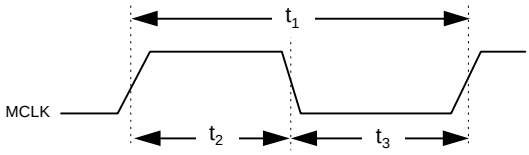

Figure 27. Master Clock

Serial Port Clocks

The Auxiliary Serial Port Clock (ASCLK) is an input and does not need to be programmed. The maximum frequency of ASCLK is 6.5 MHz. The Baseband Serial Port Clock (BSCLK) and the Voiceband Serial Port Clock (VSCLK) are individually programmable by setting the BSCLKRATE and VSCLKRATE registers.

$$\text{BSCLK} = \frac{13\ \text{MHz}}{2 \times \text{BSCLKRATE}}$$

BSCLKRATE can have a value from 0...1023.
When BSCLKRATE = 0, BSCLK = 13MHz.

$$\text{VSCLK} = \frac{13\ \text{MHz}}{5 \times (1 + \text{VSCLKRATE})}$$

Allowable values for VSCLKRATE are 0 to 16 in Normal Mode and 24 in DAI Mode.

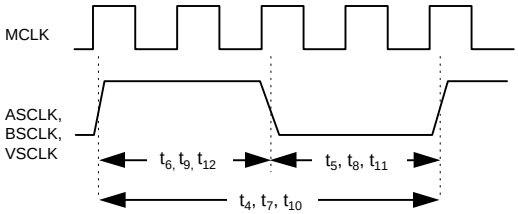

Figure 28. ASCLK, BSCLK, VSCLK

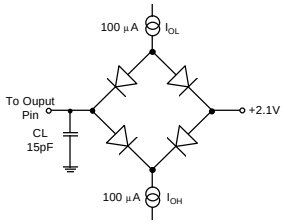

Figure 29. Load Circuit for Timing Specifications

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TIMING CHARACTERISTICS

Baseband Serial Port

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

All timing parameters are guaranteed by design but not production tested

Parameter	Comment (see Figure 30)	Min	Max	Units
t_{29}	BSDI, BSDIFS Setup before BSCLK Low	25		ns
t_{30}	BSDI, BSDIFS Hold after BSCLK Low	10		ns
t_{31}	BSDOFS Delay from BSCLK High		30	ns
t_{32}	BSDOFS Hold after BSCLK High	-15		ns
t_{33}	BSDO Hold after BSCLK High	-15		ns
t_{34}	BSDO Delay from BSCLK High		30	ns
t_{35}	BSDIFS Low to BSDI LSB Read by BSPORT	20		ns
t_{36}	Interval between consecutive BSDIFS pulses	96		ns

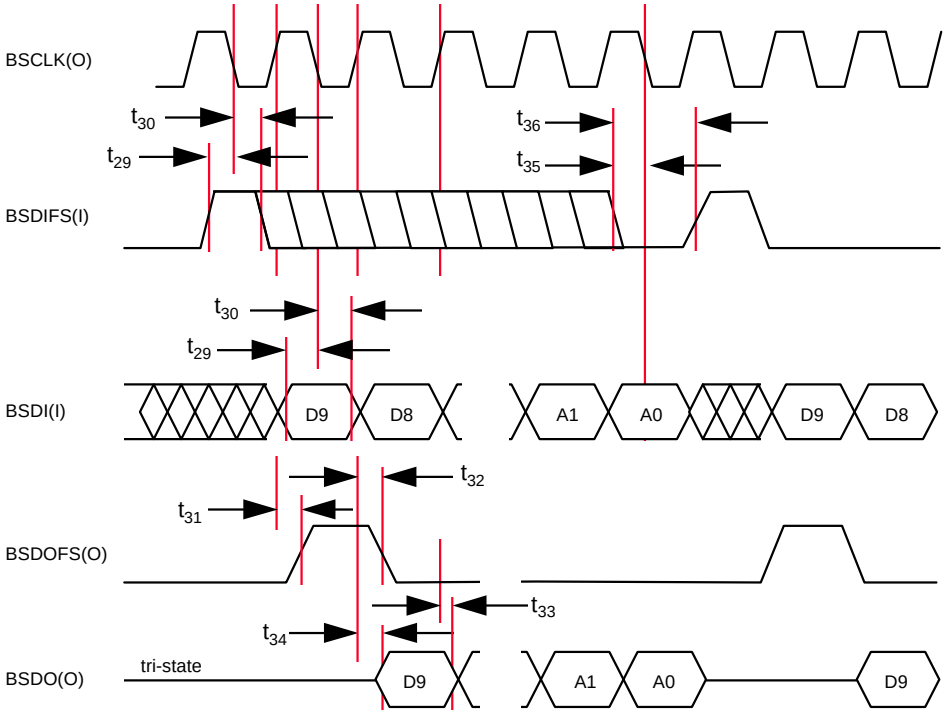

Figure 30. Baseband Serial Port Timing

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TIMING CHARACTERISTICS

Auxiliary Serial Port

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

All timing parameters are guaranteed by design but not production tested

Parameter	**Comment** see Figure 31	Min	Max	Units
t_{21}	ASDIFS Low to ASCLK High	20		ns
t_{22}	ASCLK Low to ASDIFS High	20		ns
t_{23}	ASDI Setup Before ASCLK Low	20		ns
t_{24}	ASDI Hold after ASCLK Low	20		ns
t_{25}	ASDO Delay from ASCLK High		55	ns
t_{26}	ASDO Hold after ASCLK High	-10		ns
t_{27}	ASDOFS Low to ASCLK High	20		ns
t_{28}	ASCLK Low to ASDOFS High	t_5		ns
t_{60}	ASDOFS High to ASDO tri-state			ns

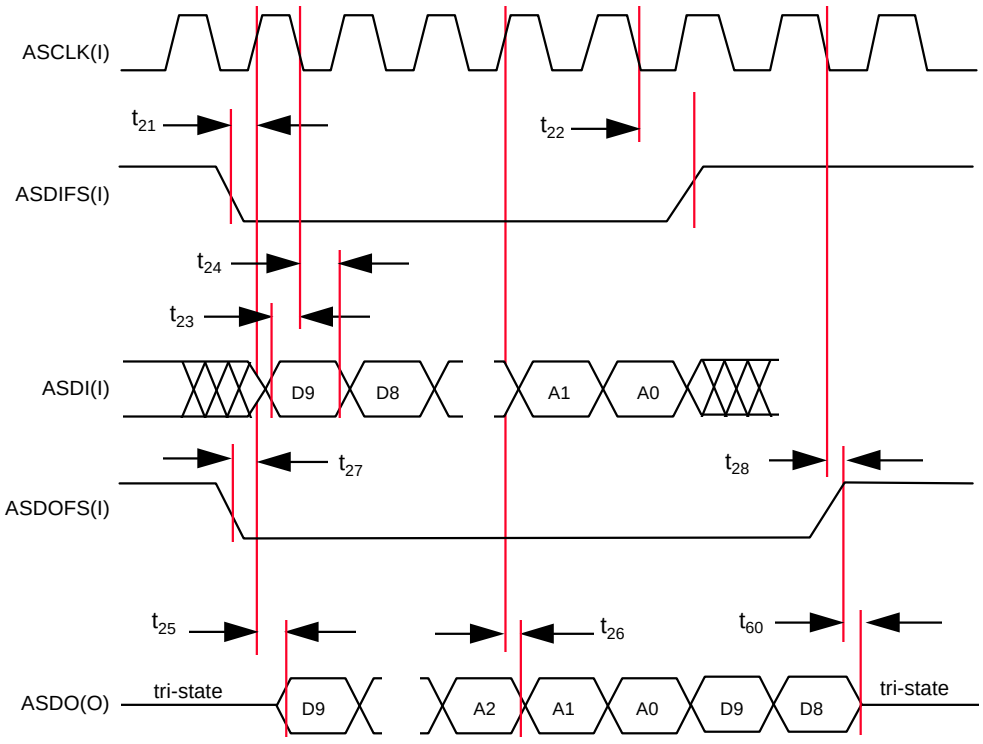

Figure 31. Auxiliary Serial Port Timing

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TIMING CHARACTERISTICS

Voiceband Serial Port

DVDD = AVDD = 2.7V to 3.3V, TA = -40°C to +85°C unless stated otherwise

All timing parameters are guaranteed by design but not production tested

Parameter	Normal Mode see Figure 32 ; DAI Mode see Figure 33	Min	Max	Units
t_{43}	VSDI Setup before VSCLK Low	25		ns
t_{44}	VSDI Hold after VSCLK Low	10		ns
t_{47}	VSFS Delay from VSCLK High		25	ns
t_{48}	VSFS Hold after VSCLK High	-20		ns
t_{49}	VSDO Hold after VSCLK High	-20		ns
t_{50}	VSDO Delay from VSCLK High		20	ns

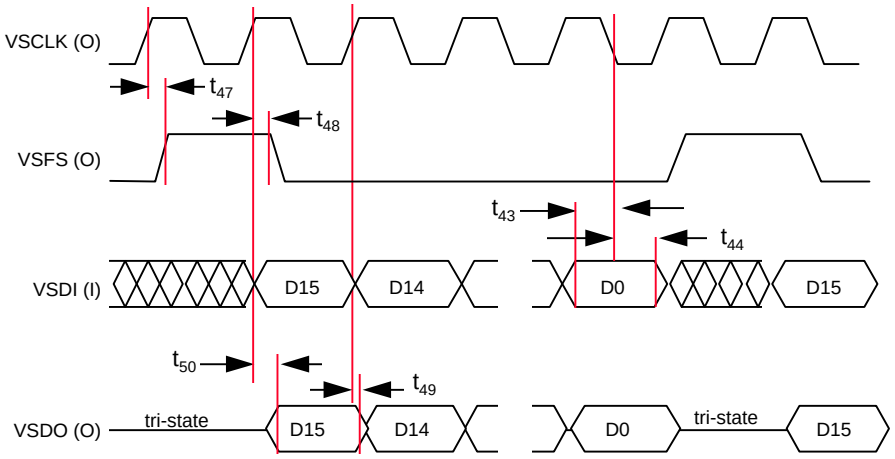

Figure 32. Voiceband Serial Port (Normal Mode) Timing

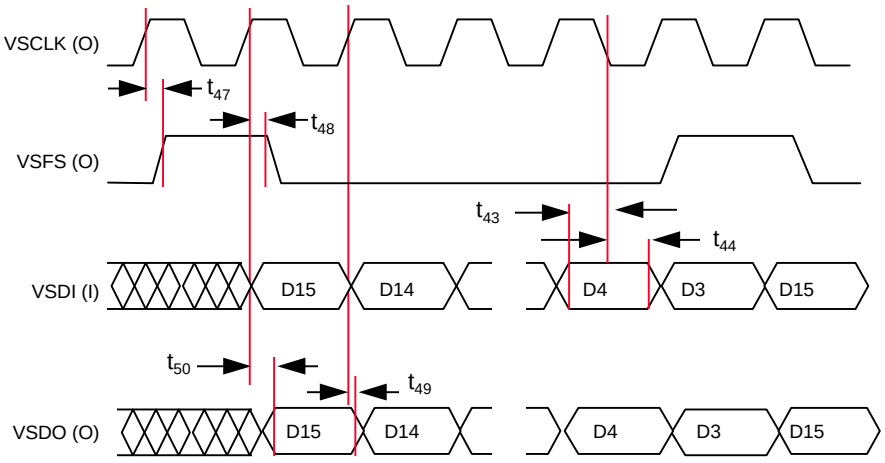

Figure 33. Voiceband Serial Port (DAI Mode) Timing

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JTAG

The JTAG port is a 4 pin interface described in Table 25.

Table 25. JTAG Test Access Port

Pin	Function
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data Input
TDO	Test Data Output

The AD6421 supports the instructions Bypass, Sample / Preload, Extest, IDCode and one private instruction. To put the AD6421 into the required mode, the Instruction Register must be loaded with the Instruction Code shown in Table 26.

Table 26. Instruction Code

Instruction	Instruction Code
Extest	0 0 0
Sample / Preload	0 0 1
IDCode	0 1 0
Private1	0 1 1
Bypass	1 0 0 - 1 1 1

The IDCode is a 32 bit number which can be scanned out through TDO. Its contents are defined below.

MSB LSB

Version (4 bits)	Part Number (16 bits)	Manufacturer ID (11 bits)	
0 hex	277C hex	0E5 hex	1hex
Complete ID Code : 0277C1CB hex			

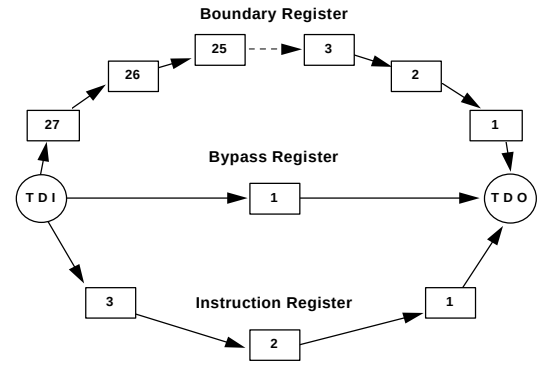

Figure 34. Serial Scan Paths

The boundary scan chain allows all the digital pins on the chip to be connected into a shift register between the TDI and TDO pins. The digital pins can be sampled, or controlled over the JTAG port to perform testing. The order of the boundary scan chain is shown in Table 27.

Table 27. Boundary Chain Cells

TDI		
#	Cell Name	Type
27	ASDI	input
26	ASDIFS	input
25	ASDOFS	input
24	ASDO	output / tri-state
23	*ASDOEN*	tri-state control
22	ASCLK	input
21	MODE	input
20	BSCLK	output / tri-state
19	*BSCLKEN*	tri-state control
18	BSDO	output / tri-state
17	*BSDOEN*	tri-state control
16	BSDOFS	output / tri-state
15	*BSDOFSEN*	tri-state control
14	BSDIFS	input / output
13	*BSDIFSEN*	I/O control
12	BSDI	input
11	MCLK	input
10	RXON	input
9	TXON	input
8	RESET	input
7	VSCLK	output / tri-state
6	*VSCLKEN*	tri-state control
5	VSDO	output / tri-state
4	*VSDOEN*	tri-state control
3	VSFS	output / tri-state
2	*VSFSEN*	tri-state control
1	VSDI	input
TDO		

Cells shown in *ITALIC* are internal cells, which control either the direction of the associated pin or allow to tri-state an output pin. When the tri-state control cell has a value of 1, the associated pin is an output while the pin is tri-stated otherwise. When the I/O control cell has a value of 1, the associated pin is an output while the pin is an input otherwise.

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APPLICATION NOTES

Interface to the Radio Section

The AD6421 interfaces to a standard type of radio architecture, which is widely used in many mobile radios.
Even though no conditions are set in terms of specific components to be used in the radio section, a few principal assumptions have been made.

It is assumed, that the receive signal is provided by the radio in demodulated I and Q format at baseband frequency. Also the AD6421 provides the transmit signal at baseband frequency in form of I and Q components.

It is further assumed, that the gain of the IF amplifier is controlled by an analog voltage like in the AD607, AD6459 or in the AD6432.

The AD6421 generates a voltage for proper control of the burst envelope ramps and amplitude (power level). This voltage is typically fed into a power amplifier controller, which can be a separate circuit or an embedded function like in the AD6432. This controller is necessary due to the nonlinear behavior of the power amplifiers. The power amplifier controller receives a feedback signal from the antenna output, which is proportional to the output power. A control signal for the power amplifier is generated out of the ramp signal in combination with the feedback signal.

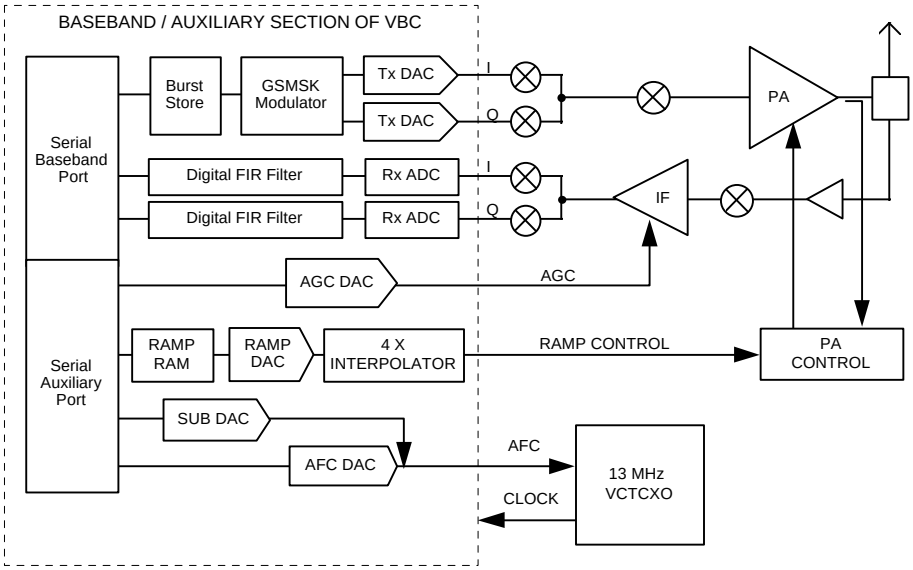

Figure 35. Principal Interface to the Radio Section

Interface to the AD6432

The AD6421 is designed to interface directly to the GSM IF I/Q Modulator and Demodulator AD6432. Figure 36 shows the transmit and receive interfaces, the phase locked loop control, and the gain control circuit interfaces to the AD6432.

Receive Interface

The interface between the AD6421 and the AD6432 provide for in-phase and quadrature (I and Q) channels which can be driven either differentially or in the single-ended configuration. The respective pins (IRxP, IRxN, QRxP, and QRxN) are DC coupled through 4.7 k-Ohm resistors which are integrated within the AD6432. Externally, a 100 pF capacitor is extended to ground to complete a first-order low pass filter with a 3 dB point at 338 kHz. Alternatively, balanced coupling may be used with a single 50 pF capacitor between the complementary signals as illustrated for the I-channel. This low pass filter is the only external filter required to prevent aliasing of the baseband analog signal prior to sampling within the AD6421.

When used in the single ended configuration, the IRxN and QRxN pins of the AD6421 must be externally biased at 1.5 volts to agree with the AD6432 I/Q output common mode. The AD6421 has an external autocalibration mode which can calibrate out any offsets resulting from the IF demodulation circuitry.

Transmit Filter

In order to meet the stringent GSM Phase 2 requirements and depending on the filtering capabilities of the radio section, an external low-pass filter may be required. A passive second order low-pass with a cutoff frequency of 600 kHz
(R = 6.8 kΩ and C = 15 pF) is suggested as shown
in Figure 36.

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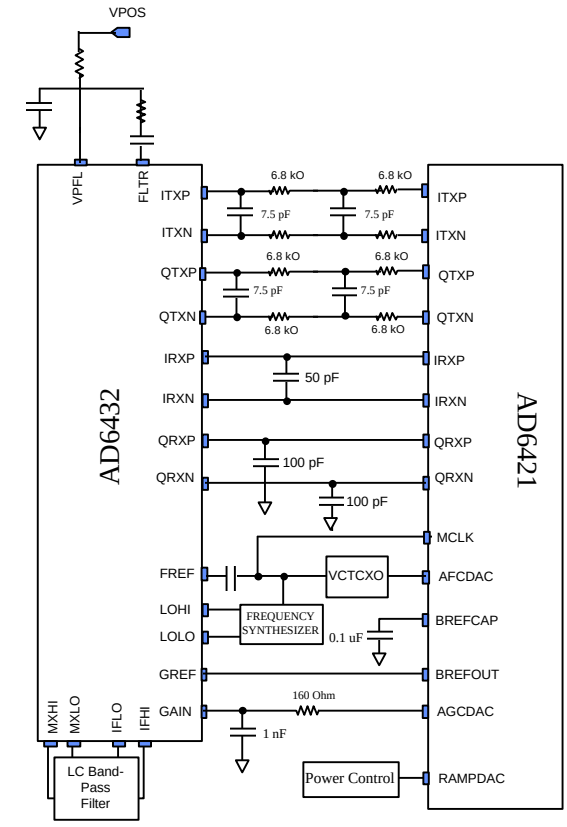

Figure 36. Interface to AD6432

Microphone Interface

The analog inputs of the AD6421 support interfacing to microphones with a minimum of external components as shown in Figure 37.

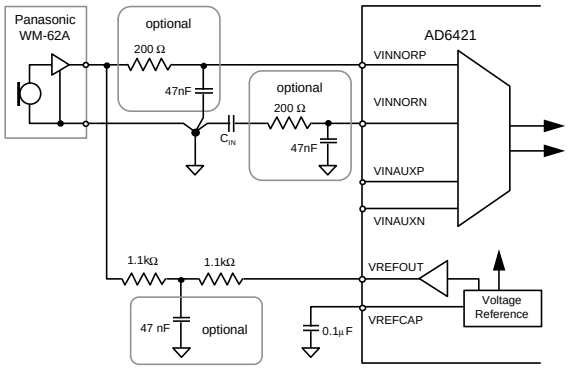

Figure 37 - Example Microphone Interface

Modulating Consecutive Ones

Testing of the radio section performance may require that the AD6421 generates simple and well defined burst signals which contain only consecutive ones. This can be accomplished by certain programming of two TXDELAY registers. For better understanding, please refer to Table 5 and Figure 4 (Transmit Timing).
Firstly, the period T3 is extended to the length of the burst plus a certain design specific delay for the ramp-up process to e.g. 160 T_{BIT}. During T3 the AD6421 automatically modulates consecutive ones. The length of this period is determined by the control register TXDELAY3. TXDELAY3 can have a value from 0 to 1023 Q_{BIT}. Assuming a length of 160 T_{BIT} is desired, the TXDELAY3 should be set to $4 \times 160 = 640$.
Secondly, the period T4 ,where normally the bits of the burst store would be modulated, is reduced to zero. This is accomplished by setting TXDELAY2, which determines the length of T4, to 0. This means, that after T3 has expired, the AD6421 continues directly with T5, where the modulator still modulates consecutive ones.

Grounding and Layout

The analog inputs to the AD6421 can be driven either differentially or single-endedly. In the differential configuration, the excellent Common-Mode Rejection of the part will remove common mode noise on these inputs. The analog and digital supplies of the AD6421 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters on the receive sections of the baseband and voiceband sections will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the AD6421 ADCs is high and the noise levels from the AD6421 are so low, care must be taken with regard to grounding and layout.

The printed circuit board which houses the AD6421 should be designed so that the analog and digital sections are separated and confined to certain sections of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD6421 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD6421. If the AD6421 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD6421.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD6421 to avoid noise coupling. The power supply lines to the AD6421 should use as large a trace as possi-

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ble to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. All analog and digital supplies should be decoupled to AGND and DGND respectively with 0.1μF ceramic capacitors in parallel with 10μF tantalum capacitors. To achieve the best from these decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD6421, it is recommended that the system´s AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD6421 and AGND and the recommended digital supply decoupling capacitors between the DVDD pins and DGND.

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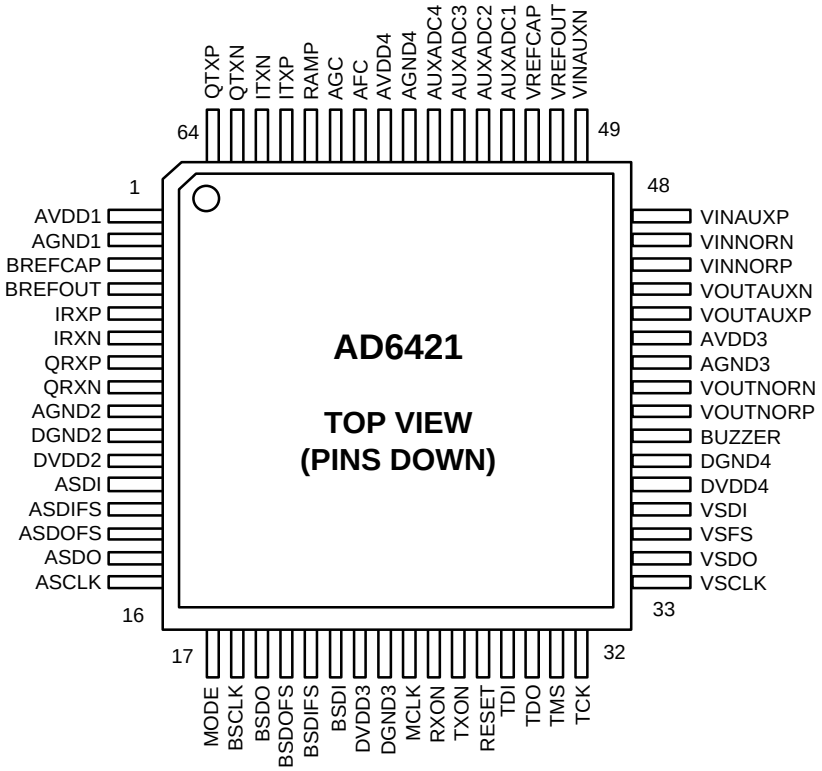
AD6421 PIN LOCATION

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
1	AVDD1	17	MODE	33	VSCLK	49	VINAUXN
2	AGND1	18	BSCLK	34	VSDO	50	VREFOUT
3	BREFCAP	19	BSDO	35	VSFS	51	VREFCAP
4	BREFOUT	20	BSDOFS	36	VSDI	52	AUXADC1
5	IRXP	21	BSDIFS	37	DVDD4	53	AUXADC2
6	IRXN	22	BSDI	38	DGND4	54	AUXADC3
7	QRXP	23	DVDD3	39	BUZZER	55	AUXADC4
8	QRXN	24	DGND3	40	VOUTNORP	56	AGND4
9	AGND2	25	MCLK	41	VOUTNORN	57	AVDD4
10	DGND2	26	RXON	42	AGND3	58	AFC
11	DVDD2	27	TXON	43	AVDD3	59	AGC
12	ASDI	28	RESET	44	VOUTAUXP	60	RAMP
13	ASDIFS	29	TDI	45	VOUTAUXN	61	ITXP
14	ASDOFS	30	TDO	46	VINNORP	62	ITXN
15	ASDO	31	TMS	47	VINNORN	63	QTXN
16	ASCLK	32	TCK	48	VINAUXP	64	QTXP



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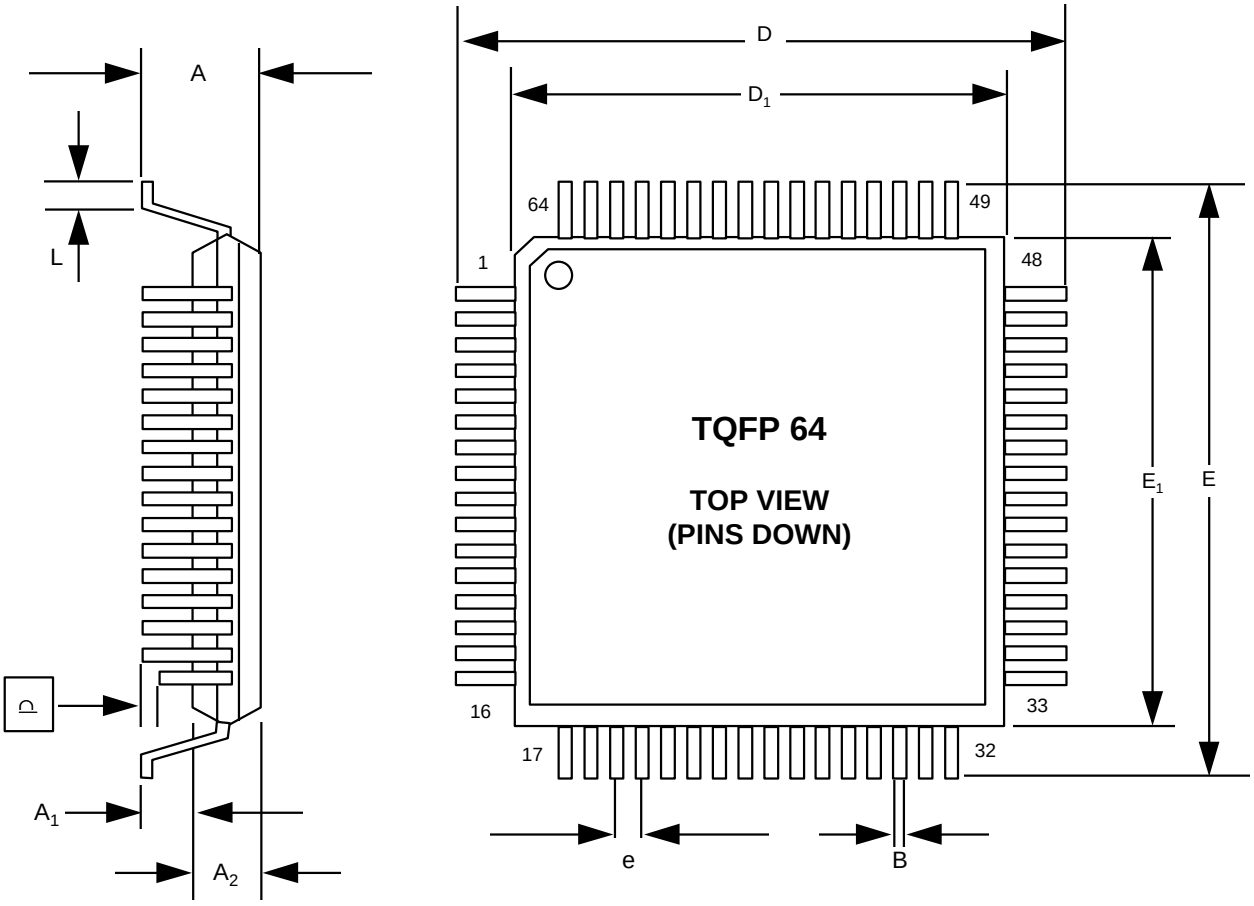
OUTLINE DIMENSIONS

64-Lead Thin Plastic Quad Flatpack (TQFP)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			1.60			0.063
A_1	0.05		0.15	0.002		0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D, E	11.80	12.00	12.20	0.465	0.472	0.480
D_1 , E_1	9.90	10.00	10.10	0.390	0.394	0.340
L	0.50	0.60	0.75	0.020	0.024	0.030
e		0.5			0.012	
B	0.17	0.22	0.27	0.007	0.009	0.011
∩			0.08			0.003

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