1 INTRODUCTION

The TMP68C711E9 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. New design techniques were used to achieve a nominal bus speed of 2.1MHz. In addition, the fully static design allows operation at frequencies down to dc, further reducing power consumption.

1.1 FEATURES

The following are some of the hardware and software highlights.

HARDWARE FEATURES

- 12K Bytes of EPROM
- 512 Bytes of EEPROM
- 512 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  Four Stage Programmable Prescaler
  Three Input Capture/Five Output Compare Functions or
  Four Input Capture/Four Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Plastic Leaded chip Carrier Packages.

SOFTWARE FEATURES

- Enhanced M6800/M6801 Instruction Set
- 16×16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

1.2 GENERAL DESCRIPTION

The high-density CMOS technology used on the TMP68HC11E9 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 12K bytes of EPROM, 512 bytes of electrically eraseable programmable ROM (EEPROM), and 512 bytes of static RAM.

Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected.

Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

A block diagram of the TMP68C711E9 is shown in Figure 1.1

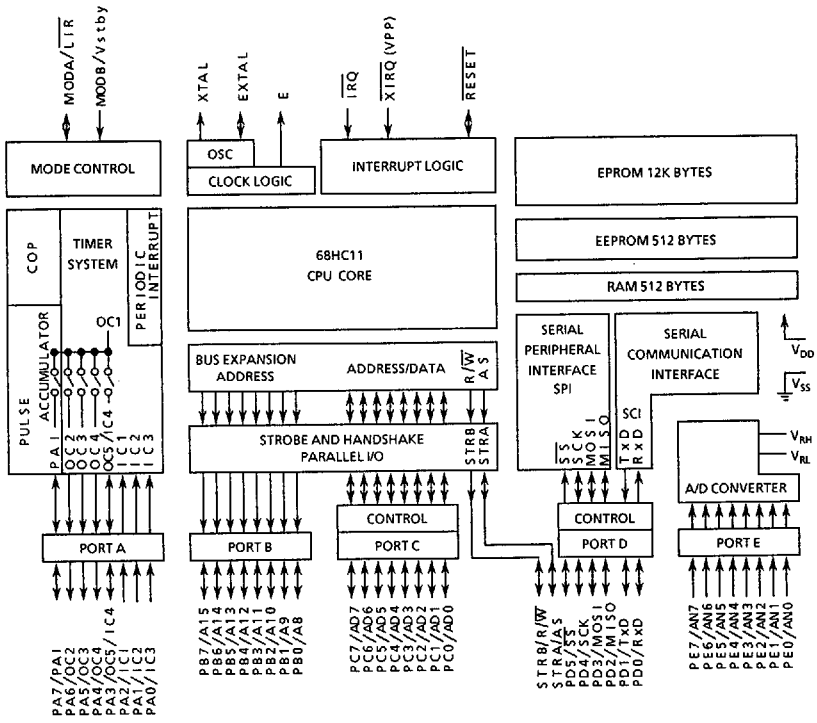


Figure 1.1 TMP68C711E9 Block Diagram

2. OPERATING MODES AND SIGNAL DESCRIPTIONS

This section describes the operating modes and signals of the TMP68C711J6.

2.1 OPERATING MODES

The TMP68C711E9 uses two dedicated pins, MODA and MODB, to select one of two normal operating modes or one of two special operating modes. A value reflecting the MCU status or mode selected is latched on bits SMOD and MDA of the HPRIO register on the rising edge of reset. The normal operating modes are the single-chip and expanded-multiplexed modes. The special operating modes are the bootstrap, test and EPROM emulation modes. Mode selection according to the values encoded on the MODA and MODB pins, and the value latched in the SMOD and MDA bits are shown in the following table:

Table2.1 Operation Modes

Signal			Mode Selected	HPRIO Register	
RESET	MODA	MODB		SMOD	MDA
1	0	1	(Normal) Single-Chip	0	0
1	1	1	(Normal) Expanded-Multiplexed	0	1
1	0	0	(Special) Bootstrap (BOOT)	1	0
1	1	0	(Special) Test	1	1

2.1.1 Single-Chip Operating Mode

In single-chip operating mode, the TMP68C711E9 functions as a monolithic microcontroller without external address or data buses. Port B, port C, strobe A, and strobe B function as general purpose I/O and handshake signals. Refer to SECTION 4 PARALLEL I/O in TMP68HC11A8 for additional information.

2.1.2 Expanded Multiplexed Operating Mode

In expanded multiplexed operating mode, the TMP68C711E9 has the capability of accessing a 64K byte address space. This total address space includes the same on-chip memory addresses used for single-chip operating mode plus external peripheral and memory devices. The expansion bus is made up of port B and port C, and control signals AS and R/$\overline{W}$. Figure 2.1 shows a recommended way of demultiplexing low order addresses from data at port C. The address, R/$\overline{W}$, and AS signals are active and valid for all bus cycles including accesses to internal memory locations.

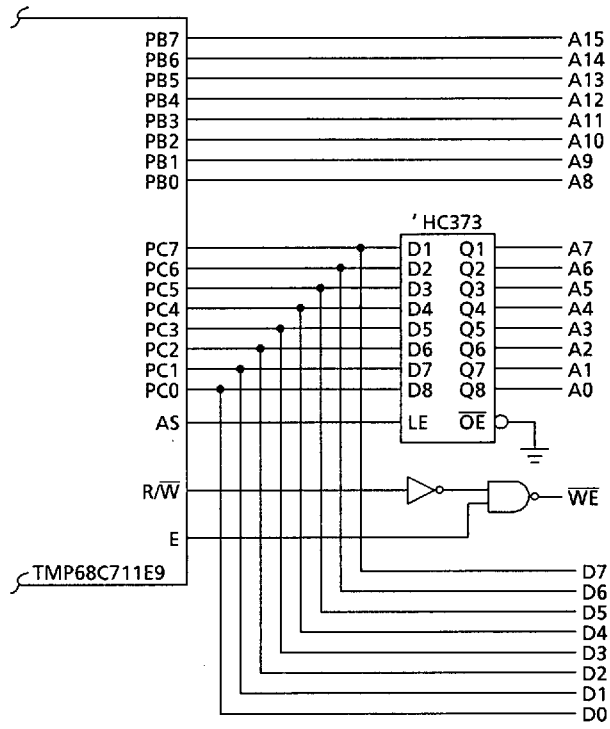


Figure 2.1. Address/Data Demultiplexing

2.1.3 Special Bootstrap Operating Mode

The bootstrap mode is considered a special operating mode as distinguished from the normal single-chip operating mode. This is a very versatile operating mode since there are essentially no limitations on the special purpose program that can be loaded into the internal RAM. The boot loader program is contained in the 192 byte bootstrap ROM. This ROM is enabled only if the MCU is reset in special bootstrap operating mode, and appears as internal memory space at locations $BF40-$BFFF. The boot loader program will use the SCI to read a 512 byte program into on-chip RAM at locations $0000-$01FF. After the final byte is received, control is automatically passed to that program at location $0000.

The TMP68C711E9 communicates through the SCI port. After reset in special bootstrap operating mode, the SCI is running at E clock/16 (7812 baud for E clock equal 2 MHz). If the security feature was specified and the security bit is set, $FF is output by the SCI transmitter. The EEPROM is then erased. If erasure is unsuccessful, $FF is

output again and erasure is attempted again. Upon successful erasure of the EEPROM, all internal RAM is written over with $FF. The CONFIG register is then erased. The boot loader program now proceeds as though the part had not been in security mode.

If the part is not in security mode (or has completed the above erase sequence), a break character is output by the SCI transmitter. For normal use of the boot loader program, the user sends $FF to the SCI receiver at either E clock/16 (7812 baud for E clock = 2MHz) or E clock/104 (1200 baud for E clock = 2MHz).

Note : This $FF is not echoed through the SCI transmitter.

Next the user must download 512 bytes of program data to be put into RAM starting at location $0000. These characters are echoed through the transmitter. When loading is complete, the program jumps to location $0000 and begins executing that code.

If the SCI transmitter pin is to be used, an external pullup resistor is required because port D pins are configured for wire-OR operation.

In special bootstrap operating mode the interrupt vectors are directed to RAM as shown in Table 2.1. This allows the user to use interrupts by way of a jump table. For example: to use the SWI interrupt, a jump instruction would be placed in RAM at locations $00F4, $00F5, and $00F6. When an SWI is encountered, the vector (which is in the boot loader ROM program) will direct program control to location $00F4 in RAM which in turn contains a JUMP instruction to the interrupt service routine.

Table 2.1 Bootstrap Mode Jump Table

Address	Jump Table
00C4	SCI
00C7	SPI
00CA	Pulse Accumulator Input Edge
00CD	Pulse Accumulator Overflow
00D0	Timer Overflow
00D3	Timer Output Compare 5/Input Capture 4
00D6	Timer Output Compare 4
00D9	Timer Output Compare 3
00DC	Timer Output Compare 2
00DF	Timer Output Compare 1
00E2	Timer Input Capture 3
00E5	Timer Input Capture 2
00E8	Timer Input Capture 1
00EB	Real Time Interrupt
00EE	$\overline{\text{IRQ}}$
00F1	$\overline{\text{XIRQ}}$
00F4	SWI
00F7	Illegal Opcode
00FA	COP Fail
00FD	Clock Monitor
Start of Boot Code	Reset

Bootstrap mode (BOOT) is entered out of reset if the voltage level on both MODA and MODB is low. The programming aspect of bootstrap mode, used to program the PROM (EPROM or OTPROM) through the MCU, is entered automatically if $\overline{IRQ}$ is low and programming voltage is available on the V_{PP} pin. $\overline{IRQ}$ should be pulled up while in reset with MODA and MODB configured for bootstrap mode to prevent unintentional programming of the PROM. The PROG mode, used for programming the MCU as though it were a standard 27256 type EPROM is entered by holding a low signal on the MODA, MODB, and $\overline{RESET}$ pins. See Section 4 for details on the PROG mode.

2.1.4 Additional Boot Loader Program Options

The user may tie the receiver to the transmitter (with an external pull-up resistor). This will cause the program to jump directly to the beginning of EEPROM ($B600). Another way to cause the program to jump directly to EEPROM is to transmit either a break or $00 as the first character rather than the normal $FF.

Note that none of these options bypass the security check and so do not compromise those customers using security.

Keep in mind that upon entry to the downloaded program at location $0000, some registers have been changed from their reset states. The SCI transmitter and receiver are enabled which cause port D pins 0 and 1 to be dedicated to SCI use. Also port D is configured for wired-OR operation. It may be necessary for the user to write to the SCCR2 and SPCR registers to disable the SCI and/or port D wire-OR operation.

2.1.5 Special Test Operating Mode

The test mode is a special operating mode intended primarily for factory testing. This mode is very similar to the expanded multiplexed operating mode. In special test operating mode, the reset and interrupt vectors are fetched from external memory locations $BFC0-BFFF rather than $FFC0-$FFFF. There are no time limits for protection of the TMSK2, OPTION, and INIT registers, so these registers may be written repeatedly. Also a special TEST1 register is enabled which allows several factory test functions to be invoked.

The special test operating mode is not recommended for use by an end user because of the reduced system security;however, an end user may wish to come out of reset in special test operating mode. Then, after some initialization, the SMOD and MDA bits could be rewritten to select a normal operating mode to re-enable the protection features.

2.1.6 PROM Emulation Mode (PROG)

PROM emulation mode, the PROG aspect of bootstrap mode, is used for programming the MCU as though it were a standard 27256 type EPROM. This mode is entered by holding a low signal on the MODA, MODB, and $\overline{\text{RESET}}$ pins. A socket adapter is required for OTPROM or EPROM programming in this mode.

2.2 SIGNAL PIN DESCRIPTIONS

The following paragraphs provide a description of the input/output signals. Reference is made, where applicable, to other sections that contain more detail about the function being performed.

2.2.1 Input Power (V_{DD}) and Ground (V_{SS})

Power is supplied to the microcontroller using these pins. V_{DD} is the positive power input and V_{SS} is ground. Although the TMP68C711E9 is a CMOS device, very fast signal transitions are present on many of its pins. Short rise and fall times are present even when the microcontroller is operating at slow clock rates. Special care must be taken to provide good power supply bypassing at the MCU. Recommended bypassing would include a 0.1 μF ceramic capacitor between the V_{DD} and V_{SS} pins and physically adjacent to one of the two pins. A bulk capacitance, whose size depends on the other circuity in the system, should also be present on the circuit board.

2.2.2 Reset ($\overline{\text{RESET}}$)

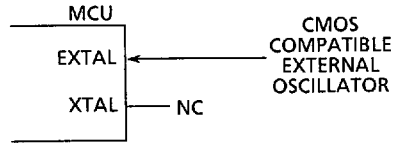
This active low bidirectional control signal is used as an input to initialize the TMP68C711E9 to a known startup state, and as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or computer operating properly (COP) watchdog circuit. This reset signal is significantly different from the reset signal used on other Motorola MCUs. Please refer to SECTION 9 RESETS, INTERRUPTS, AND LOW POWER MODES in TMP68HC11E9 before designing circuitry to generate or monitor this signal.

2.2.3 Crystal Driver and External Clock Input (XTAL, EXTAL)

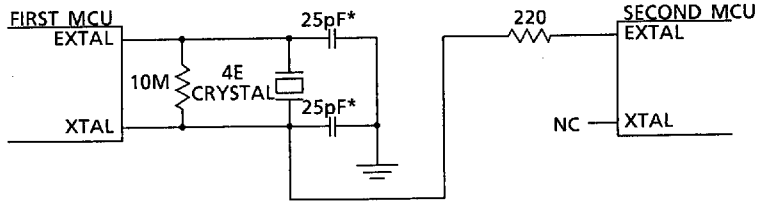
These two pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. The frequency applied to these pins shall be four times higher than the desired E clock rate. The XTAL pin is normally left unterminated when using an external CMOS compatible clock input to the EXTAL pin. The XTAL output is normally intended to drive only a crystal.

The XTAL output may be buffered with a high input impedance buffer such as the 74HC04, or it may be used to drive the EXTAL input of another TMP68HC11.

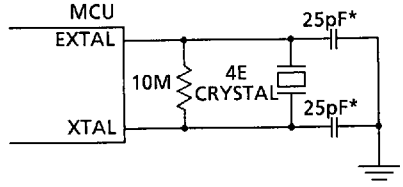
In all cases take extra care in the circuit board layout around the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to Figures 2.2 for diagrams of oscillator circuits.



(a) External Oscillator Connections



(b) One Crystal Driving Two MCUs



(c) Common Crystal Connections

*Values include all stray capacitances.

Figure 2.1 Oscillator Connections

2.2.4 E Clock Output (E)

This is the output connection for the internally generated E clock which can be used as a timing reference. The frequency of the E clock output is actually one fourth that of the input frequency at the XTAL and EXTAL pins. When the E clock output is low an internal process is taking place and, when high, data is being accessed. The E clock signal is halted when the MCU is in STOP mode.

2.2.5 Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ input provides a means for requesting asynchronous interrupts to the TMP68C711E9. It is program selectable (OPTION register) with a choice of either negative edge-sensitive or level-sensitive triggering, and is always configured to level-sensitive triggering by reset. The $\overline{IRQ}$ pin requires an external pullup resistor to V_{DD} (typically 4.7K ohm).

2.2.6 Non-Maskable Interrupt ($\overline{XIRQ}$/Vpp)

This input provides a means for requesting a non-maskable interrupt, after reset initialization. During reset, the X bit in the condition code register is set and any interrupt is masked until MCU software enables it. The $\overline{XIRQ}$ input is level sensitive and requires an external pullup resistor to V_{DD}.

2.2.7 Mode A/Load Instruction Register and Mode B/Standby Voltage (MODA/$\overline{LIR}$, MODB/V_{STBY})

During reset, MODA and MODB are used to select one of the four operating modes. Refer to Table 2.1 Paragraph 2.1 OPERATING MODES provides additional information.

After the operating mode has been selected, the $\overline{LIR}$ pin provides an open-drain output to indicate that an instruction is starting. All instructions are made up of a series of E clock cycles. The $\overline{LIR}$ signal goes low during the first E clock cycle of each instruction (opcode fetch). This output is provided as an aid in program debugging.

The V_{STBY} signal is used as the input for RAM standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal 512-byte RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

2.2.8 A/D Converter Reference Voltages (V_{RL}, V_{RH})

These two inputs provide the reference voltages for the analog-to-digital converter circuitry.

2.2.9 Strobe B and Read/Write (STRB/R/$\overline{W}$)

This signal acts as a strobe B output or as a data bus direction indicator depending on the operating mode.

In single-chip operating mode, the STRB output acts as a programmable strobe for handshake with other parallel I/O devices. Refer to SECTION 4 PARALLEL I/O in TMP68HC11A8 for additional information.

In expanded multiplexed operating mode, R/$\overline{W}$ is used to control the direction of transfers on the external data bus. A low on the R/$\overline{W}$ signal indicates data is being written to the external data bus. A high on this signal indicates that a read cycle is in progress. R/$\overline{W}$ will stay low during consecutive data bus write cycles, such as in a double-byte store. The NAND of inverted R/$\overline{W}$ with the E clock should be used as the write enable signal for an external static RAM.

2.2.10 Strobe A and Address Strobe (STRA/AS)

This signal acts as an edge detecting strobe A input or as an address strobe bus control output depending on the operating mode.

In single-chip operating mode, the STRA input acts as a programmable strobe for handshake with other parallel I/O devices. Refer to SECTION 4 PARALLEL I/O in TMP68HC11A8 for additional information.

In expanded multiplexed operating mode, the AS output is used to demultiplex the address and data signals at port C. Refer to 2.1.2 Expanded Multiplexed Operating Mode for additional information.

2.2.11 Port Signals

Ports A, D, and E signals are independent of the operating mode. Port B provides eight general purpose output signals in single-chip operating modes and provides eight high-order address signals when the microcontroller is in expanded multiplexed operating modes. Port C provides eight general purpose input/output signals when the microcontroller is in single-chip operating modes. When the microcontroller is in expanded multiplexed operating modes, port C is used for a multiplexed address/data bus. Table 2.2 shows a summary of the 40 port signals as they relate to the operating modes. Unused inputs and I/O pins configured as inputs should be terminated high or low.

Table 2.2 Port Signal Summary

Port-Bit	Single-Chip and Bootstrap Mode	Expanded Multiplexed and Special Test Mode
A-0	PA0/IC3	PA0/IC3
A-1	PA1/IC2	PA1/IC2
A-2	PA2/IC1	PA2/IC1
A-3	PA3/OC5/IC4/and-or OC1	PA3/OC5/IC4/and-or OC1
A-4	PA4/OC4/and-or OC1	PA4/OC4/and-or OC1
A-5	PA5/OC3/and-or OC1	PA5/OC3/and-or OC1
A-6	PA6/OC2/and-or OC1	PA6/OC2/and-or OC1
A-7	PA7/PAI/and-or OC1	PA7/PAI/and-or OC1
B-0	PB0	A8
B-1	PB1	A9
B-2	PB2	A10
B-3	PB3	A11
B-4	PB4	A12
B-5	PB5	A13
B-6	PB6	A14
B-7	PB7	A15
C-0	PC0	A0/D0
C-1	PC1	A1/D1
C-2	PC2	A2/D2
C-3	PC3	A3/D3
C-4	PC4	A4/D4
C-5	PC5	A5/D5
C-6	PC6	A6/D6
C-7	PC7	A7/D7
D-0	PD0/RxD	PD0/RxD
D-1	PD1/TxD	PD1/TxD
D-2	PD2/MISO	PD2/MISO
D-3	PD3/MOSI	PD3/MOSI
D-4	PD4/SCK	PD4/SCK
D-5	PD5/$\overline{SS}$	PD5/$\overline{SS}$
D-6	STRA	AS
D-7	STRB	R/$\overline{W}$
E-0	PE0/AN0	PE0/AN0
E-1	PE1/AN1	PE1/AN1
E-2	PE2/AN2	PE2/AN2
E-3	PE3/AN3	PE3/AN3
E-4	PE4/AN4	PE4/AN4
E-5	PE5/AN5	PE5/AN5
E-6	PE6/AN6	PE6/AN6
E-7	PE7/AN7	PE7/AN7

2.2.11.1 Port A.

Port A may be configured for: four input capture functions (IC1, IC2, IC3, IC4) and three output compare functions (OC2, OC3, OC4), or three input capture functions (IC1, IC2, IC3) and four output compare functions (OC2, OC3, OC4, OC5) , and either a pulse accumulator input (PAI) or a fifth output compare function (OC1) . Refer to 8.1 PROGRAMMABLE TIMER in TMP68HC11E9 for additional information.

Any port A pin that is not used for its alternate timer function may be used as a general-purpose input or output line.

2.2.11.2 Port B.

While in single-chip operating modes, all of the port B pins are general-purpose output pins. During MCU reads of this port, the level sensed at the input side of the port B output drivers is read. Port B may also be use in a simple strobed output mode where an output pulse appears at the STRB signal each time data is written to port B.

When in expanded multiplexed operating modes, all of the port B pins act as high order address output signals. During each MCU cycle, bits 8 through 15 of the address are output on the PB0-PB7 lines respectively.

2.2.11.3 Port C.

While in single-chip operating modes, all port C pins are general-purpose input/output pins. Port C inputs can be latched by providing an input transition to the STRA signal. Port C may also be used in full handshake modes of parallel I/O where the STRA input and STRB output act as handshake control lines.

When in expanded multiplexed operating modes, all port C pins are configured as multiplexed address/data signals. During the address portion of each MCU cycle, bits 0 through 7 of the address are output on the PC0-PC7 lines. During the data portion of each MCU cycle (E high), pins 0 through 7 are bidirectional data signals (D0-D7). The direction of data at the port C pins is indicated by the R/$\overline{W}$ signal.

2.2.11.4 Port D.

Port D pins 0-5 may be used for general purpose I/O signals. Port D pins alternately serve as the serial communications interface (SCI) and serial peripheral interface (SPI) signals when those subsystems are enabled.

Pin PD0 is the receive data input (RxD) signal for the serial communication interface (SCI).

Pin PD1 is the transmit data output (TxD) signal for the SCI.

Pins PD2 through PD5 are dedicated to the SPI. PD2 is the master-in-slave-out (MISO) signal. PD3 is the master-out-slave in (MOSI) signal. PD4 is the serial clock (SCK) signal and PD5 is the slave select ($\overline{SS}$) input.

2.2.11.5 Port E.

Port E is used for general-purpose inputs and/or analog-to-digital (A/D) input channels. Reading port E during the sampling portion of an A/D conversion could cause very small disturbances and affect the accuracy of that result. If very high accuracy is required, avoid reading port E during conversions.

3. ON-CHIP MEMORIES

This section describes the on-chip ROM, RAM, and EEPROM memories. The memory maps for each mode of operation are shown and the RAM and I/O mapping register (INIT) is described. The INIT register allows the on-chip RAM and the 64 control registers to be moved to suit the needs of a particular application.

3.1 MEMORY MAPS

Composite memory maps for each mode of operation are shown in Figure 3.1. Memory locations are shown in the shaded areas and the contents of these shaded areas are shown to the right. These modes include single-chip, expanded multiplexed, special bootstrap, and special test.

Single-chip operating modes do not generate external addresses. Refer to Table 3.1 for a full list of the registers.

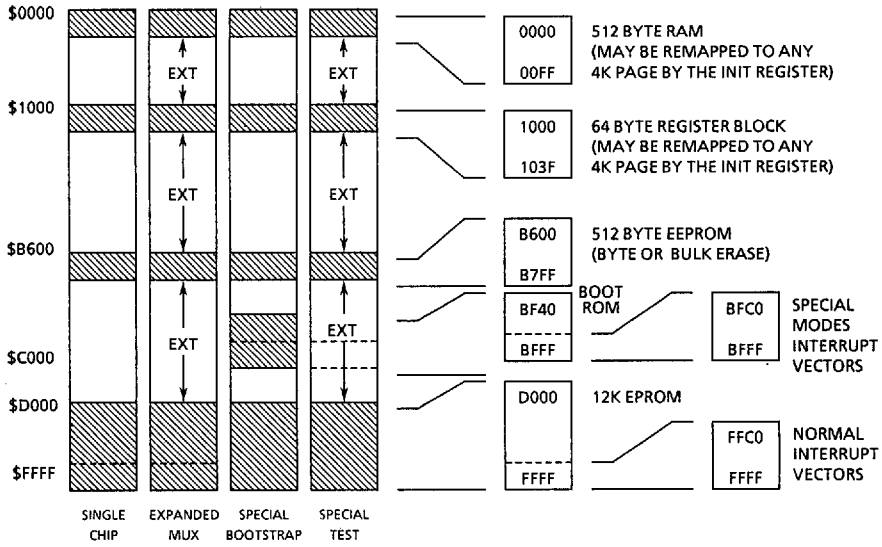


Figure 3.1 Memory Maps

In expanded multiplexed operating modes, memory locations are basically the same as the single-chip operating modes; however, the locations between the shaded areas (designated EXT) are for externally addressed memory and I/O. If an external memory or I/O device is located to overlap an enabled internal resource, the internal resource will take priority. For reads of such an address the data (if any) driving the port C data inputs is ignored and will not result in any harmful conflict with the internal read. For writes to such an address data is driven out of the port C data pins as well as to the internal location. No external devices should drive port C during write accesses to internal locations; however, there is normally no conflict since the external address decode and/or data direction control should incorporate the R/$\overline{W}$ signal in their development. The R/$\overline{W}$, AS, address, and write data signals are valid for all accesses including accesses to internal memory and registers.

The special bootstrap operating mode memory locations are similar to the single-chip operating mode memory locations except that a bootstrap program at memory locations $BF40 through $BFFF is enabled. The reset and interrupt vectors are addressed at $BFC0-$BFFF while in the special bootstrap operating mode. These vector addresses are within the 192 byte memory used for the bootstrap program.

The special test operating mode memory map is the same as the expanded multiplexed operating mode memory map except that the reset and interrupt vectors are located at external memory locations $BFC0-$BFFF.

Table 3.1 Register and Control Bit Assignments (Sheet 1 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1000	Bit 7	–	–	–	–	–	–	Bit 0	PORTA	I/O Port A
	U	U	U	U	U	U	U	U		
$1001									Reserved	
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC	Parallel I/O Control Register
	0	0	0	0	0	0	1	1		
$1003	Bit 7	–	–	–	–	–	–	Bit 0	PORTC	I/O Port C
	U	U	U	U	U	U	U	U		
$1004	Bit 7	–	–	–	–	–	–	Bit 0	PORTB	Output Port B
	0	0	0	0	0	0	0	0		
$1005	Bit 7	–	–	–	–	–	–	Bit 0	PORTCL	Alternate Latched Port C
	U	U	U	U	U	U	U	U		
$1006									Reserved	
$1007	Bit 7	–	–	–	–	–	–	Bit 0	DDRC	Data Direction for Port C
	0	0	0	0	0	0	0	0		
$1008			Bit 5	–	–	–	–	Bit 0	PORTD	I/O Port D
			U	U	U	U	U	U		
$1009			Bit 5	–	–	–	–	Bit 0	DDRD	Data Direction for Port D
			0	0	0	0	0	0		
$100A	Bit 7	–	–	–	–	–	–	Bit 0	PORTE	Input Port E
	U	U	U	U	U	U	U	U		
$100B	FOC1	FOC2	FOC3	FOC4	FOC5				CFORC	Compare Force Register
	0	0	0	0	0					
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3				OC1M	OC1 Action Mask Register
	0	0	0	0	0					
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3				OC1D	OC1 Action Data Register
	0	0	0	0	0					
$100E	Bit 15	–	–	–	–	–	–	Bit 8	TCNT	Timer Counter Register
$100F	Bit 7	–	–	–	–	–	–	Bit 0		
$1010	Bit 15	–	–	–	–	–	–	Bit 8	TIC1	Input Capture 1 Register
$1011	Bit 7	–	–	–	–	–	–	Bit 0		
$1012	Bit 15	–	–	–	–	–	–	Bit 8	TIC2	Input Capture 2 Register
$1013	Bit 7	–	–	–	–	–	–	Bit 0		
$1014	Bit 15	–	–	–	–	–	–	Bit 8	TIC3	Input Capture 3 Register
$1015	Bit 7	–	–	–	–	–	–	Bit 0		
$1016	Bit 15	–	–	–	–	–	–	Bit 8	TOC1	Output Compare 1 Register
$1017	Bit 7	–	–	–	–	–	–	Bit 0		
$1018	Bit 15	–	–	–	–	–	–	Bit 8	TOC2	Output Compare 2 Register
$1019	Bit 7	–	–	–	–	–	–	Bit 0		

Table 3.1 Register and Control Bit Assignments (Sheet 2 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$101A	Bit 15	–	–	–	–	–	–	Bit 8	TOC3	Output Compare 3 Register
$101B	Bit 7	–	–	–	–	–	–	Bit 0		
$101C	Bit 15	–	–	–	–	–	–	Bit 8	TOC4	Output Compare 4 Register
$101D	Bit 7	–	–	–	–	–	–	Bit 0		
$101E	Bit 15	–	–	–	–	–	–	Bit 8	TOC5	Output Compare 5 Register
$101F	Bit 7	–	–	–	–	–	–	Bit 0		
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1	Timer Control Register 1
	0	0	0	0	0	0	0	0		
$1021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2	Timer Control Register 2
	0	0	0	0	0	0	0	0		
$1022	OC1I	OC2I	OC3I	OC4I	I4OC5I	IC1I	IC2I	IC3I	TMSK1	Timer Interrupt Mask Register 1
	0	0	0	0	0	0	0	0		
$1023	OC1F	OC2F	OC3F	OC4F	I4OC5F	IC1F	IC2F	IC3F	TFLG1	Timer Interrupt Flag Register 1
	0	0	0	0	0	0	0	0		
$1024	TOI	RTII	PAOVI	PAII			PR1	PR0	TMSK2	Timer Interrupt Mask Register 2
	0	0	0	0	0	0	0	0		
$1025	TOF	RTIF	PAOVF	PAIF					TFLG2	Timer Interrupt Flag Register 2
	0	0	0	0	0	0	0	0		
$1026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL	Pulse Accumulator Control Register
	0	0	0	0	0	0	0	0		
$1027	Bit 7	–	–	–	–	–	–	Bit 0	PACNT	Pulse Accumulator Count Register
	U	U	U	U	U	U	U	U		
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR	SPI Control Register
	0	0	0	0	0	1	U	U		
$1029	SPIF	WCOL		MODF					SPSR	SPI Status Register
	0	0	0	0	0	0	0	0		
$102A	Bit 7	–	–	–	–	–	–	Bit 0	SPDR	SPI Data Register
	U	U	U	U	U	U	U	U		
$102B	TCLR		SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD	SCI Baud Rate Control
	0	0	0	0	0	U	U	U		
$102C	R8	T8		M	WAKE				SCCR1	SCI Control Register 1
	U	U	0	0	0	0	0	0		
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2	SCI Control Register 2
	0	0	0	0	0	0	0	0		
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE		SCSR	SCI Status Register
	1	1	0	0	0	0	0	0		
$102F	Bit 7	–	–	–	–	–	–	Bit 0	SCDR	SCI Data (Read RDR, Write TDR)
	U	U	U	U	U	U	U	U		
$1030	CCF		SCAN	MULT	CD	CC	CB	CA	ADCTL	A/D Control Register
	0	0	U	U	U	U	U	U		
$1031	Bit 7	–	–	–	–	–	–	Bit 0	ADR1	A/D Result Register 1
	U	U	U	U	U	U	U	U		
$1032	Bit 7	–	–	–	–	–	–	Bit 0	ADR2	A/D Result Register 2
	U	U	U	U	U	U	U	U		
$1033	Bit 7	–	–	–	–	–	–	Bit 0	ADR3	A/D Result Register 3
	U	U	U	U	U	U	U	U		
$1034	Bit 7	–	–	–	–	–	–	Bit	ADR4	A/D Result Register 4
	U	U	U	U	U	U	U	U		
$1035				PTCON	BPRT3	BPRT2	BPRT1	BPRT0	BPROT	EEPROM Block Protect Reg.
	0	0	0	1	1	1	1	1		

Table 3.1 Register and Control Bit Assignments (Sheet 2 of 2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
$1036 Thru $1038									Reserved	
$1039	ADPU	CSEL	IRQE	DLY	CME		CR1	CR0	OPTION	System Configuration Options
	0	0	0	1	0	0	0	0		
$103A	Bit 7	–	–	–	–	–	–	Bit 0	COPRST	Am/Reset COP Timer Circuity
	U	U	U	U	U	U	U	U		
$103B	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	PGM	PPROG	EEPROM and PROM Programming Control Register
	0	0	0	0	0	0	0	0		
$103C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO	Highest Prioriy 1-Bit Int and Misc
	–	–	–	–	0	1	0	1		
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT	RAM and I/O Mapping Register
	0	0	0	0	0	0	0	1		
$103E	TILOP		OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1	Factory TEST Control Register
	0	0	0	0	–	0	0	0		
$103F						NOCOP	ROMON	EEON	CONFIG	COP, EPROM and EEPROM Enables
	0	0	0	0	1	*	*	*		

Initial state
(Control bit only)

0 : Clear
1 : Set
U : Undefined
– : Effected by a MOD pin status
* : Fixed with a programming value of register CONFIG
□ : Bits changed only within 64E clock cycles after reset

4. PROGRAMMABLE READ ONLY MEMORY (PROM)

The TMP68C711E9 has 12K bytes of programmable read only memory (PROM), either erasable programmable read only memory (EPROM) or one-time programmable read only memory (OTPROM). The PROM address is $D000-$FFFF. The memory maps is shown in Figure 4.1.

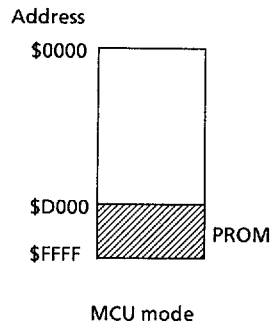


Figure 4.1 Memory Map

4.1 PROM PROGRAMMING

In MCU Mode, the PROM is programmed through the MCU in the bootstrap or test modes.

4.2 PROM PROGRAMMING USING THE MCU

Programming the OTPROM or EPROM through the MCU is only allowed in special test and bootstrap modes. With EPON bit the set, the various control bits of the PPROG register are manipulated to program the PROM locations. The erased state of a PROM byte is $FF.

4.2.1 PROM Programming Control Register (PPROG)

This register is used to control the programming of the OTPROM or EPROM. PPROG is cleared on reset so that the PROM is configured for normal read.

	7	6	5	4	3	2	1	0	
$103B	ODD	EVEN	ELAT	BYTE	ROW	ERASE	EELAT	PGM	PPROG
RESET:	0	0	0	0	0	0	0	0	

Bits 7, 6, 4, 3, 2, and 1 are used for EEPROM programming. For the details, see "3.5 EEPROM" in "2.4 TMP68HC11E9".

ELAT - EPROM (OTPROM) Latch Control

1 = PROM address and data bus are configured for programming. Writes to PROM cause address and data to be latched. The PROM cannot be read.

0 = PROM address and data bus configured for normal reads. PROM cannot be programmed.

PGM - EPROM (OTPROM) Program Command

This bit may be written only when ELAT = 1.

1 = Programming power switched on to PROM array.

0 = Programming power switched off.

4.2.2 PROM Programming Sequence

Before programming, ensure that V_{PP} voltage is available on the $\overline{XIRQ}$ pin.

Note that $\overline{XIRQ}$ must not become active (be brought low) during programming. This state would disrupt or corrupt the programming of the OTPROM or EPROM. The proper sequence for programming the PROM through the MCU (with EPON bit set in CONFIG) is as follows:

STEP	Comments
1. Write $20 to PPROG 2. Write data to PROM 3. Write $21 to PPROG 4. Delay 1 ms. 5. Write $20 to PPROG	Set ELAT bit (PGM = 0) to enable PROM latches. Store Data to PROM Address. Set PGM bit (ELAT = 1) to enable PROM high voltage. Turn off high voltage to PROM array.
6. Repeat steps 2 through 5, as needed.	
7. Write $00 to PPROG	Return to read mode.

4.2.3 Protecting the PROM

some precautions are necessary in order to protect the OTPROM or EPROM. For systems which do not make use of the on-chip programming capability, but program the TMP68C711J6 as a standard EPROM, voltage on the $\overline{XIRQ}/V_{PP}$ pin should never be permitted to be greater than V_{DD}. The PROM cannot be programmed or corrupted without high voltage on the $\overline{XIRQ}$ pin.

4.2.4 Erasing the PROM

OTPROM MCU devices are shipped in an erased state. Once programmed, they cannot be erased. Electrical erasing procedures cannot be performed on OTPROM device.

5. ELECTRICAL SPECIFICATIONS

This section contains the electrical specifications and associated timing information for the TMP68C711E9 MCU.

5.1 MAXIMUM RATINGS

Raing	Symbol	Value	Unit
Supply Voltage	V_{DD}	− 0.3 to + 7.0	V
Input Voltage	V_{in}	− 0.3 to + 7.0	V
Operating Temperature Range TMP68C711E9	T_a	T_L to T_H − 40 to 85	℃
Storage Temperature Range	T_{stg}	− 55 to 150	℃
Current Drain per Pin* Excluding V_{DD}, V_{SS}, V_{RH}, and V_{RL}	I_D	25	mA

* One pin at a time, observing maximum power dissipation limits.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields;however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

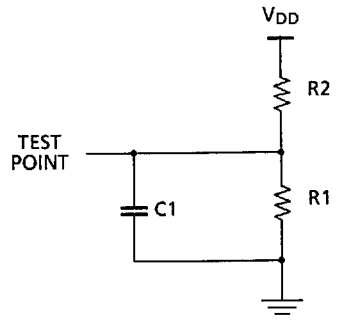
5.2 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H, unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Output Voltage I_{Load} = ± 10.0 μA (see Note 1)	All Outputs All Outputs Except $\overline{RESET}$ and MODA	VOL VOH	– V_{DD} – 0.1	0.1 –	V
Output High Voltage ILoad = -0.8mA, VDD = 4.5V (see Note 1)	All Outputs Except RESET, XTAL, and MODA	V_{OH}	V_{DD} – 0.8	–	V
Output Low Voltage I_{Load} = 1.6mA	All Outputs Except XTAL	V_{OL}	–	0.4	V
Input High Voltage	All Inputs Except $\overline{RESET}$ $\overline{RESET}$	V_{IH}	0.7 × V_{DD} 0.8 × V_{DD}	V_{DD} V_{DD}	V
Input Low Voltage	All Inputs	V_{IL}	V_{SS}	0.2 × V_{DD}	V
I/O Ports, Three-State Leakage $V_{in} = V_{IH}$ or V_{IL}	PA7, PA3, PC0-PC7, PD0-PD5, STRA/AS, MODA/$\overline{LIR}$, $\overline{RESET}$	I_{OZ}	–	± 10	μA
Input Current (see Note 2) $V_{in} = V_{DD}$ or V_{SS} $V_{in} = V_{DD}$ or V_{SS}	PA0-PA2, $\overline{IRQ}$ $\overline{XIRQ}$ MODB/V_{STBY}	I_{in}	– –	± 1 ± 10	μA
RAM Standby Voltage	Powerdown	V_{SB}	4.0	V_{DD}	V
RAM Standby Current	Powerdown	I_{SB}	–	20	μA
Total Supply Current(see Note 3) RUN: Single-Chip Mode Expanded Multiplexed Mode WAIT: All Peripheral Functions Shut Down Single-Chip Mode Expanded Multiplexed Mode STOP: No Clocks, Single-Chip Mode		I_{DD} W_{IDD} S_{IDD}	 – – – – –	 15 27 6 15 100	 mA mA mA mA μA
Input Capacitance PA7, PA3, PC0-PC7, PD0-PD5, STRA/AS, MODA/$\overline{LIR}$, $\overline{RESET}$	PA0-PA2, PE0-PE7, $\overline{IRQ}$, $\overline{XIRQ}$, $\overline{EXTAL}$	C_{in}	– –	8 12	pF
Power Dissipation	Single Chip Mode Expanded Multiplexed Mode	P_D	– –	85 150	mW
Program Power Supply Voltage		V_{PP}	12.0	13.0	V
Program Power Supply Current		I_{PP}	TBD	TBD	mA

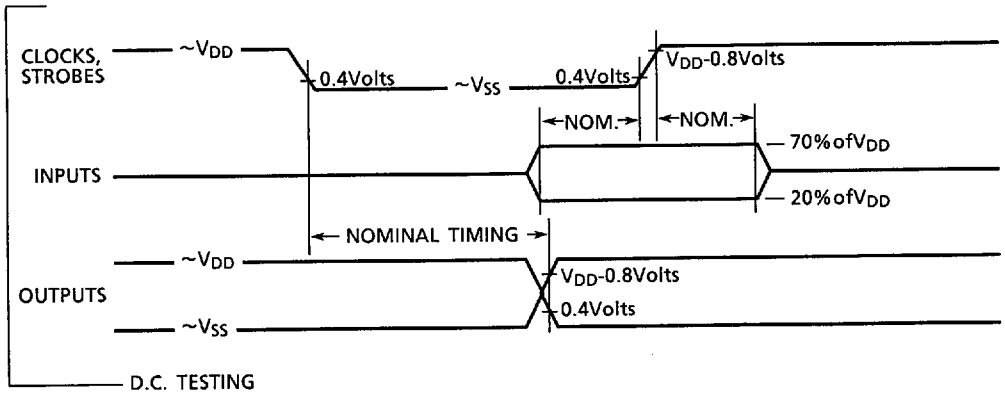
Notes:

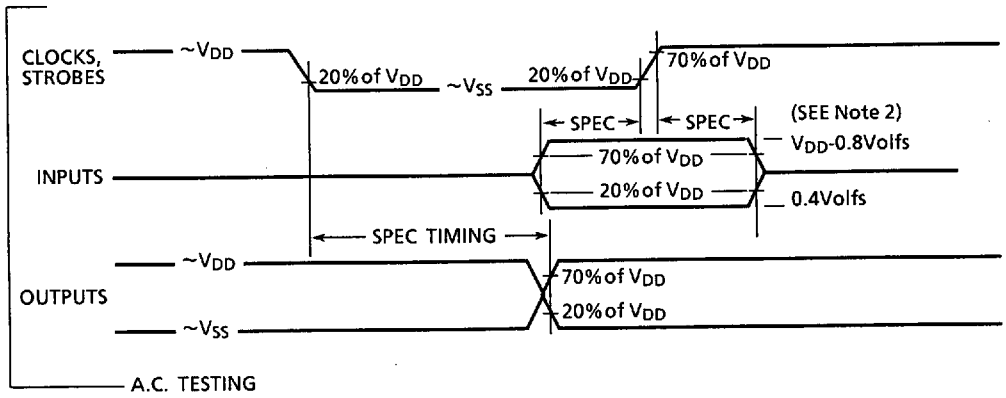
1. V_{OH} specification for $\overline{RESET}$ and MODA is not applicable because they are open-drain pins.
   V_{OH} specification not applicable to ports C and D in wire-OR mode.
2. See A/D specification for leakage current for port E.
3. All ports configured as inputs,
   $V_{IH} \geqq V_{DD} - 0.2$ V, $V_{IL} \leqq 0.2$ V, No DC loads
   EXTAL is driven with a square wave, and t_{cyc} = 476.5 ns.



Equivalent Test Load[1]

Pins	R1	R2	C
PA3-PA7 PB0-PB7 PC0-PC7 PD0, PD5 E, AS, R/$\overline{W}$	3.26kΩ	2.38kΩ	90pF
PD1-PD4	3.26kΩ	2.38kΩ	200pF





Notes:
1. Full test loads are applied during all DC electrical and AC timing measurements.
2. During ac timing measurements, inputs are driven to 0.4 volts and V_{DD}-0.8 volts while timing measurements are taken at the 20% and 70% of V_{DD} points.

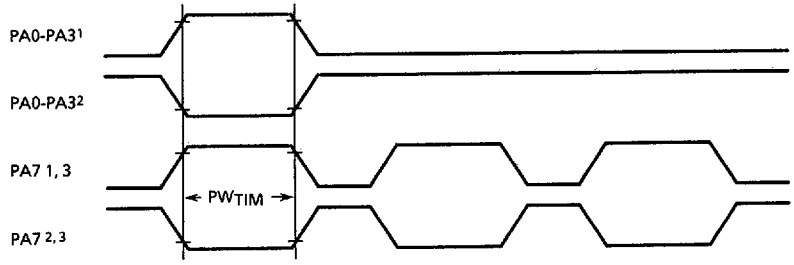
Figure 5.1 Test Methods

5.3 CONTROL TIMING (V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H)

Characteristic		Symbol	1.0MHz		2.0MHz		2.1MHz		Unit
			Min	Max	Min	Max	Min	Max	
Frequency of Operation		f_O	dc	1.0	dc	2.0	dc	2.1	MHz
E Clock Period		t_{cyc}	1000	–	500	–	476	–	ns
Crystal Frequency		f_{XTAL}	–	4.0	–	8.0	–	8.4	MHz
External Oscillator Frequency		$4f_O$	dc	4.0	dc	8.0	dc	8.4	MHz
Processor Control Setup Time(see Figures 5.3, 5.5, and 5.6)	$t_{PCS} = 1/4\ t_{cyc}$-50 ns	t_{PCS}	200	–	75	–	69	–	ns
Reset Input Pulse Width (see Note 1 and Figure 5.3)	(To Guarantee External Reset Vector)	PW_{RSTL}	8	–	8	–	8	–	t_{cyc}
	(Minimum Input Time; May be Preempted by Internal Reset)		1	–	1	–	1	–	
Mode Programming Setup Time (see Figure 5.3)		t_{MPS}	2	–	2	–	2	–	tcyc
Mode Programming Hold Time (see Figure 5.3)		t_{MPH}	0	–	0	–	0	–	ns
Interrupt Pulse Width, IRQ Edge Sensitive Mode (see Figures 5.4 and 5.6)	$PW_{IRQ} = t_{cyc} + 20$ ns	PW_{IRQ}	1020	–	520	–	496	–	ns
Wait Recovery Startup Time (See Figure 5.5)		t_{WRS}	–	4	–	4	–	4	tcyc
Timer Pulse Width Input Capture, Pulse Accumulator Input (see Figure 5.2)	$PW_{TIM} = t_{cyc} + 20$ ns	PW_{TIM}	1020	–	520	–	496	–	ns

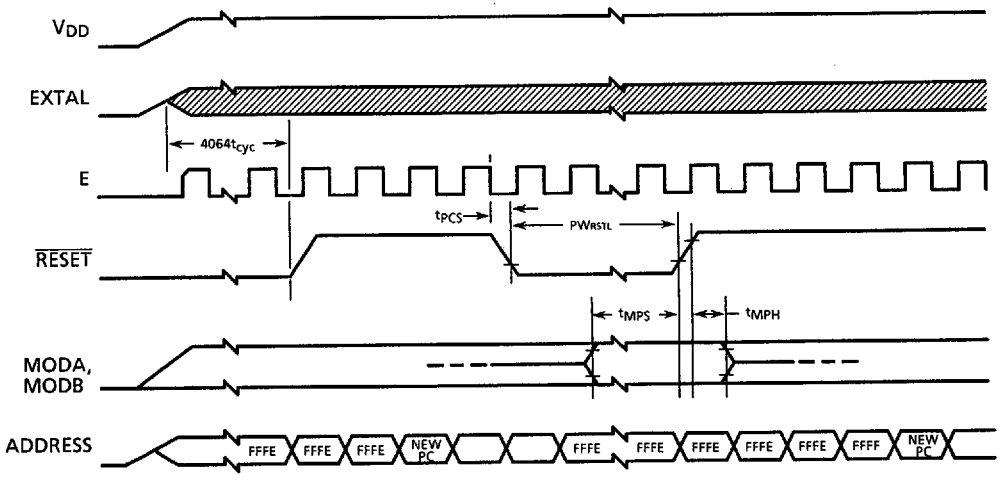
Note : 1. $\overline{\text{RESET}}$ will be recognized during the first clock cycle it is held low. Internal circuity then drives the pin low for four clock cycles, releases the pin, and samples the pin level two cycles later to detemine the source of the interrupt. See SECTION9 RESETS, INTERRUPT, AND LOW POWER MODES for details.

2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.



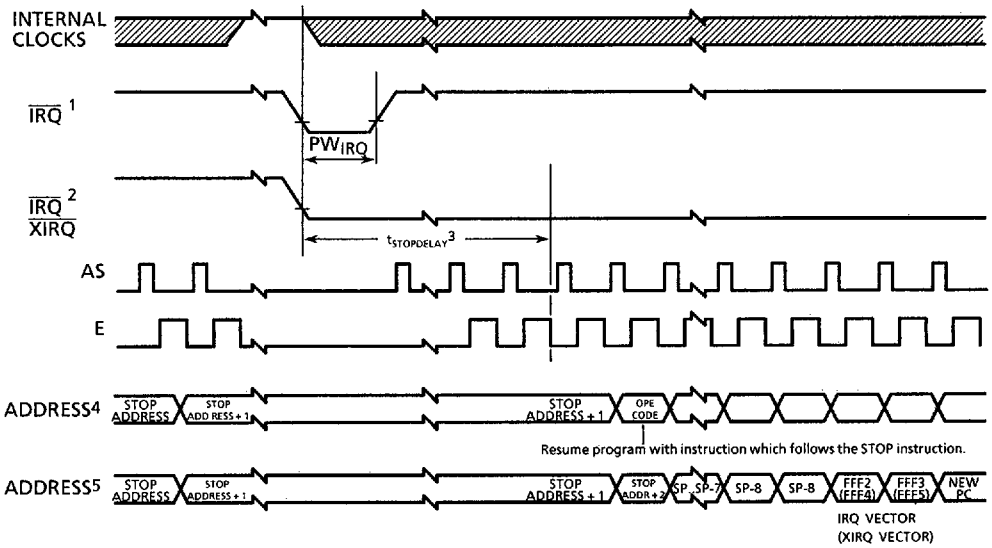
Notes :
1. Rising edge sensitive input
2. Falling edge sensitive input
3. Maximum pulse accumulator clocking rate is E frequency divided by 2.

Figure 5.2 Timer Inputs Timing Diagram



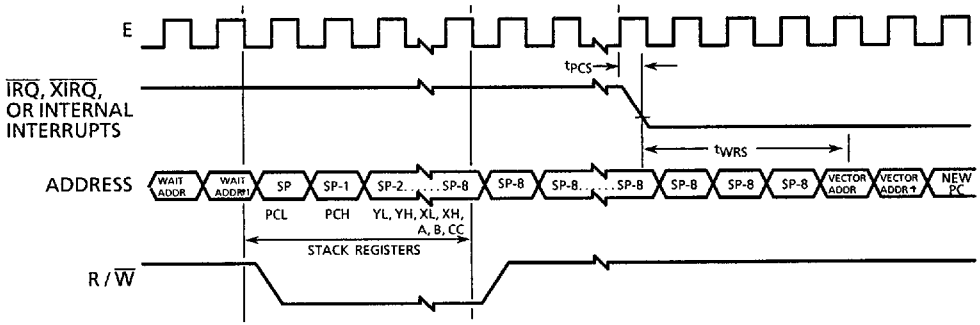
Note : Refer to Table 9.5 for pin states during $\overline{\text{RESET}}$

Figure 5.3 POR and External Reset Timing Diagram



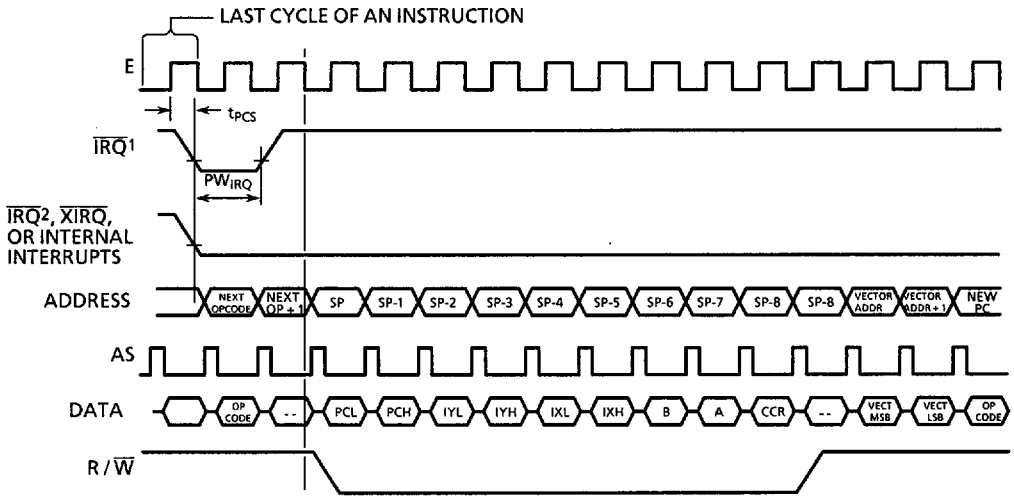
Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY} = 4064t_{cyc}$ if DLY bit = 1 or $4t_{cyc}$ if DLY = 0.
4. $\overline{XIRQ}$ with X bit CCR = 1 .
5. $\overline{IRQ}$, or ($\overline{XIRQ}$ with X bit in CCR = 0) .
6. Refer to Table 9.5 for pin states during STOP.

Figure 5.4 STOP Recovery Diagram



Notes :
1 Refer to Table 9.5 for pin states during WAIT.
2 $\overline{RESET}$ will also cause recovery from WAIT.

Figure 5.5 WAIT Recovery from Interrupt Timing Diagram



Notes :
1. Edge sensitive $\overline{IRQ}$ pin (IRQE bit = 1).
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0).

Figure 5.6 Interrupt Timing Diagram

5.4 PERIPHERAL PORT TIMING (V_{DD}=5.0 Vdc±10%,V_{SS}=0 Vdc,T_a=T_L to T_H)

Characteristic	Symbol	1.0MHz		2.0MHz		2.1MHz		Unit
		Min	Max	Min	Max	Min	Max	
E Clock Period	t_{cyc}	1000	–	500	–	476	–	ns
Peripheral Data Setup Time (MCU Read of Ports A,C,D, and E) (see Figure 5.8)	t_{PDSU}	100	–	100	–	100	–	ns
Peripheral Data Hole Time (MCU Read of Ports A,C,D, and E) (see Figure 5.8)	t_{PDH}	50	–	50	–	50	–	ns
Delay Time, Peripheral Data Write (see Figures 5.7, 5.9, 5.12, and 5.13)	t_{PWD}							ns
MCU Write to Port A		–	150	–	150	–	150	
MCU Writes to Ports B,C, and D t_{PWD} = 1/4t_{cyc} + 90 ns		–	340	–	215	–	209	
Input Data Setup Time(Port C) (see Figure 5.10 and 5.11)	t_{IS}	60	–	60	–	60	–	ns
Input Data Hold Time(Port C) (see Figure 5.10 and 5.11)	t_{IH}	100	–	100	–	100	–	ns
Delay Time, E Fall to STRB t_{DEB} = 1.4t_{cyc} + 100 ns (see Figures 5.9, 5.11, 5.12,and 5.13)	t_{DEB}	–	350	–	225	–	219	ns
Setup Time, STRA Asserted to E Fall(see Note 1) (see Figures 5.11, 5.12, and 5.13)	t_{AES}	0	–	0	–	0	–	ns
Delay Time, STRA Asserted to Port C Data Output Valid (see Figure 5.13)	t_{PCD}	–	100	–	100	–	100	ns
Hold Time, STRA Negated to Port C Data (see Figure 5.13)	t_{PCH}	10	–	10	–	10	–	ns
Three-State Hold Time (see Figure 5.13)	t_{PCZ}	–	150	–	150	–	150	ns

Notes :

1. If this setup time is met, STRB will acknowledge in the next cycle. If it is not met, the response may be delayed one more cycle.
2. Port C and D timing is valid for active drive (CWOM and DWOM bits not set in PIOC and SPCR registers respectively).
3. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless otherwise noted.

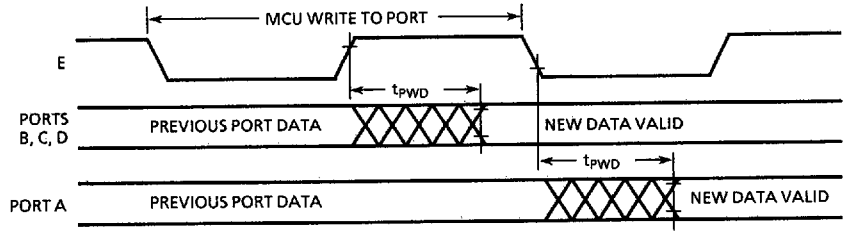
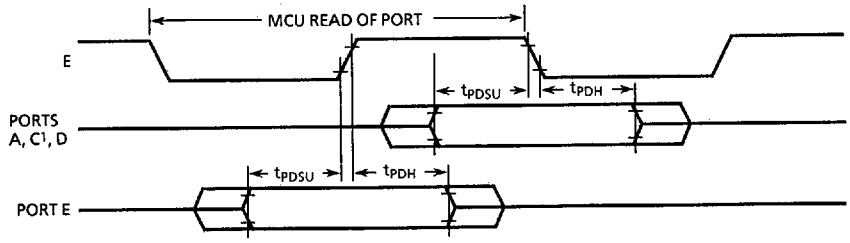


Figure 5.7 Port Write Timing Diagram



Note1 : For non-latched operation of Port C.

Figure 5.8 Port Read Timing Diagram

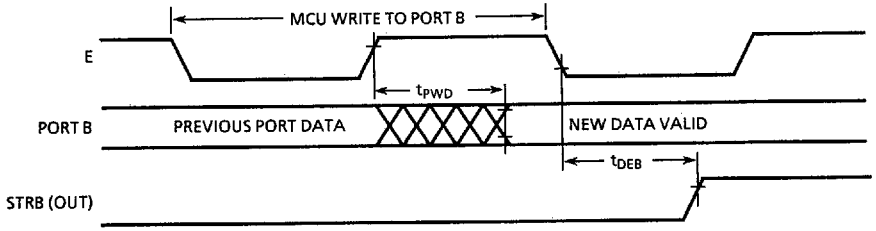


Figure 5.9 Simple Output Strobe Timing Diagram

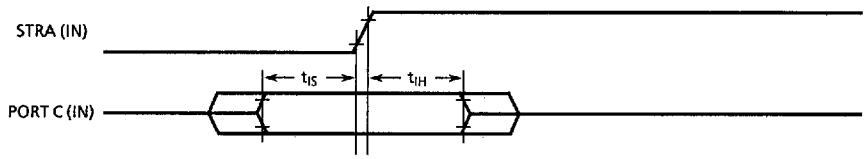
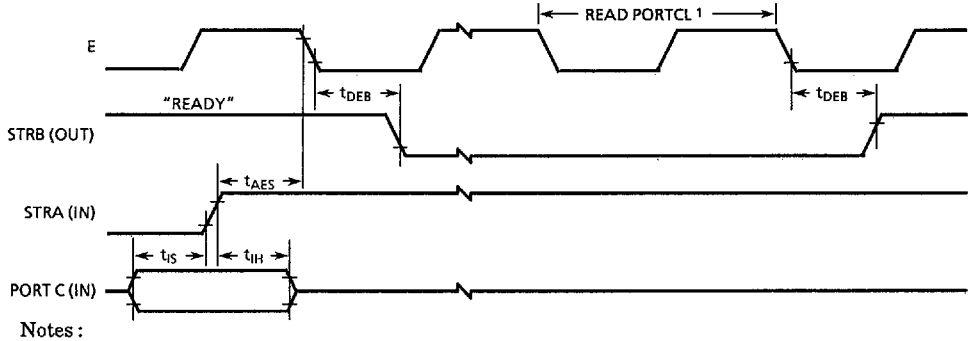
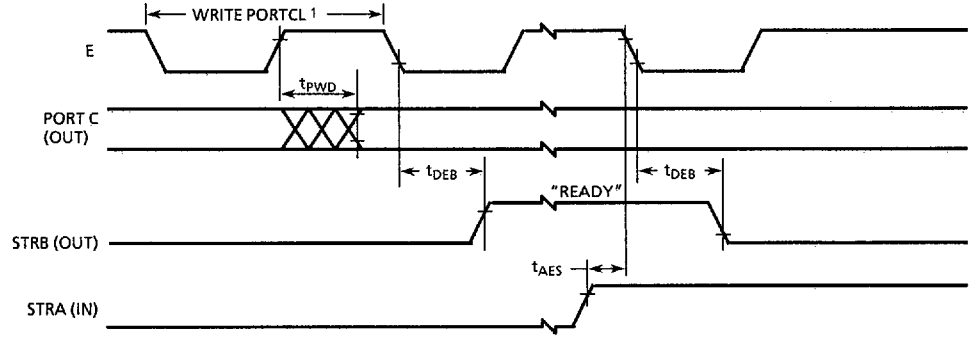


Figure 5.10 Simple Input Strobe Timing Diagram



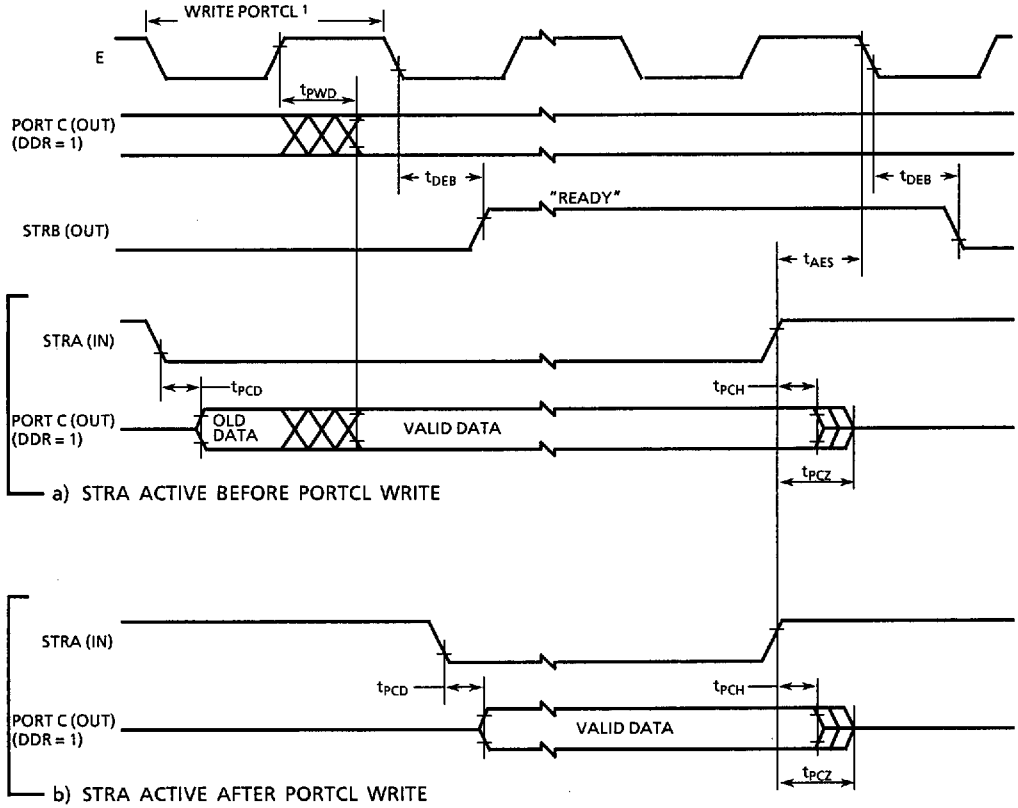
Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 5.11 Port C Input Handshake Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows rising edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 5.12 Port C Output Handshake Timing Diagram



Notes :
1. After reading PIOC with STAF set.
2. Figure shows edge STRA (EGA = 1) and high true STRB (INVB = 1)

Figure 5.13 Three-State Variation of Output Handshake Timing Diagram (STRA Enables Output Buffer)

5.5 A/D CONVERTER CHARACTERISTICS(VDD = 5.0 Vdc ± 10%, VSS = 0Vdc, Ta = TL to TH, 750kHz ≦ E ≦ 2.1MHz, unless otherwise noted)

Characteristic	Parameter	Min	Absolute	Max	Unit
Resolution	Number of Bits Resolved by the A/D	8	–	–	Bits
Non-Linearity	Maximum Deviation from the Ideal A/D Transfer Characteristics	–	–	± 1/2	LSB
Zero Error	Difference Between the Output of an Ideal and an Actual A/D for Zero Input Voltage	–	–	± 1/2	LSB
Full Scale Error	Difference Between the Output of an Ideal an Actual A/D for Full-Scale Input Voltage	–	–	± 1/2	LSB
Total Unadjusted Error	Maximum Sum of Non-Linearity, Zero Error, and Full-Scale Error	–	–	± 1/2	LSB
Quantization Error	Uncertainty Due to Converter Resolution	–	–	± 1/2	LSB
Absolute Accuracy	Difference Between the Actual Input Voltage and the Full-Scale Weighted Equivalent of the Binary Output Code, All Error Sources Included	–	–	± 1	LSB
Conversion Range	Analog Input Voltage Range	V_{RL}	–	V_{RH}	V
V_{RH}	Maximum Analog Reference Voltage (see Note 2)	V_{RL}	–	V_{DD} + 0.1	V
V_{RL}	Minimum Analog Reference Voltage (see Note 2)	V_{SS} – 0.1	–	V_{RH}	V
ΔV_R	Minimum Difference between V_{RH} and V_{RL} (see Note 2)	3	–	–	V
Conversion Time	Total Time to Perform a Single Analog-to-Digital Conversion: a. E Clock b. Internal RC Oscillator	– –	32 –	– tcyc + 32	tcyc μs
Monotonicity	Conversion Result Never Decreases with an Increase in Input Voltage and has no Missing Codes		Guaranteed		
Zero Input Reading	Conversion Result when $V_{in} = V_{RL}$	00	–	–	Hex
Full Scale Reading	Conversion Result when $V_{in} = V_{RH}$	–	–	FF	Hex
Sample Acquisition Time	Analog Input Acquisition Sampling Time: a. E Clock b. Internal RC Oscillator	– –	12 –	– 12	tcyc μs
Sample/Hold Capacitance	Input Capacitance during Sample PE0-PE7	–	20 (Typ)	–	pF
Input Leakage	Input Leakage on A/D Pins PE0-PE7 V_{RL}, V_{RH}	– –	– –	400 1.0	nA μA

Notes:

1. Source impedances greater than 10KΩ will adversely affect accuracy, due mainly to input leakage.
2. Performance verified down to 2.5V ΔV_R, but accuracy is tested and guaranteed at $\Delta V_R = 5V \pm 10\%$.

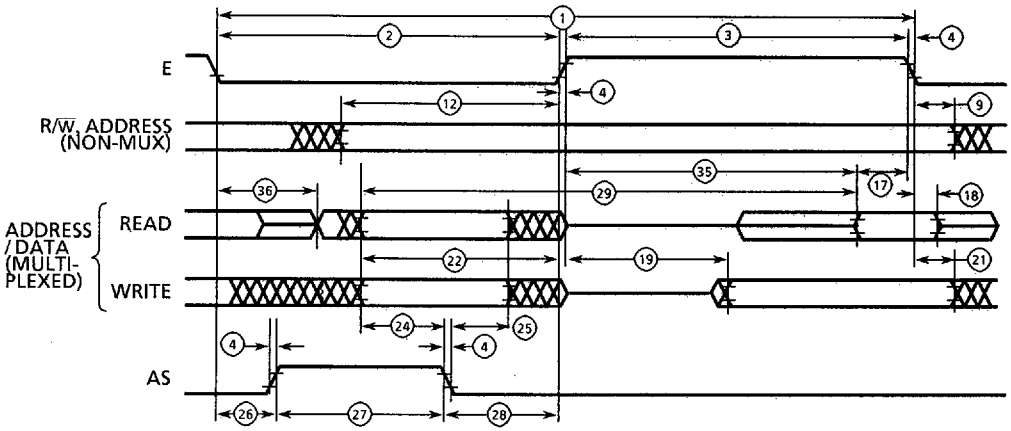
5.6 EXPANSION BUS TIMING

(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H, see Figure 5.14)

Num	Characteristic	Symbol	1.05MHz		2.0MHz		2.1MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1000	–	500	–	476	–	ns
2	PUlse Width, E Low $PW_{EL} = 1/2t_{cyc}$-23 ns	PW_{EL}	477	–	227	–	215	–	ns
3	PUlse Width, E High $PW_{EH} = 1/2t_{cyc}$-28 ns	PW_{EH}	472	–	222	–	210	–	ns
4	E and AS Rise and Fall Time	t_r, t_f	–	20	–	20	–	20	ns
9	Address Hold Time $t_{AV} = 1/8t_{cyc}$-29.5ns see Note 1(a)	t_{AH}	95.5	–	33	–	30	–	ns
12	Non-Muxed Address Valid Time to E Rise $t_{AV} = PW_{EL}-(t_{ASD} + 80$ ns) see Note 1(b)	t_{AV}	281.5	–	94	–	85	–	ns
17	Read Data Setup Time	t_{DSR}	30	–	30	–	30	–	ns
18	Read Data Hold Time(Max = t_{MAD})	t_{DHR}	10	145.5	10	83	10	80	ns
19	Write Data Delay Time $t_{DDW} = 1/8t_{cyc} + 65.5$ ns see Note 1(a)	t_{DDW}	–	190.5	–	128	–	125	ns
21	Write Data Hold Time $t_{DHW} = 1/8t_{cyc}$-29.5 ns see Note 1(a)	t_{DHW}	95.5	–	33	–	30	–	ns
22	Muxed Address Valid Time to E Rise $t_{AVM} = PW_{EL}-(t_{ASD} + 90$ ns) see Note 1(b)	t_{AVM}	271.5	–	84	–	75	–	ns
24	Muxed Address Valid Time to As Fall $t_{ASL} = PW_{ASH}$-70 ns	t_{ASL}	151	–	26	–	20	–	ns
25	Muxed Address Hold Time $t_{AHL} = 1/8\ t_{cyc}$-29.5 ns see Note 1(b)	t_{AHL}	95.5	–	33	–	30	–	ns
26	Delay Time,E to AS Rise $t_{ASD} = 1/8\ t_{cyc}$-9.5 ns see Note 1(a)	t_{ASD}	115.5	–	53	–	50	–	ns
27	Pulse Width, AS High $PW_{ASH} = 1/4t_{cyc}$-29 ns	PW_{ASH}	221	–	96	–	90	–	ns
28	Delay Time, AS to E Rise $t_{ASED} = 1/8t_{cyc}$-9.5 ns see Note 1(b)	t_{ASED}	115.5	–	53	–	50	–	ns
29	MPU Address Access Time $t_{ACCA} = t_{AVM} + t_r + PW_{EH}-t_{DSR}$ see note 1(b)	t_{ACCA}	733.5	–	296	–	275	–	ns
35	MPU Access Time $t_{ACCE} = PW_{EH}-t_{DSR}$	t_{ACCE}	–	442	–	192	–	180	ns
36	Muxed Address Delay (Previous Cycle MPU Read) $t_{MAD} = t_{ASD} + 30$ ns see Note 1(a)	t_{MAD}	145.5	–	83	–	80	–	ns

Notes :

1. Input clocks with duty cycles other than 50% will affect bus performance. Timing parameters affected by input clock duty cycle are identified by (a) and (b). To recalculate the approximate bus timing values, substitute the follwing expressions in place of 1/8 t_{cyc} in the above formulas where applicable:
   (a) (1-DC) × 1/4tcyc
   (b) DC × 1/4tcyc
   Where :
   DC is the decimal value of duty cycle percentage (high time)
2. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} unless othewise noted.



Note : Measurement point shown are 20% and 70% V_{DD}.

Figure 5.14 Expansion Bus Timing Diagram

5.7 SERIAL PERIPHERAL INTERFACE (SPI) TIMING

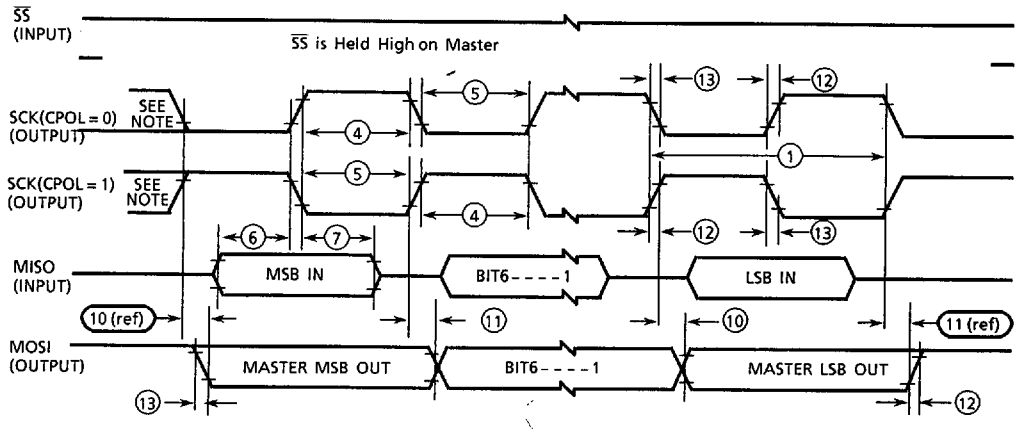
(V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_a = T_L$ to T_H, see Figure 5.15)

Num.	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency				
	Master	f_{OP} (m)	dc	1.05	MHz
	Slave	f_{OP} (s)	dc	2.1	MHz
1	Cycle Time				
	Master	t_{cyc} (m)	2.0	–	t_{cyc}
	Slave	t_{cyc} (s)	480	–	ns
2	Enable Lead Time				
	Master	t_{lead} (m)	*	–	ns
	Slave	t_{lead} (s)	240	–	ns
3	Enable Lag Time				
	Master	t_{lag} (m)	*	–	ns
	Slave	t_{lag} (s)	240	–	ns
4	Clock (SCK) High Time				
	Master	t_w (SCKH) $_m$	340	–	ns
	Slave	t_w (SCKH) $_s$	190	–	ns
5	Clock (SCK) Low Time				
	Master	t_w (SCKL) $_m$	340	–	ns
	Slave	t_w (SCKL) $_s$	190	–	ns
6	Data Setup Time (Inputs)				
	Master	t_{su} (m)	100	–	ns
	Slave	t_{su} (s)	100	–	ns
7	Data Hold Time (Inputs)				
	Master	t_h (m)	100	–	ns
	Slave	t_h (s)	100	–	ns
8	Access Time (Time to Data Active from High-Impedance State)				
	Slave	t_a	0	120	ns
9	Disable Time (Hold Time to High-Impedance State)				
	Slave	t_{dis}	–	240	ns
10	Data Valid (After Enable Edge)**	t_v (S)	–	240	ns
11	Data Hold Time (Outputs) (After Enable Edge)	t_{ho}	0	–	ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200pF)				
	SPI Outputs(SCK, MOSI, and MISO)	t_{rm}	–	100	ns
	SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	t_{rs}	–	2.0	μs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200pF)				
	SPI outputs(SCK, MOSI, and MISO)	t_{fm}	–	100	ns
	SPI Inputs(SCK, MOSI, MISO, and $\overline{SS}$)	t_{fs}	–	2.0	μs

*Signal production depends on software.

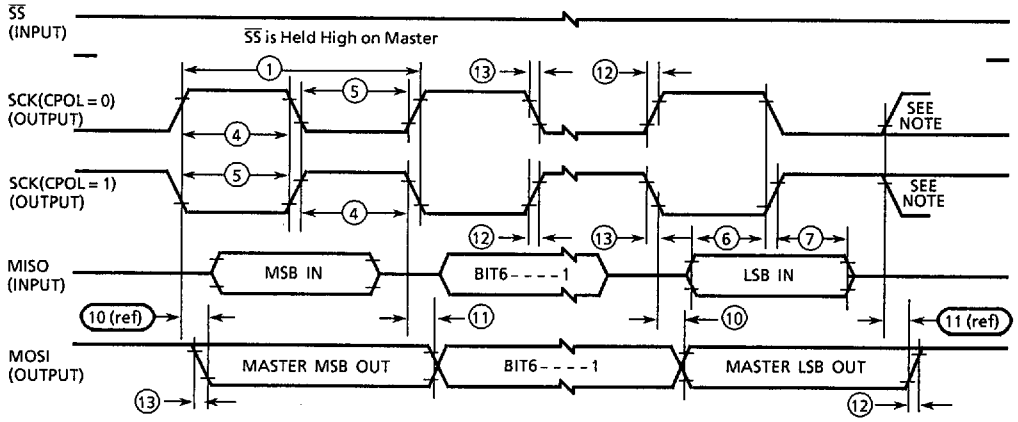
**Assumes 200 pF load on all SPI pins.

Note : All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.



Note : This first clock edge is generated internally but is not seen at the SCK pin.

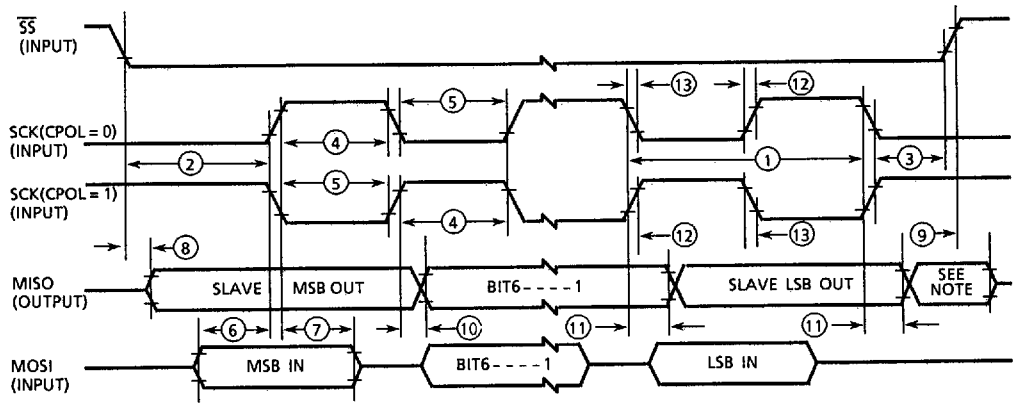
a) SPI MASTER TIMING (CPHA = 0)



Note : This last clock edge is generated internally but is not seen at the SCK pin.

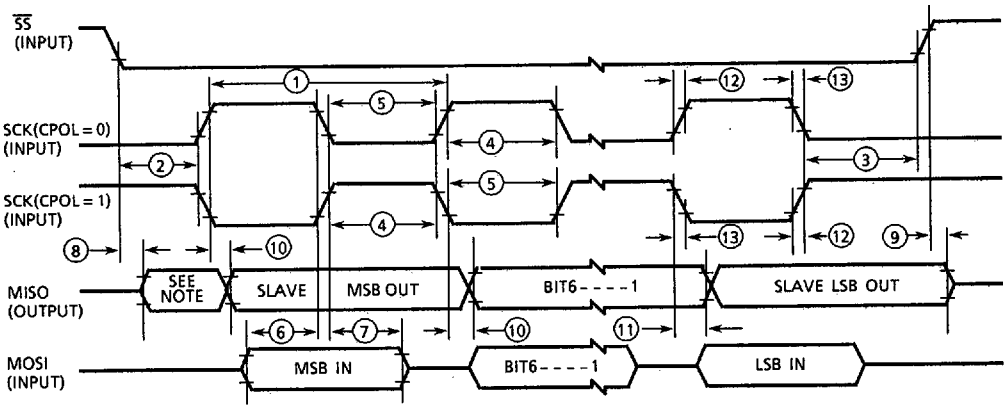
b) SPI MASTER TIMING (CPHA = 1)

Figure 5.15 SPI Timing Diagrams (Sheet 1 of 2)



Note : Not defined but normally MSB of character just received.

c) SPI SLAVE TIMING (CPHA = 0)



Note : Not defined but normally LSB of character previously transmitted.

d) SPI SLAVE TIMING (CPHA = 1)

Figure 5.15 SPI Timing Diagrams (Sheet 2 of 2)

5.8 EEPROM CHARACTERISTICS

(V_{DD}=5.0 Vdc±10%, V_{SS}=0 Vdc, T_a=T_L to T_H)

Characteristic	Temperature Range	Unit
	– 40 to 85°C	
Programming Time (See Note 1)		
Under 1.0 MHz with RC Oscillator Enable	10	ms
1.0 to 2.0 MHz with RC Oscillator Disabled	20	
2.0 MHz (or Anytime RC Oscillator Enabled)	10	
Erase Time (see Note 1) Byte, Row, and Bulk	10	ms
Write/Erase Endurance	10, 000	Cycles
Data Retention	10	Years

Notes:

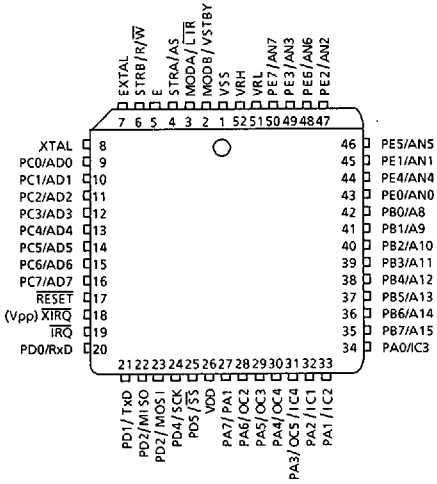
1. The RC oscillator must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0MHz.

6. PIN ASSIGNMENTS

6.1 PIN ASSIGNMENTS

The TMP68C711E9 is available in a 52-pin plastic lead chip carrier (PLCC) package. The following paragraph provide pin assignments.

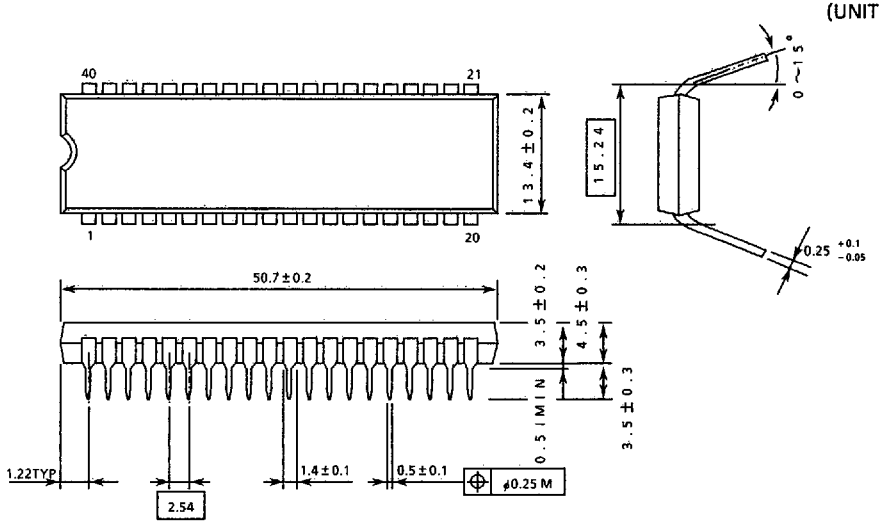
T SUFFIX
52 PIN PLCC



DIP40-P-600

P SUFFIX : 40PIN DIP (Dual Inline Package)

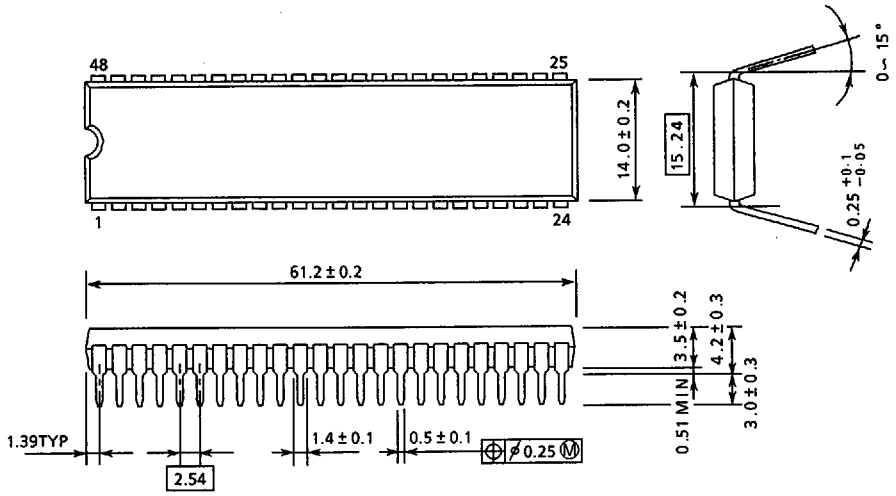
(UNIT : mm)



DIP48-P-600

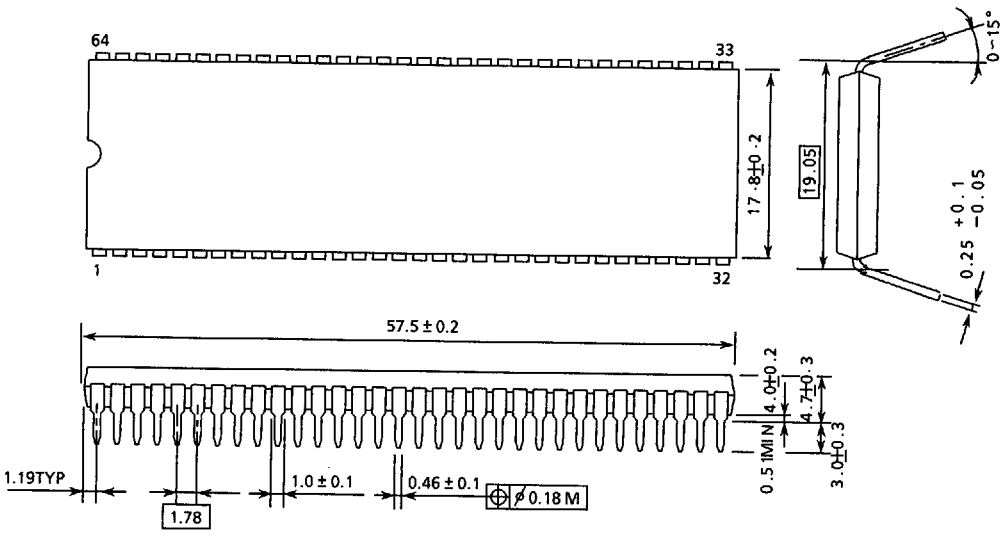
(UNIT : mm)

P SUFFIX : 48PIN DIP (Dual Inline Package)



SDIP64-P-750

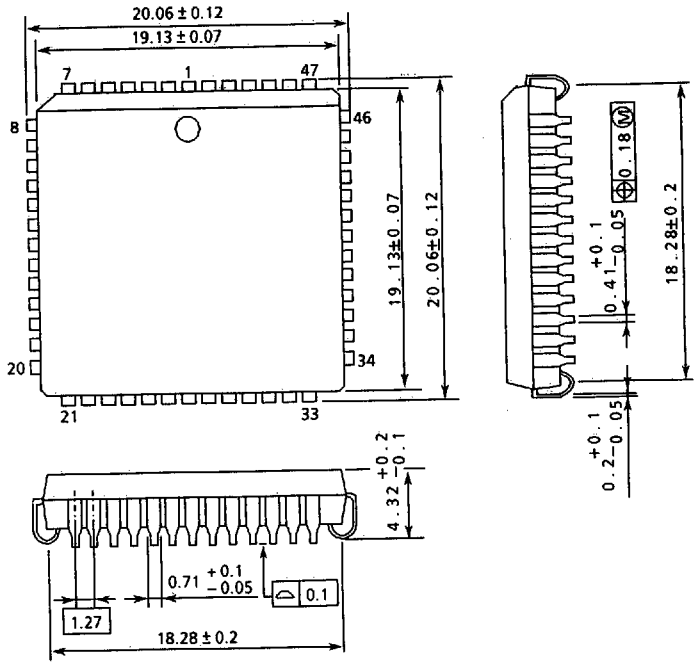
N SUFFIX : 64PIN SDIP (Shrink Dual Inline Package) (UNIT : mm)



QFJ52-P-S750

T SUFFIX : 52PIN QFJ (Quad Flat J-leaded Package) (PLCC)

(UNIT : mm)



F SUFFIX 64 PIN QFP (Quad Flat Package)

(UNIT : mm)