SGS-THOMSON MICROELECTRONICS

ST90E40
ST90T40

T-49-19-08

16K EPROM HCMOS MCUs WITH RAM AND EEPROM

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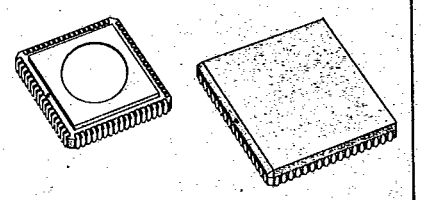
- Single chip microcontroller with 16K bytes of EPROM; 256 bytes of RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- 512 bytes of high-reliability EEPROM on-chip, with 300,000 erase/write cycle capability and 10 year data retention.
- On-chip programmable security protection against external reading of internal memory.
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I²C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Two 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Full function Serial Communications Interface with 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to seven 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases.
- 68-lead Ceramic Windowed package for ST90E40



CLCC68W PLCC68

(Ordering Information at the end of the datasheet)

Figure 1. ST90E40 Block Diagram

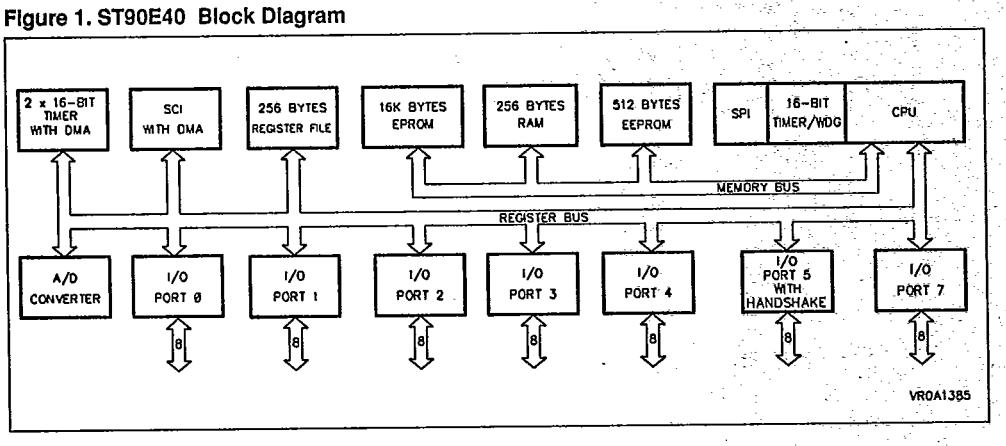


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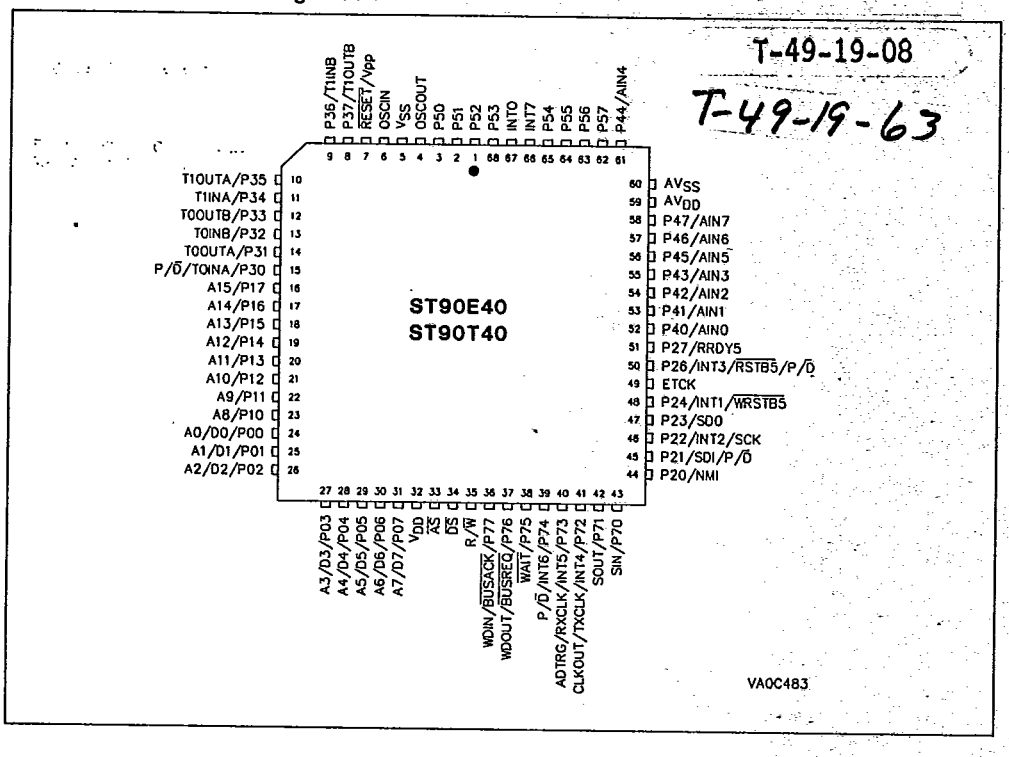
Figure 2. ST90E40 Pin Configuration



GENERAL DESCRIPTION

The ST90E40 and ST90T40 are EPROM members with EEPROM of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage up to 112K bytes of external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

A key point of the ST90E40 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I²C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E40 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

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R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90E40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. figure 1.2 shows the Functions allocated to each I/O Port pins.

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PIN DESCRIPTION (Continued)

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Table 1. ST90E40 I/O Port Alternate Function Summary

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I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31
P1.0	A8	O	Address bit 8	23
P1.1	A9	O	Address bit 9	22
P1.2	A10	O	Address bit 10	21
P1.3	A11	O	Address bit 11	20
P1.4	A12	O	Address bit 12	19
P1.5	A13	O	Address bit 13	18
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	16
P2.0	NMI	I	Non-Maskable Interrupt	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45
P2.1	SDI	I	SPI Serial Data Out	45
P2.2	INT2	I	External Interrupt 2	46
P2.2	SCK	O	SPI Serial Clock	46
P2.3	SDO	O	SPI Serial Data In	47
P2.4	INT1	I	External Interrupt 1	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	48
P2.5	WRRDY5	I	Handshake Write Ready P5	49
P2.6	INT3	I	External Interrupt 3	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50

Table 1. ST90E40 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P2.6	P/D	O	Program/Data Space Select	50
P2.7	RDRDY5	O	Handshake Read Ready P5	51
P3.0	T0INA	I	MF Timer 0 Input A	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15
P3.1	T0OUTA	O	MF Timer 0 Output A	14
P3.2	T0INB	I	MF Timer 0 Input B	13
P3.3	T0OUTB	O	MF Timer 0 Output B	12
P3.4	T1INA	I	MF Timer 1 Input A	11
P3.5	T1OUTA	O	MF Timer 1 Output A	10
P3.6	T1INB	I	MF Timer 1 Input B	9
P3.7	T1OUTB	O	MF Timer 1 Output B	8
P4.0	AIN0	I	A/D Analog Input 0	52
P4.1	AIN1	I	A/D Analog Input 1	53
P4.2	AIN2	I	A/D Analog Input 2	54
P4.3	AIN3	I	A/D Analog Input 3	55
P4.4	AIN4	I	A/D Analog Input 4	61
P4.5	AIN5	I	A/D Analog Input 5	56
P4.6	AIN6	I	A/D Analog Input 6	57
P4.7	AIN7	I	A/D Analog Input 7	58
P5.0		I/O	I/O Handshake Port 5	3
P5.1		I/O	I/O Handshake Port 5	2
P5.2		I/O	I/O Handshake Port 5	1
P5.3		I/O	I/O Handshake Port 5	68
P5.4		I/O	I/O Handshake Port 5	65
P5.5		I/O	I/O Handshake Port 5	64
P5.6		I/O	I/O Handshake Port 5	63
P5.7		I/O	I/O Handshake Port 5	62

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PIN DESCRIPTION (Continued)

Table 1. ST90E40 I/O Port Alternate Function Summary (Continued) T-49-19-63

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin Number
P7.0	SIN	I	SCI Serial Input	43
P7.1	SOUT	O	SCI Serial Output	42
P7.2	INT4	I	External Interrupt 4	41
P7.2	TXCLK	I	SCI Transmit Clock Input	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41
P7.3	INT5	I	External Interrupt 5	40
P7.3	RXCLK	I	SCI Receive Clock Input	40
P7.3	ADTRG	I	A/D Conversion Trigger	40
P7.4	INT6	I	External Interrupt 6	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39
P7.5	$\overline{WAIT}$	I	External Wait Input	38
P7.6	WDOUT	O	T/WD Output	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37
P7.7	WDIN	I	T/WD Input	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36

MEMORY

The memory of the ST90E40 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E40 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T40 OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E40 executes external memory cycles for instruction fetches. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

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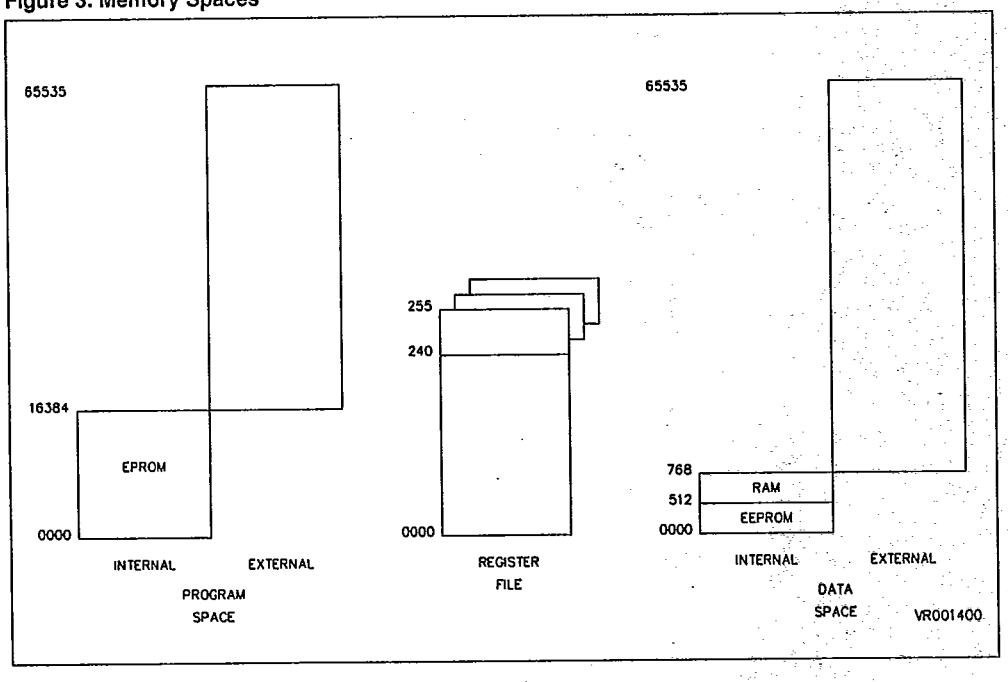
EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E40 (16320 for the ST90T40) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

Figure 3. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

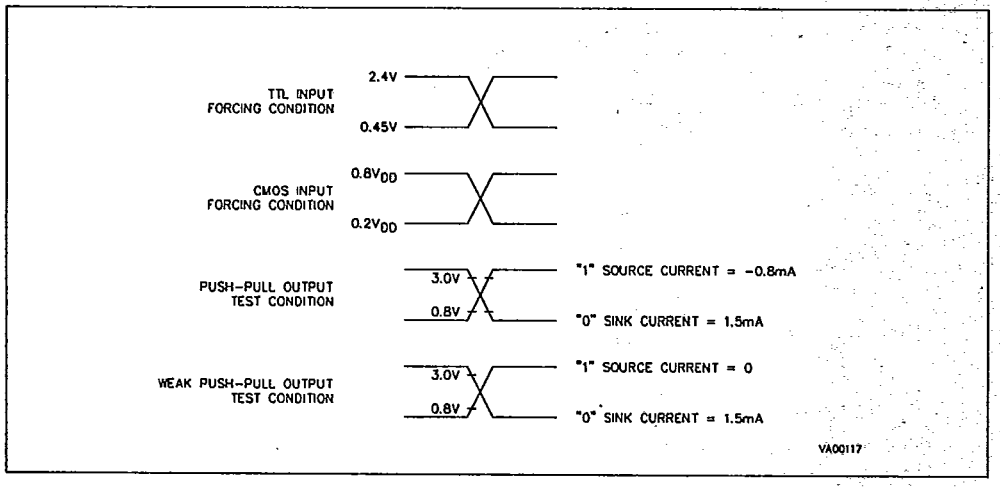
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	−80	−200	−420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	−10		+10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	−30		+30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	−3		+3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	−10		+10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	−10		+10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



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AC ELECTRICAL CHARACTERISTICS

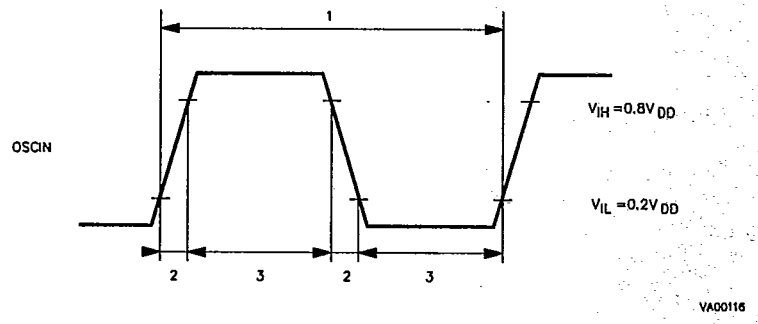
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

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N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

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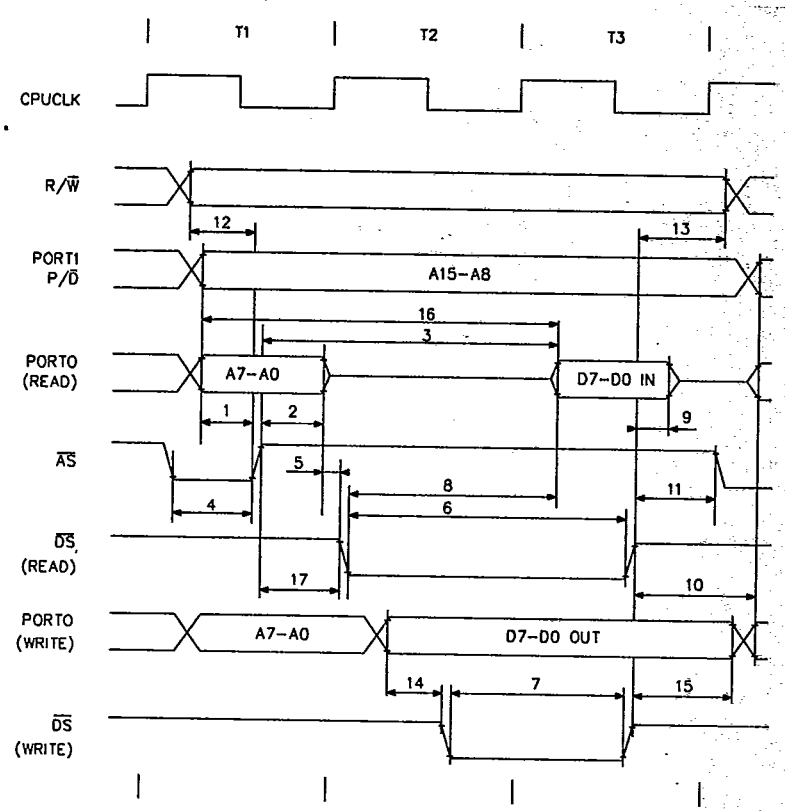

EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

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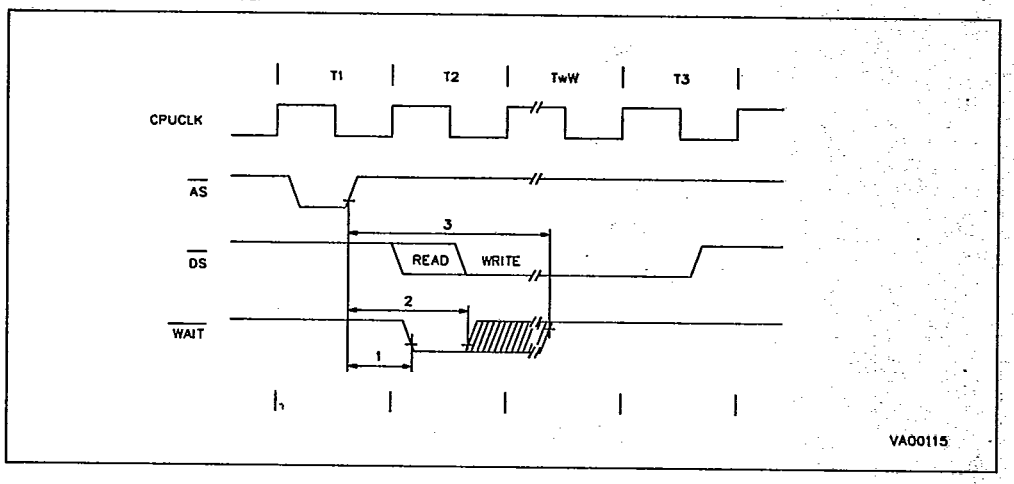
N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	(P+1)TpC –29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC –4	(P+W+1)TpC –4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC –29	(P+W+1)TpC –29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING



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BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

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N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

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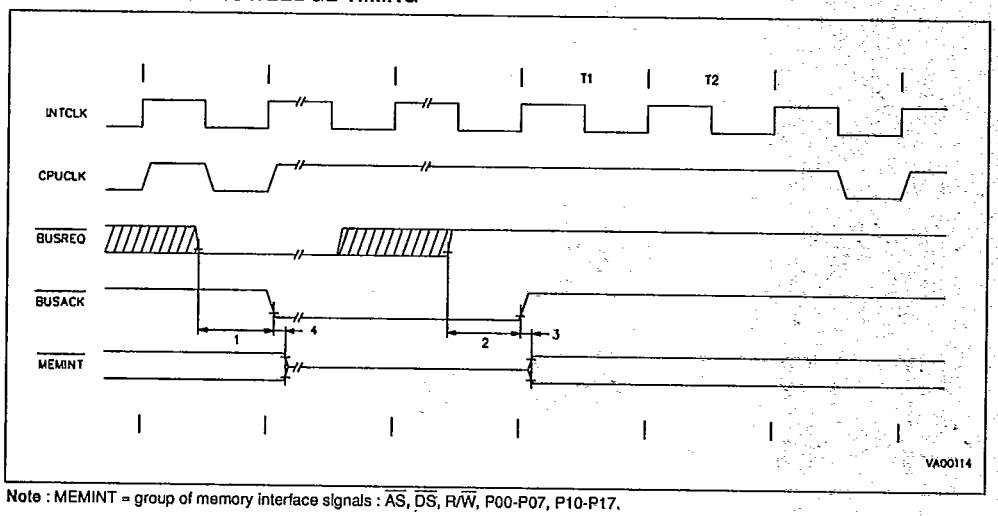
BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

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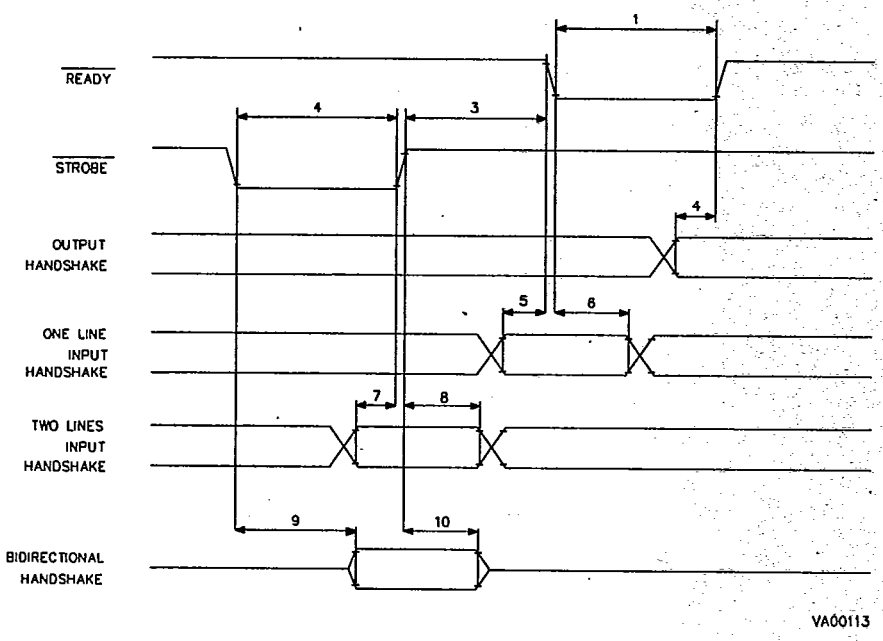
N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) –18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+(W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Hand-shake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Hand-shake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING



EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period; prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

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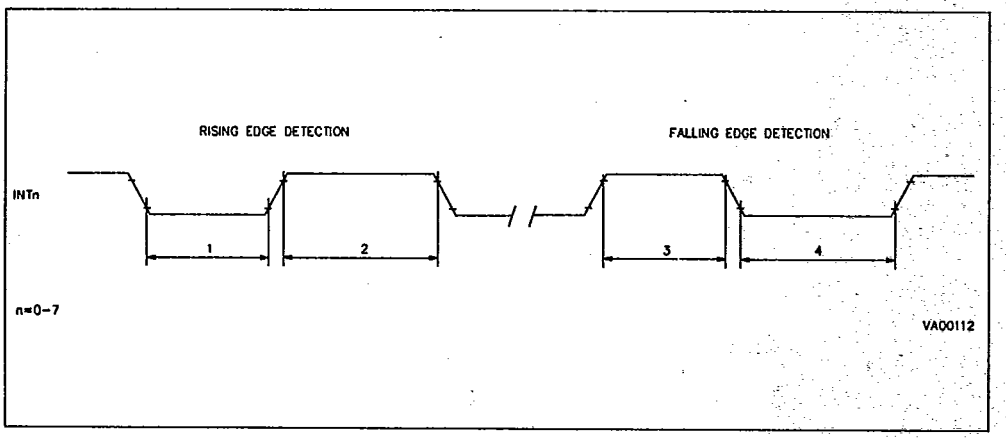
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50nF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

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N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

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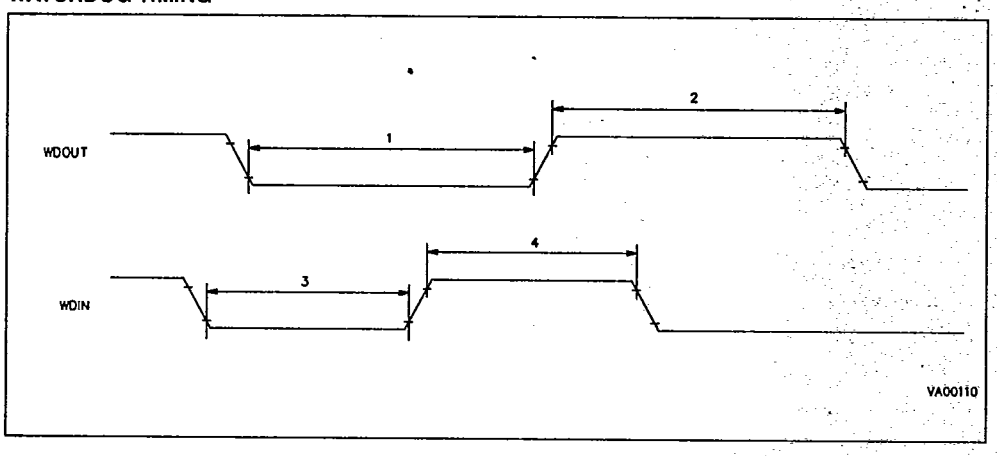
WATCHDOG TIMING



SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

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N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

Note: 1. TpC is the Clock period.

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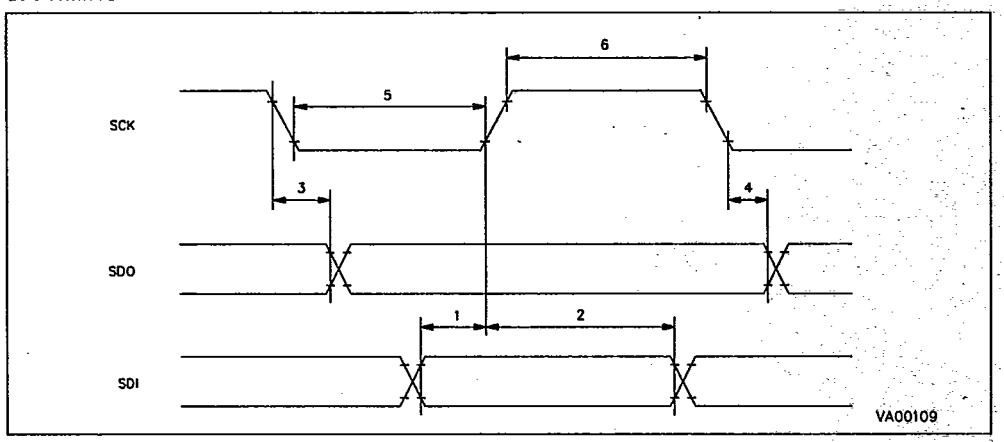
SPI TIMING



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PACKAGES MECHANICAL DATA

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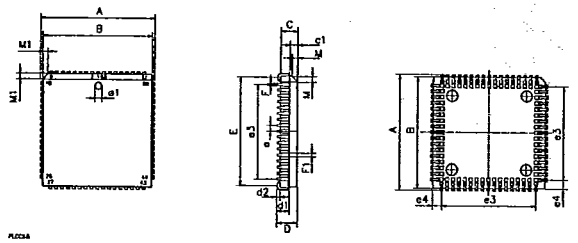
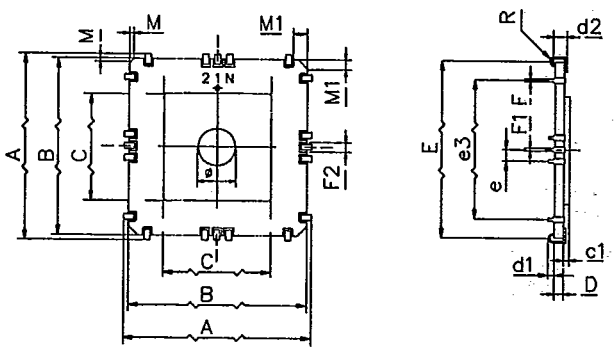
Figure 5. 68-Lead Plastic Leaded Chip Carrier (C)



Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.20		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.10			0.004
M		1.27			0.050	
M1		1.14			0.044	
Ø1		7.36			0.289	

Figure 6. 68-Lead Window Ceramic Leaded Chip Carrier (L)



Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A		25.14			0.989	
B	23.87		24.51	0.939		0.964
C			15.45			0.608
C1			1.30			0.051
D	1.82		2.23	0.071		0.087
d1	–	–	–	–	–	–
d2	–	–	–	–	–	–
E	–	–	–	–	–	–
e		1.27			0.050	
e3	–	–	–	–	–	–
F		0.45			0.017	
F1		0.63			0.025	
F2	–	–	–	–	–	–
M	–	–	–	–	–	–
M1	–	–	–	–	–	–
R		0.76			0.030	
Ø		8.89			0.350	

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ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E40L6	24MHz	– 40°C to + 85°C	CLCC68-W
ST90E40L1	24MHz	0°C to + 85°C	CLCC68-W
ST90T40C6	24MHz	– 40°C to + 85°C	PLCC68
ST90T40C1	24MHz	0°C to + 70°C	PLCC68

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