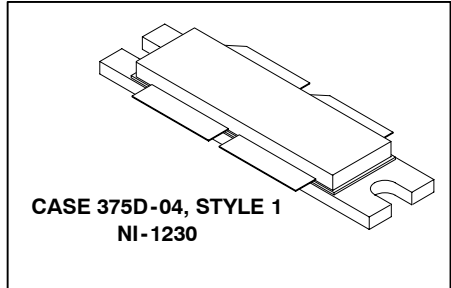


The RF Sub-Micron MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET

MRF21120R6

**2170 MHz, 120 W, 28 V
 LATERAL N-CHANNEL
 RF POWER MOSFET**



Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- W-CDMA Performance @ -45 dBc, 5 MHz Offset, 15 DTCH, 1 Perch
 Output Power — 14 Watts (Avg.)
 Power Gain — 11.5 dB
 Efficiency — 16%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2170 MHz, 120 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	389 2.22	Watts W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Operating Junction Temperature	T _J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.45	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 20 μAdc)	V _{(BR)DSS}	65	—	—	Vdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
ON CHARACTERISTICS (1)					
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 2 Adc)	g _{fs}	—	4.8	—	S
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 200 μA)	V _{GS(th)}	2.5	3	3.8	Vdc
Gate Quiescent Voltage (V _{DS} = 28 V, I _D = 500 mA)	V _{GS(Q)}	3	3.9	5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 V, I _D = 2 A)	V _{DS(on)}	—	0.38	0.5	Vdc
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	—	2.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)					
Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	G _{ps}	10.5	11.4	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	η	30	34.5	—	%
Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IMD	—	-31	-28	dB
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz, f ₂ = 2170.1 MHz)	IRL	—	-12	-9	dB
Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2140.0 MHz, f ₂ = 2140.1 MHz)	G _{ps}	—	11.5	—	dB
Common-Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	G _{ps}	—	11.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	η	—	34.5	—	%
Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	IMD	—	-31	—	dB
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 120 W PEP, I _{DQ} = 2 × 500 mA, f ₁ = 2110.0 MHz, f ₂ = 2110.1 MHz)	IRL	—	-12	—	dB
Power Output, 1 dB Compression Point (V _{DD} = 28 Vdc, CW, I _{DQ} = 2 × 500 mA, f ₁ = 2170.0 MHz)	P _{1dB}	—	120	—	Watts

(1) Each side of device measured separately.

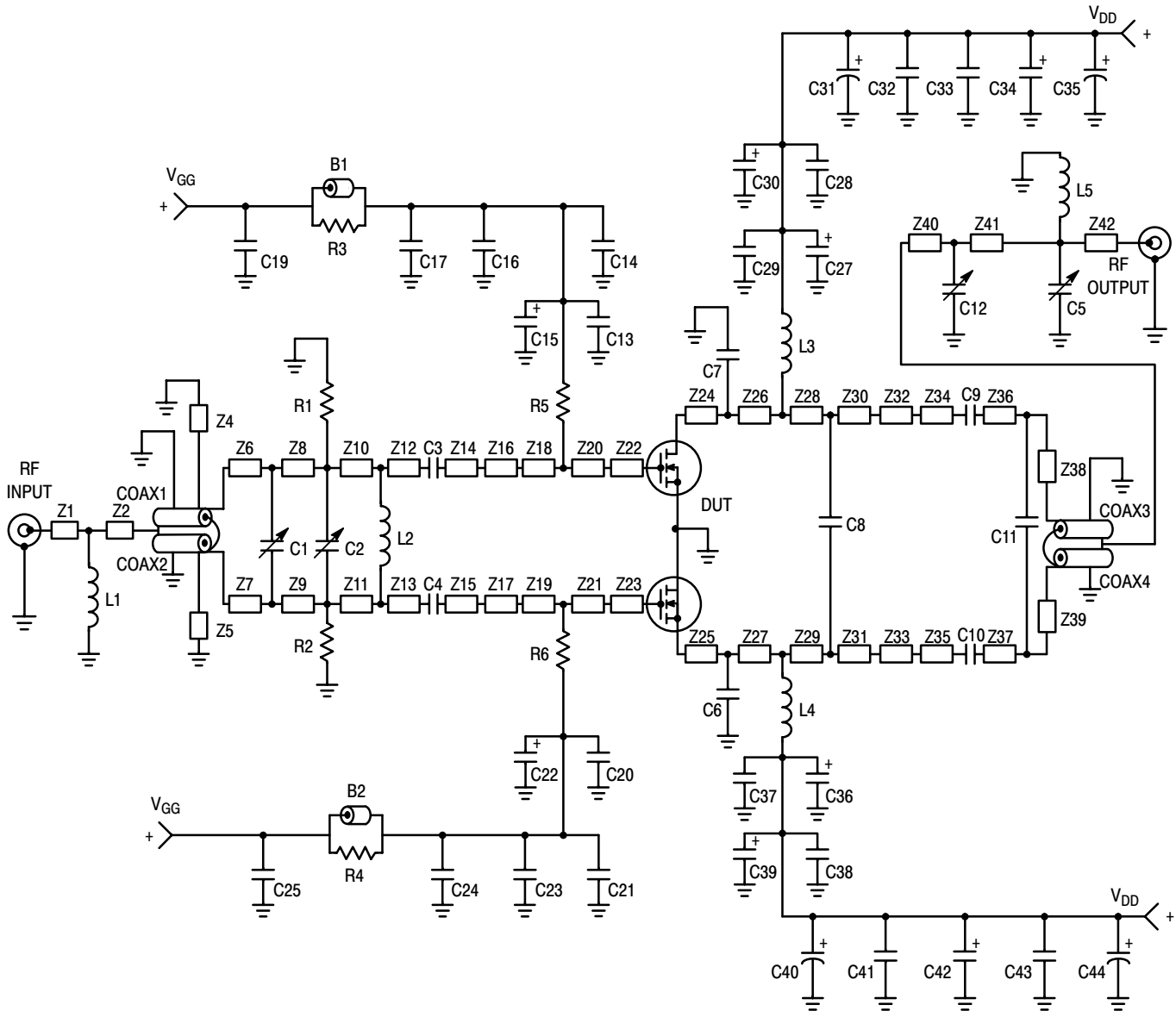
(2) Device measured in push-pull configuration.

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ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2) (continued)					
Common-Source Amplifier Power Gain ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 120 \text{ W CW}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $f_1 = 2170.0 \text{ MHz}$)	G_{ps}	—	10.5	—	dB
Drain Efficiency ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 120 \text{ W CW}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $f_1 = 2170.0 \text{ MHz}$)	η	—	42	—	%
Output Mismatch Stress ($V_{DD} = 28 \text{ Vdc}$, $P_{out} = 120 \text{ W CW}$, $I_{DQ} = 2 \times 500 \text{ mA}$, $f = 2.17 \text{ GHz}$, $VSWR = 10:1$, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(2) Device measured in push-pull configuration.



B1, B2	Ferrite Beads, Fair Rite	Z2	0.320" x 0.080" Microstrip
C1, C2, C12	0.6 - 4.5 pF Variable Capacitors, Johanson Gigatrim	Z4, Z5	1.050" x 0.080" Microstrip
C3, C4, C9, C10	10 pF Chip Capacitors, B Case, ATC	Z6, Z7	0.120" x 0.080" Microstrip
C5	0.4 - 2.5 pF Variable Capacitor, Johanson Gigatrim	Z8, Z9	0.140" x 0.080" Microstrip
C6, C7	2.0 pF Chip Capacitors, B Case, ATC	Z10, Z11	0.610" x 0.080" Microstrip
C8	0.5 pF Chip Capacitor, B Case, ATC	Z12, Z13	0.135" x 0.080" Microstrip
C11	0.2 pF Chip Capacitor, B Case, ATC	Z14, Z15	0.130" x 0.080" Microstrip
C13, C20, C29, C37	5.1 pF Chip Capacitors, B Case, ATC	Z16, Z17	0.300" x 0.350" Microstrip
C14, C21, C28, C38	91 pF Chip Capacitors, B Case, ATC	Z18, Z19	0.150" x 0.500" Microstrip
C15, C22, C27, C34, C36, C42	22 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet	Z20, Z21	0.075" x 0.500" Microstrip
C16, C23, C33, C43	0.039 μF Chip Capacitors, B Case, ATC	Z22, Z23	0.330" x 0.500" Microstrip
C17, C24, C32, C41	1000 pF Chip Capacitors, B Case, ATC	Z24, Z25	0.100" x 0.550" Microstrip
C19, C25	0.022 μF Chip Capacitors, B Case, ATC	Z26, Z27	0.175" x 0.550" Microstrip
C30, C39	1.0 μF, 35 V Tantalum Surface Mount Chip Capacitors, Kemet	Z28, Z29	0.045" x 0.550" Microstrip
C31, C40	100 μF, 50 V Electrolytic Capacitors, Sprague	Z30, Z31	0.190" x 0.325" Microstrip
C35, C44	470 μF, 63 V Electrolytic Capacitors, Sprague	Z32, Z33	0.080" x 0.325" Microstrip
Coax1, Coax2	25 Ω Semi Rigid Coax, 70 mil OD, 1.05" Long	Z34, Z35	0.515" x 0.080" Microstrip
Coax3, Coax4	50 Ω Semi Rigid Coax, 85 mil OD, 1.05" Long	Z36, Z37	0.020" x 0.080" Microstrip
L1, L5	5.0 nH Minispring Inductors, Coilcraft	Z38, Z39	0.565" x 0.080" Microstrip
L2	8.0 nH Minispring Inductor, Coilcraft	Z40	0.100" x 0.080" Microstrip
L3, L4	7.15 nH Minispring Inductors, Coilcraft	Z41	0.470" x 0.080" Microstrip
R1, R2	1 kΩ, 1/4 W Fixed Metal Film Resistors, Dale	Z42	0.100" x 0.080" Microstrip
R3, R4	270 Ω, 1/8 W Fixed Film Chip Resistors, Dale		Board Material
R5, R6	1.2 kΩ, 1/8 W Fixed Film Chip Resistors, Dale		0.03" Teflon®, ε _r = 2.55 Copper Clad, 2 oz. Cu
Z1	0.150" x 0.080" Microstrip	Connectors	N-Type Panel Mount, Stripline

Figure 1. 2.1 - 2.2 GHz Broadband Test Circuit Schematic

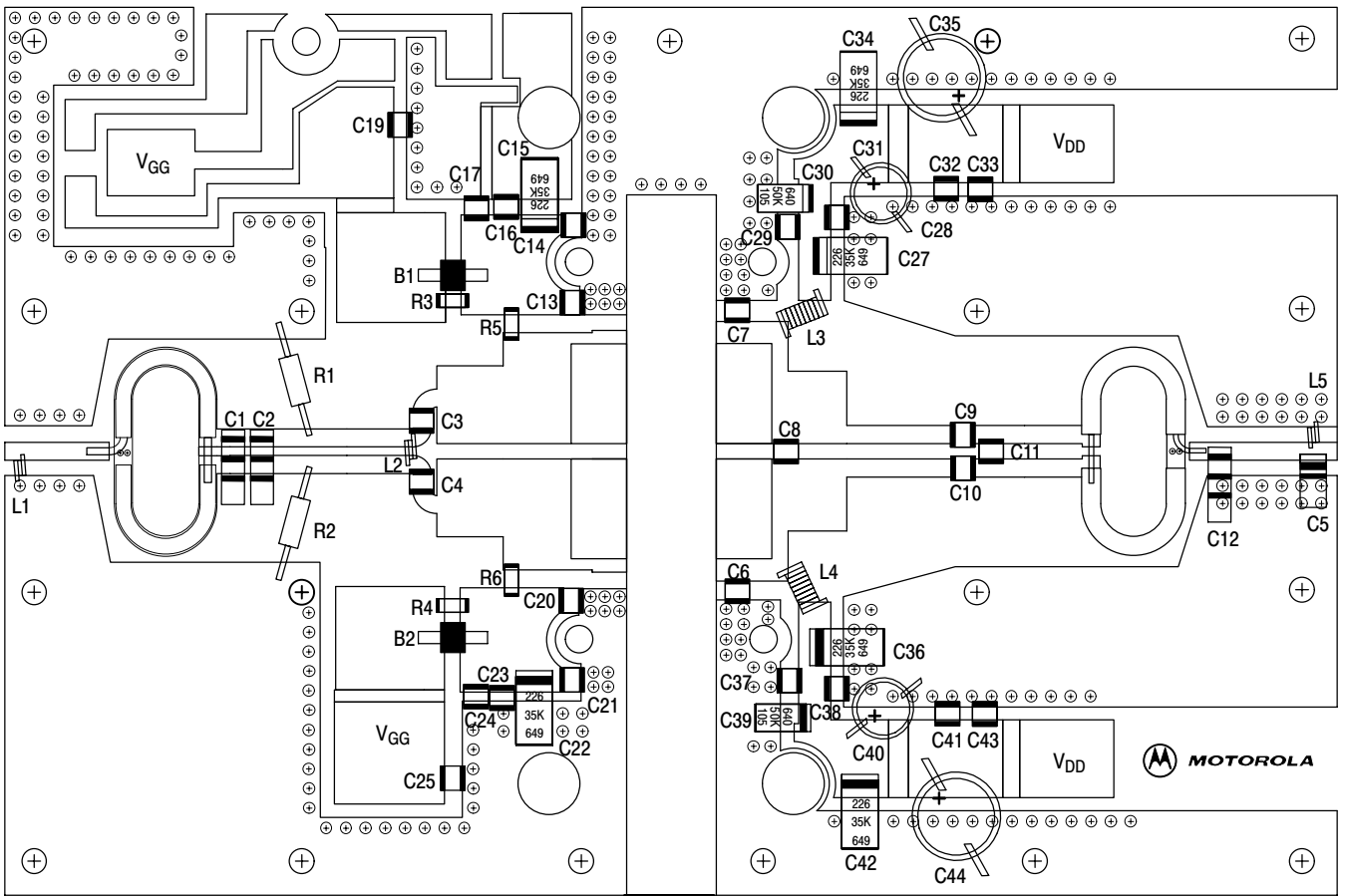


Figure 2. 2.1 - 2.2 GHz Broadband Test Circuit Component Layout

TYPICAL CHARACTERISTICS

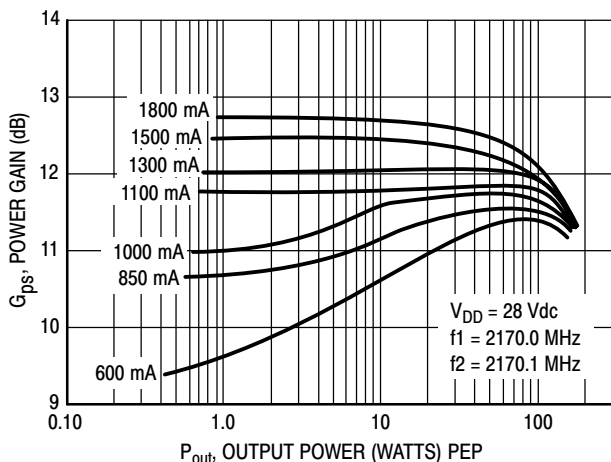


Figure 3. Power Gain versus Output Power

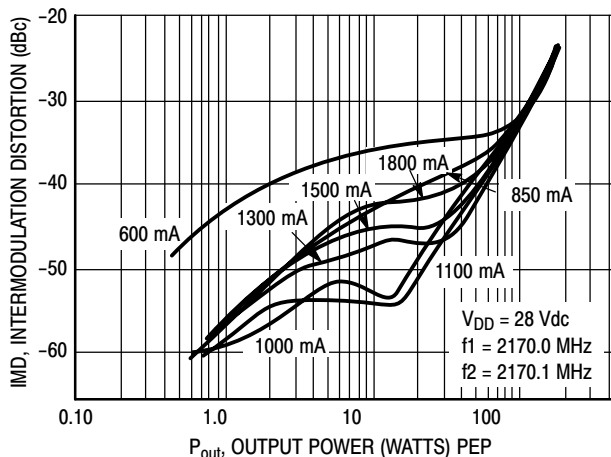


Figure 4. Intermodulation Distortion versus Output Power

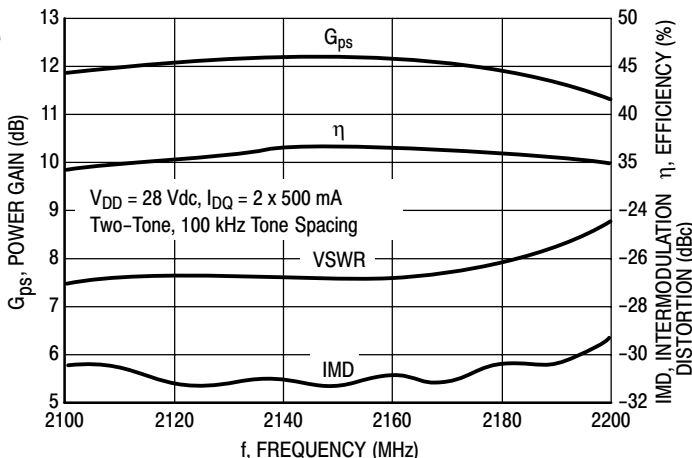


Figure 5. Class AB Broadband Circuit Performance

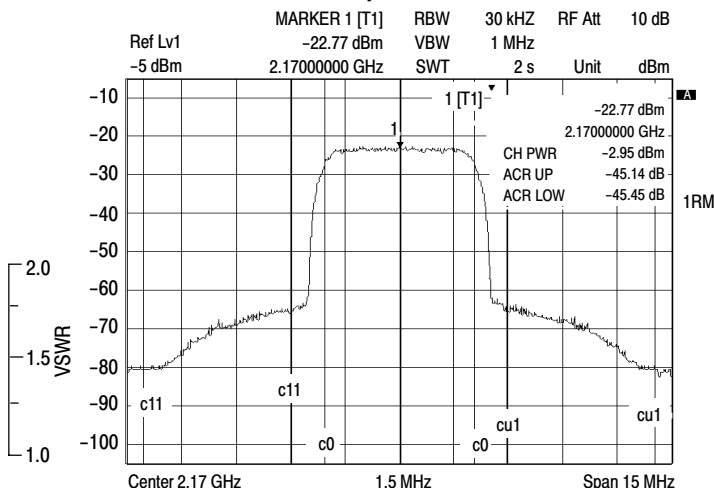


Figure 6. 2.17 GHz W-CDMA Mask at 14 Watts (Avg.), 5 MHz Offset, 15 DTCH, 1 Perch

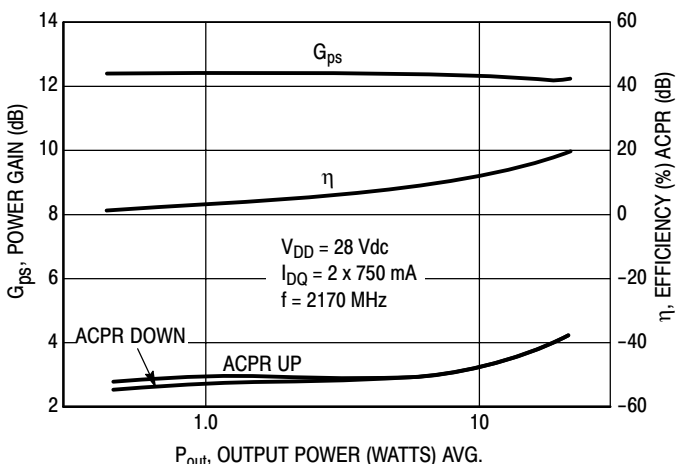


Figure 7. Power Gain, Efficiency, ACPR versus Output Power (W-CDMA)

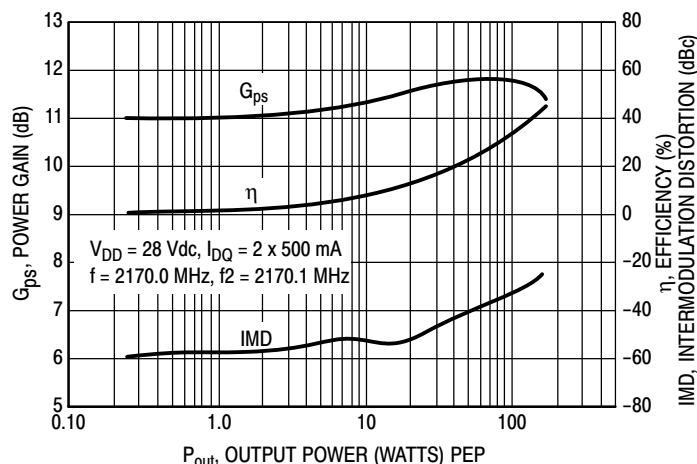
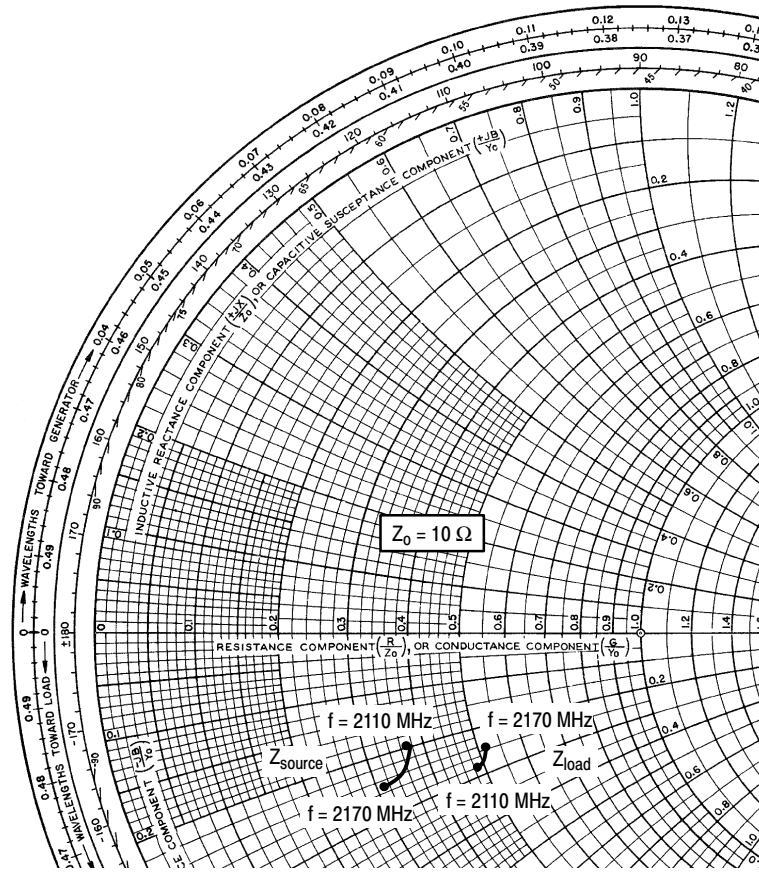


Figure 8. Power Gain, Efficiency, IMD versus Output Power

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$V_{DD} = 28\text{ V}$, $I_{DQ} = 2 \times 500\text{ mA}$, $P_{out} = 120\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$3.7 - j2.0$	$4.9 - j2.8$
2140	$3.5 - j2.4$	$5.1 - j2.7$
2170	$3.1 - j2.5$	$5.2 - j2.5$

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

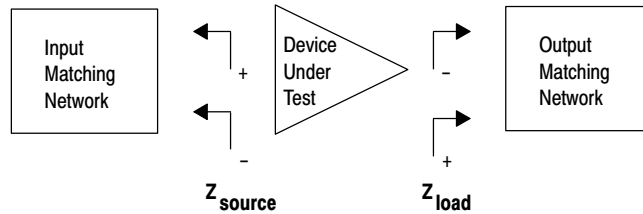
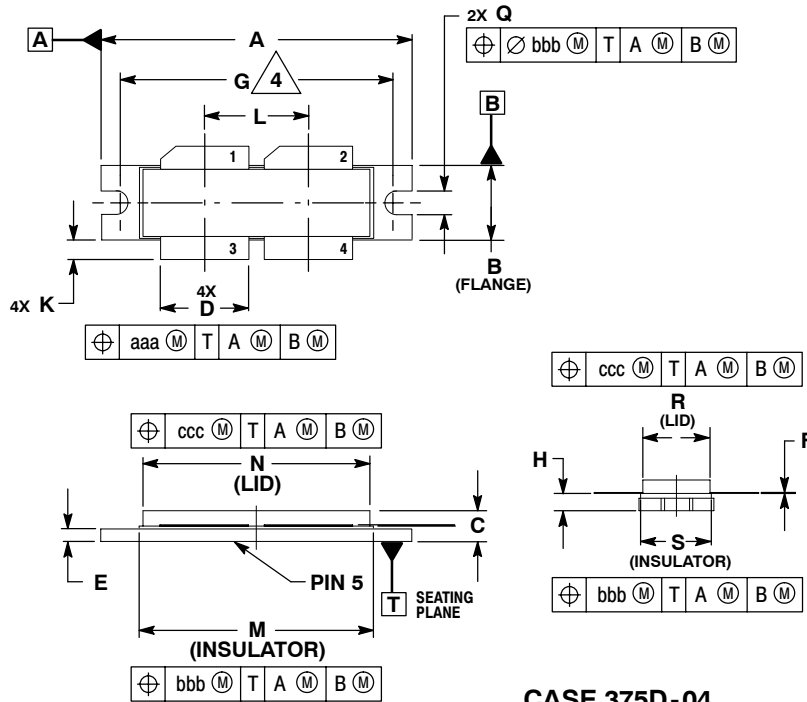


Figure 9. Series Equivalent Input and Output Impedance

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PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
 4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28
B	0.395	0.405	10.03	10.29
C	0.150	0.200	3.81	5.08
D	0.455	0.465	11.56	11.81
E	0.062	0.066	1.57	1.68
F	0.004	0.007	0.10	0.18
G	1.400 BSC		35.56 BSC	
H	0.079	0.089	2.01	2.26
K	0.117	0.137	2.97	3.48
L	0.540 BSC		13.72 BSC	
M	1.219	1.241	30.96	31.52
N	1.218	1.242	30.94	31.55
Q	0.120	0.130	3.05	3.30
R	0.355	0.365	9.01	9.27
S	0.365	0.375	9.27	9.53
aaa	0.013 REF		0.33 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.020 REF		0.51 REF	

- STYLE 1:
1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

**CASE 375D-04
ISSUE C
NI-1230**

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