MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

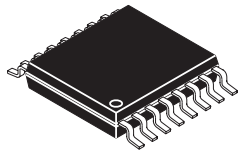
Document order number: MPC17517
Rev 1.0, 03/2004

Advance Information

1.0 A 6.8 V Dual Motor Driver IC

17517

1.0 A 6.8 V DUAL MOTOR DRIVER IC



DTB SUFFIX
CASE 948F-01
16-LEAD TSSOP

The 17517 is a monolithic triple totem-pole-output power IC designed to be used in portable electronic applications to control small DC motors and solenoids. The 17517 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V. Its low $R_{DS(ON)}$ totem-pole output MOSFETs (0.46 Ω typical) can provide continuos drive currents of 1.0 A and handle peak currents up to 3.0 A. It is easily interfaced to low-cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz.

The 17517 can drive two motors in two directions one at a time or drive one motor in two directions and one solenoid with synchronous rectification of freewheeling currents one at a time. Two-motor operation is accomplished by hooking one motor between OUTA and OUTB and hooking the other motor between OUTB and OUTC. Motor plus solenoid operation is accomplished by hooking a motor between OUTA and OUTB and a solenoid between OUTC and GND.

This device contains an integrated charge pump and level shifter (for gate drive voltages), integrated shoot-through current protection (cross-conduction suppression logic and timing), and undervoltage detection and shutdown circuitry.

The 17517 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

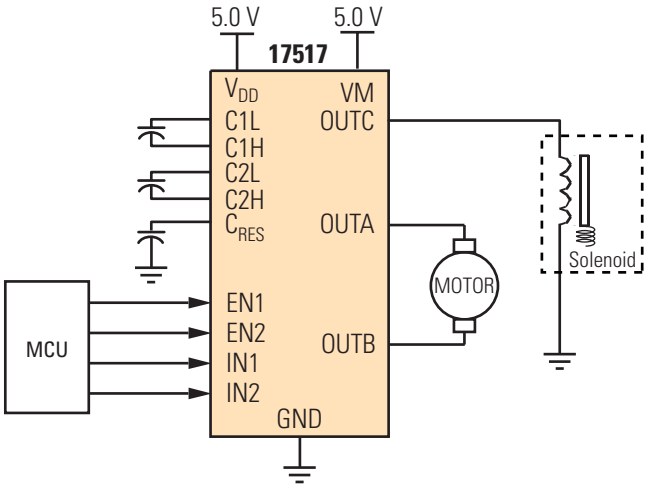
ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MPC17517DTB/R2	-20°C to 65°C	16 TSSOP

Features

- 2.0 V to 6.8 V Continuous Operation
- Output Current 1.0 A (DC), 3.0 A (Peak)
- MOSFETs < 600 mΩ $R_{DS(ON)}$ @ 25°C Guaranteed
- 3.0 V/5.0 V TTL-/CMOS-Compatible Inputs
- PWM Frequencies up to 200 kHz
- Undervoltage Shutdown

17517 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

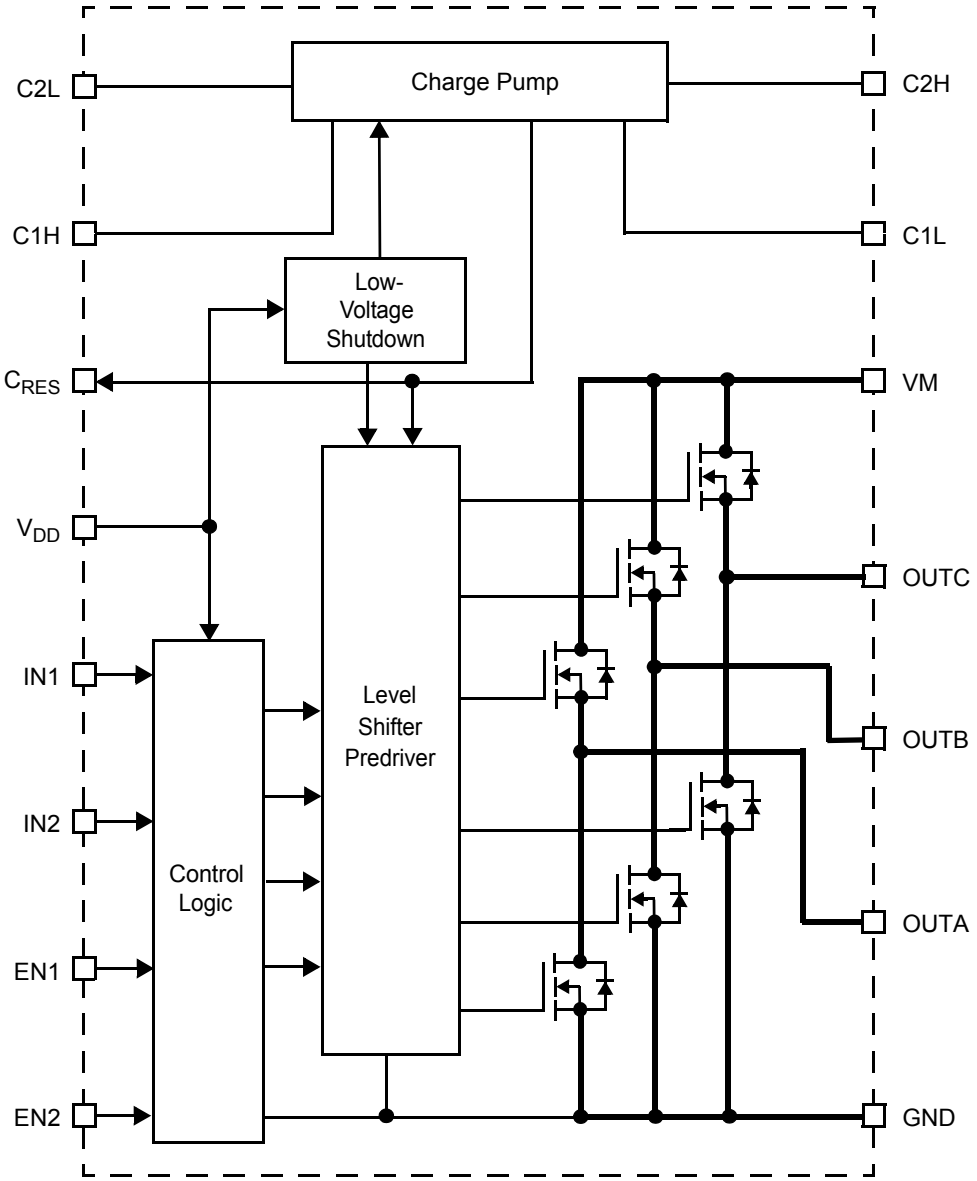
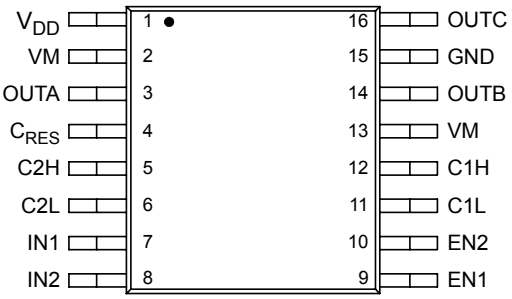


Figure 1. 17517 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	V_{DD}	Control Circuit Power Supply	Positive power source connection for control circuit.
2, 13	VM	Motor Drive Power Supply	Motor power supply voltage input terminals.
3	OUTA	Output A	Driver output A terminal.
4	C_{RES}	Charge Pump Output Capacitor Connection	Charge pump reservoir capacitor terminal.
5	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
6	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
7	IN1	Input Control 1	Control signal input 1 terminal.
8	IN2	Input Control 2	Control signal input 2 terminal.
9	EN1	Enable Control Signal Input 1	Enable control signal input 1 terminal.
10	EN2	Enable Control Signal Input 2	Enable control signal input 2 terminal.
11	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
12	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
14	OUTB	Output B	Driver output B terminal.
15	GND	Ground	Ground connection.
16	OUTC	Output C	Driver output C terminal.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	$V_{C_{RES}}$	-0.5 to 14	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (Note 1)	 I_O I_{OPK}	 1.0 3.0	A
ESD Voltage Human Body Model (Note 2) Machine Model (Note 3)	 V_{ESD1} V_{ESD2}	 ±2000 ±100	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Operating Junction Temperature	T_J	-20 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Thermal Resistance (Note 4)	$R_{\theta JA}$	190	°C/W
Power Dissipation (Note 5)	P_D	657	mW
Soldering Temperature (Note 6)	T_{SOLDER}	245	°C

Notes

1. T_A = 25°C, 10 ms pulse width at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. 37 mm x 50 mm Cu area (1.6 mm FR-4 PCB).
5. Maximum at T_A = 25°C.
6. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.7	V
Capacitor for Charge Pump	C1, C2, C3	0.01	0.1	1.0	μF
Standby Power Supply Current					
Motor Supply Standby Current	$I_{V_{MSTBY}}$	–	–	1.0	μA
Logic Supply Standby Current (Note 7)	$I_{V_{DDSTBY}}$	–	–	1.0	mA
Operating Power Supply Current					mA
Logic Supply Current (Note 8)	$I_{V_{DD}}$	–	–	3.0	
Charge Pump Circuit Supply Current	$I_{C_{RES}}$	–	–	0.7	
Low-Voltage Detection Circuit	V_{DD}DET				V
Detection Voltage (V_{DD}) (Note 9)		1.5	2.0	2.5	
Driver Output ON Resistance (Note 10)	$R_{DS(ON)}$	–	0.46	0.60	Ω
GATE DRIVE					
Gate Drive Voltage (Note 11)	$V_{C_{RES}}$				V
No Current Load		12	13	13.5	
Gate Drive Ability (Internally Supplied)	$V_{C_{RESload}}$				V
$I_{C_{RES}}$ = -1.0 mA		10	11.2	–	
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Input Function (2.7 V < V_{DD} < 5.7 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	μA
Low-Level Input Current	I_{IL}	-1.0	–	–	μA

Notes

7. $I_{V_{DDSTBY}}$ includes current to the predriver circuit.
8. $I_{V_{DD}}$ includes current to the predriver circuit.
9. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage $V_{C_{RES}}$ is applied from an external source, $V_{C_{RES}}$ = 7.5 V.
10. I_O = 1.0 A source + sink.
11. Input logic signal not present.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT (IN1, IN2, EN1, EN2)					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 12)	t_R	–	–	1.0 (Note 13)	μs
Input Pulse Fall Time (Note 14)	t_F	–	–	1.0 (Note 13)	μs
OUTPUT					
Propagation Delay Time					μs
Turn-ON Time	t_{PLH}	–	0.1	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Charge Pump Wake-Up Time (Note 15)	t_{VGON}	–	0.1	3.0	ms
Low-Voltage Detection Time	$t_{V_{DD}DET}$	–	–	10	ms

Notes

12. Time is defined between 10% and 90%.
13. That is, the input waveform slope must be steeper than this.
14. Time is defined between 90% and 10%.
15. When C1 = C2 = C3 = 0.1 μF.

Timing Diagrams

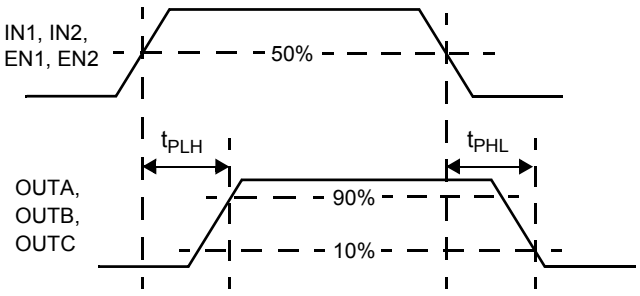


Figure 2. t_{PLH}, t_{PHL}, and t_{PZH} Timing

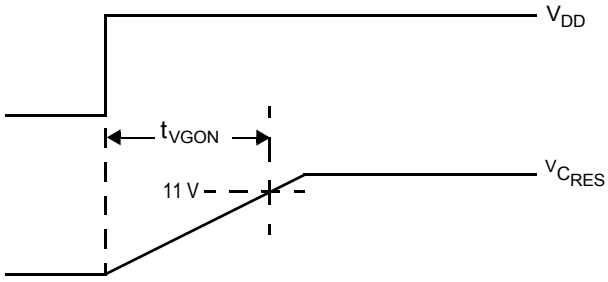


Figure 4. Charge Pump Timing

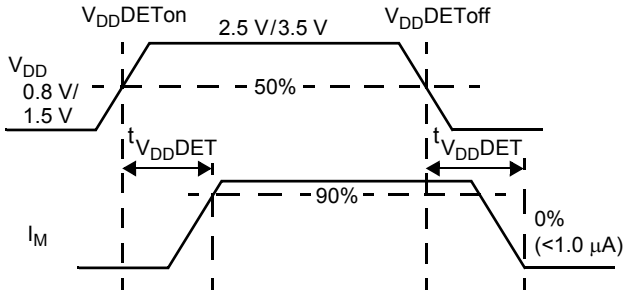


Figure 3. Low-Voltage Detection Timing

Table 1. Truth Table

INPUT				OUTPUT		
IN1	**IN2**	**EN1**	**EN2**	**OUTA**	**OUTB**	**OUTC**
Shutdown Mode						
X	X	L	L	Z	Z	Z
Channel 1 (A–B) Driving Mode						
H	H	H	L	L	L	Z
H	L	H	L	H	L	Z
L	H	H	L	L	H	Z
L	L	H	L	Z	Z	Z
Channel 2 (B–C) Driving Mode						
H	H	L	H	Z	L	L
H	L	L	H	Z	H	L
L	H	L	H	Z	L	H
L	L	L	H	Z	Z	Z
Half-Bridge (C) Driving Mode						
H	H	H	H	Z	Z	Z
H	L	H	H	Z	Z	H
L	H	H	H	Z	Z	L
L	L	H	H	Z	Z	Z

H = High.
L = Low.
Z = High impedance.
X = Don’t care.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17517 is a triple totem-pole output H-Bridge power IC designed to drive small dc motors used in portable electronics. The 17517 can operate efficiently with supply voltages as low as 2.0 V to as high as 6.8 V, and provide continuos motor drive currents of 1.0 A while handling peak currents up to 3.0 A. It is easily interfaced to low cost MCUs via parallel 3.0 V- or 5.0 V-compatible logic. The device can be pulse width modulated (PWM-ed) at up to 200 kHz. The 17517 can drive two motors in two directions one at a time; or it can drive one motor in two directions and one solenoid with synchronous rectification of freewheeling currents one at a time. Two-motor operation is accomplished by hooking one motor between OUTA and OUTB, and the other motor between OUTB and OUTC. Motor + solenoid operation is accomplished by hooking a motor between OUTA and OUTB and placing a solenoid between OUTC and GND. Table 1, Truth Table, page 8, describes the operating states versus the input conditions.

As shown in Figure 1, 17517 Simplified Internal Block Diagram, page 2, the 17517 is a monolithic triple totem-pole output bridge with built-in charge pump circuitry. Each of the six MOSFETs forming the triple totem-pole output has an $R_{DS(ON)}$ of $\leq 0.6\ \Omega$ (guaranteed by design). The IC has an integrated charge pump and level shifter (for gate drive voltages). Additionally, the IC has a built-in shoot-through current protection circuit and undervoltage lockout function. This IC has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance).

FUNCTIONAL TERMINAL DESCRIPTION

OUTA, OUTB, and OUTC

These terminals provide the connection to the internal power MOSFET triple-totem-pole H-bridge of the IC.

GND

Power and signal ground terminal.

C_{RES}

This terminal provides the connection for the external reservoir capacitor (output of the charge pump). Alternatively, this terminal can also be used as an input to supply gate-drive voltage from an external source via a series current-limiting resistor.

The voltage at the C_{RES} terminal will be approximately three times the V_{DD} voltage, as the internal charge pump utilizes a voltage tripler circuit. The V_{DDRES} voltage is used by the IC to supply gate drive for the internal power MOSFETs.

VM

The two VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the load attached between OUTA and OUTB.

The VM terminals must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between terminals.

IN1, IN1, EN1, and EN2

These terminals are input control terminals used to control the outputs. These terminals are 3.0 V/5.0 V CMOS-compatible inputs with hysteresis. These terminals work together to control OUTA, OUTB, and OUTC (refer to Table 1, Truth Table).

C1L and C1H, C2L and C2H

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

V_{DD}

This terminal carries the logic supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

APPLICATIONS

Typical Application

Figure 5 shows a typical application for the 17517. When applying the gate voltage to the C_{RES} terminal from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = {}^{V}C_{RES}/0.02\ \Omega$.

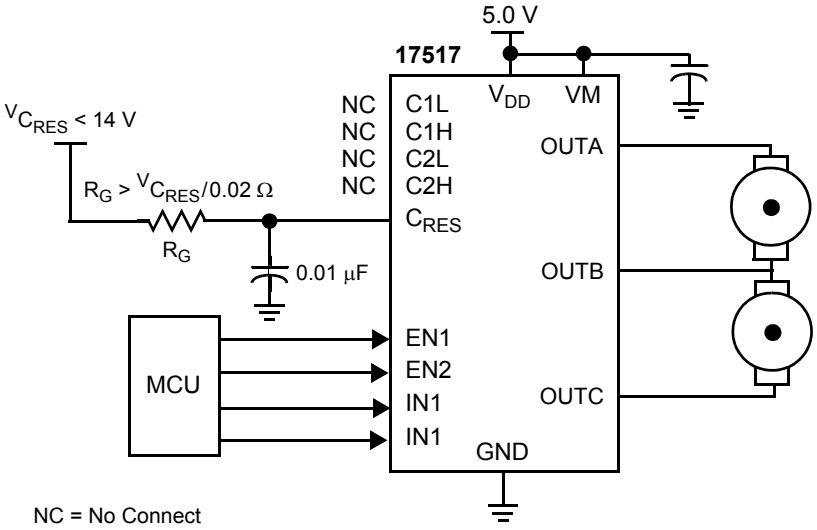


Figure 5. 17517 Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply terminal (VM) (see Figure 6).

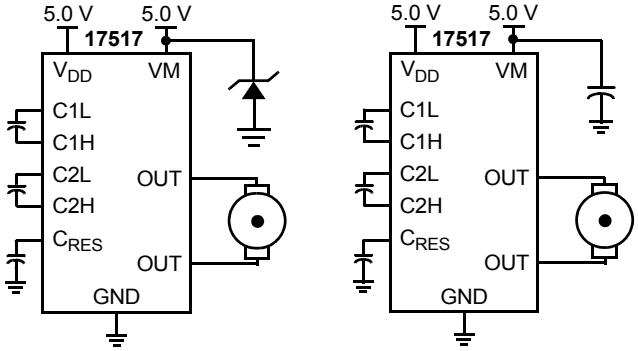


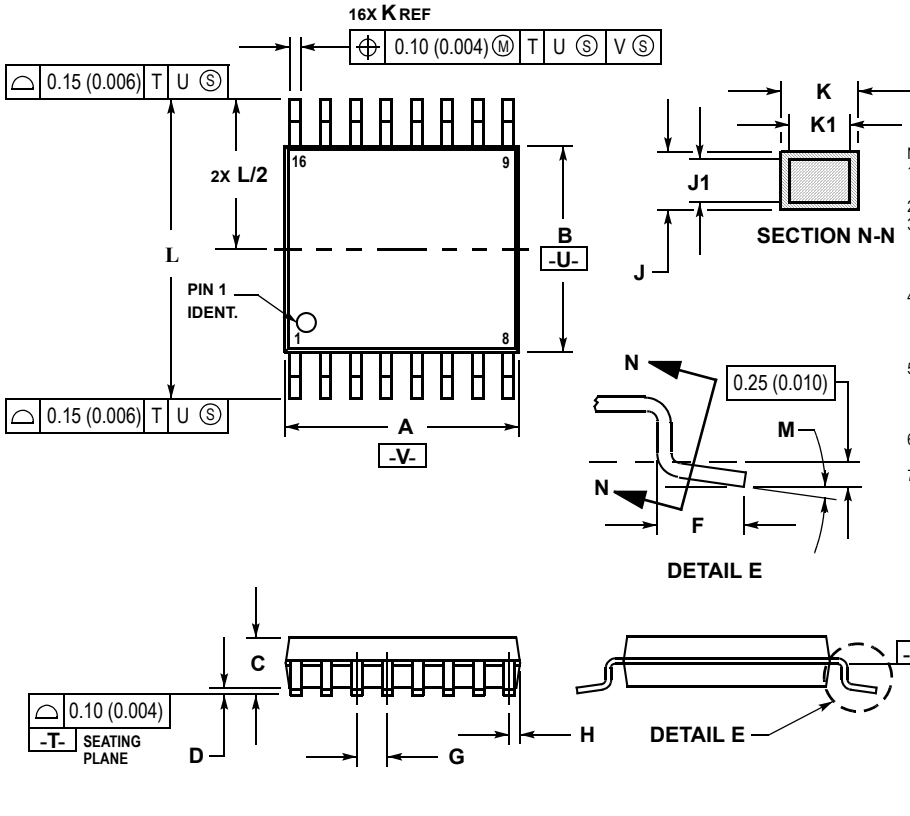
Figure 6. CEMF Snubbing Techniques

PCB Layout

When designing the printed circuit board (pcb), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

PACKAGE DIMENSIONS

DTB SUFFIX
16-LEAD TSSOP
PLASTIC PACKAGE
CASE 948F-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:
Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center
3-20-1 Minami-Azabu. Minato-ku, Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
852-26668334

HOME PAGE: http://motorola.com/semiconductors