HYBRID FLASH SOLUTION

56F801

16-bit Hybrid Controller

MOTOROLA
intelligence everywhere

digital dna

Freescale Semiconductor, Inc.

TARGET APPLICATIONS

- Pumps
- Industrial fans
- Exercise equipment
- Smart appliances
- Compressors
- Noise cancellation
- HVAC
- Remote monitoring
- Tachometers
- Cable test equipment
- General purpose devices
- Switched-mode power supplies

The 56F801 is a member of the 56800 core-based family of Hybrid Controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F801 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.
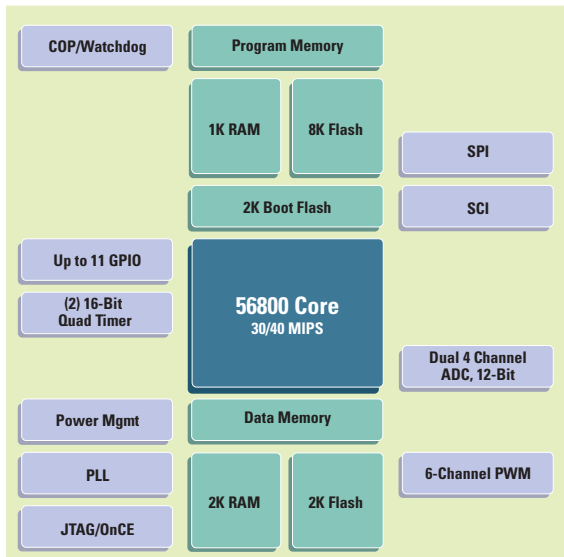
BENEFITS

- On-board voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage
- Internal Relaxation Oscillator for cost-sensitive applications by eliminating the need for an external crystal
- Flash memory is engineered to provide reliable, non-volatile memory storage, eliminating the need for external storage devices
- Easy to program with flexible application development tools
- Simple updating of Flash memory through SPI, SCI or OnCE™, using on-chip boot loader

- Program can boot directly from Flash
- Supports multiple motors or multi-phase control
- Patented distortion correction in PWM for lower-risk, better performing control
- PWM and ADC modules are tightly coupled to reduce processing overhead
- Low voltage interrupts protect the system during brownout or power failure
- Simple interface with other asynchronous serial communication devices and off-chip EE memory

56F801 16-BIT HYBRID CONTROLLER

- Up to 40 MIPS operation at 80Mhz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 12K On-chip Flash
  - 8K Program Flash
  - 2K Data Flash
  - 2K Boot Flash
- 1K Program RAM
- 1K Data RAM

- Hardware DO and REP loops
- 6-channel PWM Module
- Two 4-channel, 12-bit ADCs
- Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- JTAG/OnCE port for debugging
- On-chip Relaxation Oscillator
- 48-pin LQFP Package
- 11 shared GPIO
- Two general purpose Quad Timers

ENERGY INFORMATION

- Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply

- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

COP/Watchdog	Program Memory	
	1K RAM	8K Flash
		SPI
	2K Boot Flash	SCI
Up to 11 GPIO	**56800 Core** 30/40 MIPS	
(2) 16-Bit Quad Timer		
		Dual 4 Channel ADC, 12-Bit
Power Mgmt	Data Memory	
PLL	2K RAM / 2K Flash	6-Channel PWM
JTAG/OnCE		

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PRODUCT DOCUMENTATION

DSP56800 Family Manual
Detailed description of the 56800 family architecture, and 16-bit DSP core processor and the instruction set.
Order Number: DSP56800FM/D

DSP56F80x User's Manual
Detailed description of memory, peripherals, and interfaces of the 56F801, 56F802, 56F803, 56F805, and 56F807
Order Number: DSP56F801-7UM/D

DSP56F801 Technical Data Sheet
Electrical and timing specifications, pin descriptions, and package descriptions
Order Number: DSP56F801/D

DSP56F801 Product Brief and interfaces
Summary description and block diagram of the core, memory, peripherals
Order Number: DSP56F801PB/D

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

- The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

56800 CORE FEATURES

- Efficient 16-bit 56800 family hybrid controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

56F801 MEMORY FEATURES

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 12K On-chip Flash
    - 8K Program Flash
    - 2K Data Flash
    - 2K Boot Flash
  - 1K Program RAM
  - 1K Data RAM
- Programmable Boot Flash supports customized boot code and field upgrades of stored code through a variety of interfaces (JTAG, CAN, SPI)

56F801 PERIPHERAL CIRCUIT FEATURES

- Pulse Width Modulator (PWM) with six PWM outputs, two Fault inputs, fault-tolerant design with dead-time insertion; supports both center- and edge-aligned modes
- Two 12-bit Analog-to-Digital Converters (ADCs), which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two general purpose Quad Timers
- Serial Communication Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eleven multiplexed General Purpose I/O (GPIO) pins
- Computer Operating Properly (COP)/ Watchdog timer
- Two dedicated external interrupt pins
- External reset pin for hardware reset
- JTAG/OnCE™ for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer
- Oscillator flexibility between either an external crystal oscillator or an on-chip relaxation oscillator

ORDERING INFORMATION

PART	SUPPLY VOLTAGE	PACKAGE TYPE	PIN COUNT	FREQUENCY (MHz)	ORDER NUMBER
DSP56F801	3.0–3.6V	Low-profile Quad Flat Pack (LQFP)	48	80	DSP56F801FA80
DSP56F801	3.0–3.6V	Low-profile Quad Flat Pack (LQFP)	48	60	DSP56F801FA60
DSP56F801	3.0–3.6V	Low-profile Quad Flat Pack (LQFP)	48	80	SPAK56F801FA80

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