MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document from Analog Marketing: MM908E624/D
Rev 1.0, 09/2003

Preliminary Information

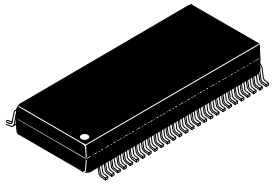
908E624

Integrated Triple High-Side Switch with Embedded MCU and LIN Serial Communication for Relay Drivers

TRIPLE HIGH-SIDE SWITCH WITH EMBEDDED MCU AND LIN

The 908E624 is a highly integrated single-package solution that includes a high-performance HC08 microcontroller with a SMARTMOS™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI), and an internal clock generator module. The analog control die provides three high-side outputs with diagnostic functions, voltage regulator, watchdog, operational amplifier, and local interconnect network (LIN) physical layer.

The 908E624 has been developed as a highly integrated and cost-effective solution for driving loads using relays within a LIN architecture. It is especially suited for the control of automotive high-current motors applications using relays (e.g., window lifts, fans, and sun roofs).



DWB SUFFIX
CASE 1365-01
54-TERMINAL SOICWB

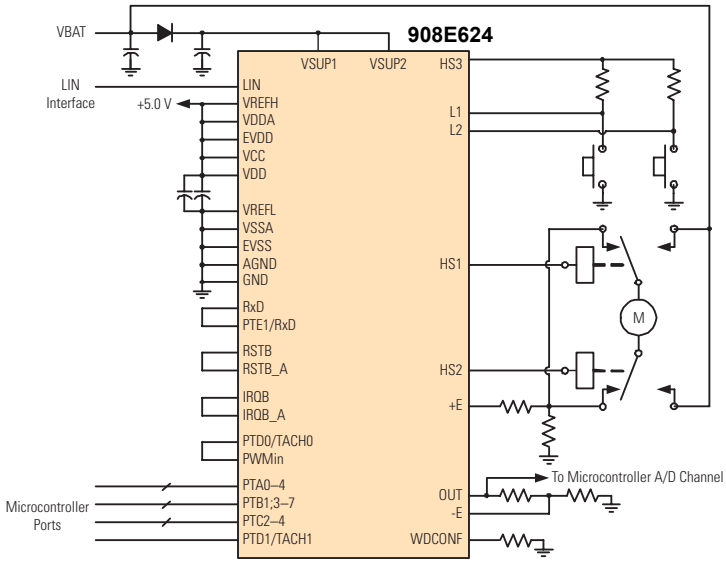
Features

- High-Performance M68HC08 Core
- 16 K Bytes of On-Chip Flash Memory
- 512 Bytes of RAM
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter (ADC)
- LIN Physical Layer Interface
- Low Drop Voltage Regulator
- Three High-Side Outputs
- Two Wake-Up Inputs
- 16 Microcontroller I/Os

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PM908E624ACDWB/R2	-40°C to 85°C	54 SOIC WB

908E624 Simplified Application Diagram



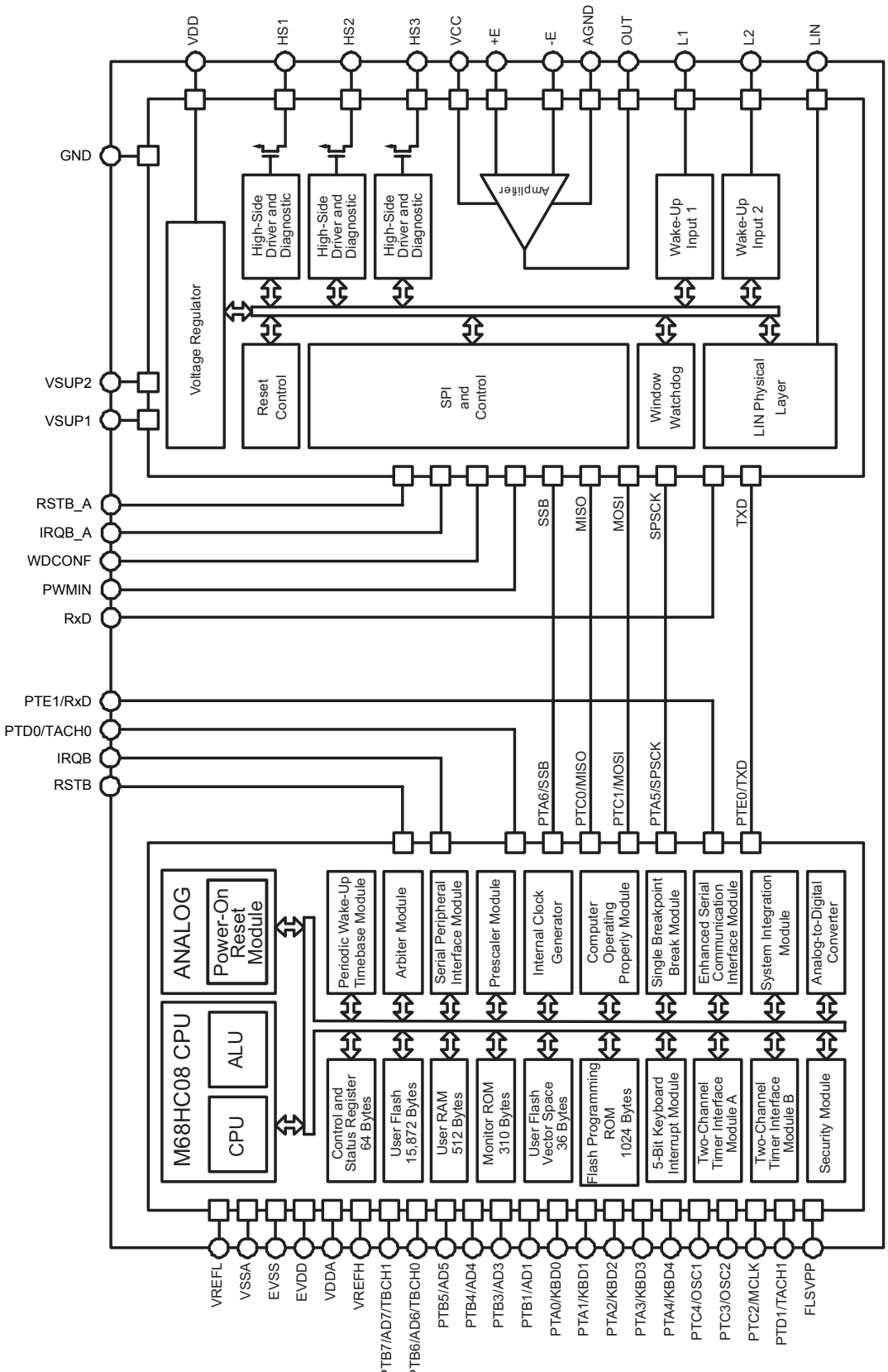
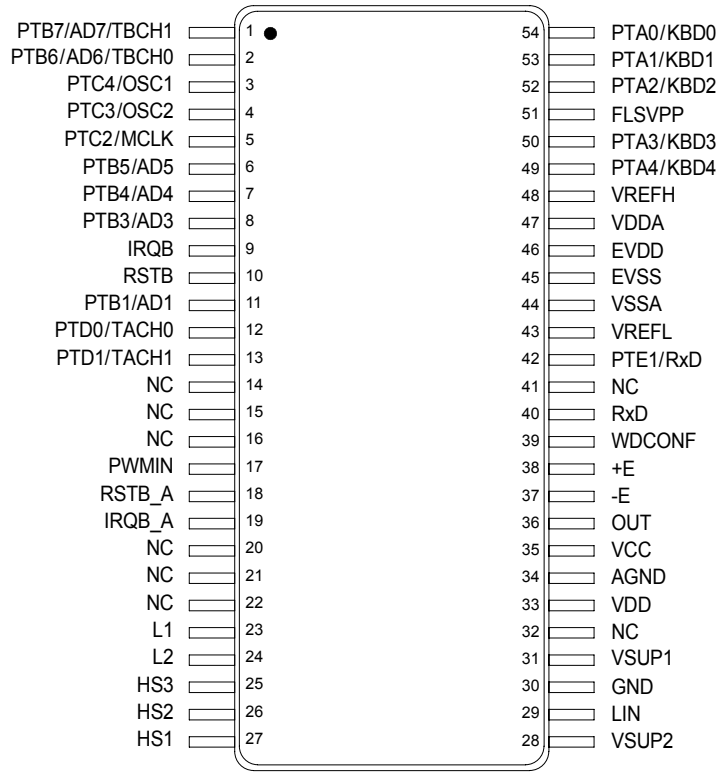


Figure 1. 908E624 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Die	Description
1	PTB7/AD7/ TBCH1	MCU	Port B, Terminal 7 (shared with ADC and Timer Channel B)
2	PTB6/AD6/ TBCH0	MCU	Port B, Terminal 6 (shared with ADC and Timer Channel B)
3	PTC4/OSC1	MCU	Port C, Terminal 4
4	PTC3/OSC2	MCU	Port C, Terminal 3
5	PTC2/MCLK	MCU	Port C, Terminal 2
6	PTB5/AD5	MCU	Port B, Terminal 5 (shared with ADC)
7	PTB4/AD4	MCU	Port B, Terminal 4 (shared with ADC)
8	PTB3/AD3	MCU	Port B, Terminal 3 (shared with ADC)
9	IRQB	MCU	Interrupt Input Terminal
10	RSTB	MCU	Reset Terminal
11	PTB1/AD1	MCU	Port B, Terminal 1 (shared with ADC)
12	PTD0/TACH0	MCU	Port D, Terminal 0 (shared with ADC and Timer Channel A)
13	PTD1/TACH1	MCU	Port D, Terminal 1 (shared with ADC and Timer Channel A)
14, 15, 16 20–22, 32, 41	NC	–	Not Connected
17	PWMIN	Analog	Direct Input Terminal for High-Side Control
18	RSTB_A	Analog	Reset Terminal

TERMINAL FUNCTION DESCRIPTION (continued)

Terminal	Terminal Name	Die	Description
19	IRQB_A	Analog	Interrupt Output Terminal
23, 24	L1, L2	Analog	40 V-Rated Wake-Up Inputs L1 and L2
25, 26, 27	HS3, HS2, HS1	Analog	High-Side Outputs 3 to 1
28, 31	VSUP2, VSUP1	Analog	Supply Voltage Terminals 2 and 1
29	LIN	Analog	LIN Physical Layer
30	GND	Analog	GND Supply Terminal
33	VDD	Analog	Voltage Regulator (+5.0 V) Output Terminal
34	AGND	Analog	GND Supply Terminal
35	VCC	Analog	+5.0 V Supply Input of the Sense Amplifier
36	OUT	Analog	Output of the Sense Amplifier
37	-E	Analog	Inverted Input of the Sense Amplifier
38	+E	Analog	Noninverted Input of the Sense Amplifier
39	WDCONF	Analog	Watchdog Configuration Terminal
40	RxD	Analog	LIN Receiver Output
42	PTE1/RxD	MCU	Port E, Terminal 1 (shared with SCI RX Line)
43	VREFL	MCU	ADC Supply Terminal
44	VSSA	MCU	GND Supply Terminal
45	EVSS	MCU	GND Supply Terminal
46	EVDD	MCU	+5.0 V Supply Terminal
47	VDDA	MCU	+5.0 V Supply Terminal
48	VREFH	MCU	ADC Supply Terminal
49	PTA4/KBD4	MCU	Port A, Terminal 4 (shared with Keyboard Module)
50	PTA3/KBD3	MCU	Port A, Terminal 3 (shared with Keyboard Module)
51	FLSVPP	MCU	Test Terminal
52	PTA2/KBD2	MCU	Port A, Terminal 2 (shared with Keyboard Module)
53	PTA1/KBD1	MCU	Port A, Terminal 1 (shared with Keyboard Module)
54	PTA0/KBD0	MCU	Port A, Terminal 0 (shared with Keyboard Module)

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-State)	$V_{SUP(ss)}$	-0.3 to 27	
Analog Chip Supply Voltage under Transient Conditions	$V_{SUP(pk)}$	-0.3 to 40	
MCU Chip Supply Voltage	V_{DD}	-0.3 to 6.0	
Logic Input Terminal Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to V_{DD}+0.3	
MCU Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum MCU Current per Terminal			mA
All Terminals except VDD/VSS/PTA0–PTA6/PTC0–PTC1	$I_{pin(1)}$	±15	
Terminals PTA0–PTA6 and PTC0–PTC1	$I_{pin(2)}$	±25	
Maximum MCU VSS Output Current	I_{MVSS}	100	mA
Maximum MCU VDD Input Current	I_{MVDD}	100	mA
E+, E- Input Voltage	V_{E+E-}	-0.3 to 7.0	V
E+ E- Input Current	I_{E+E-}	20	mA
Output Voltage	V_{OUT}	-0.3 to V_{DD}+0.3	mA
Output Current	I_{OUT}	20	mA
LIN Supply Voltage			V
Normal Operation with a 33 kΩ resistor (Steady-State)	$V_{BUS(ss)}$	-18 to 40	
Transient Input Voltage (according to ISO7637 Specification) and with External Components	$V_{BUS(dynamic)}$	-100 to 100	
L1 and L2			V
Normal Operation (Steady-State)	$V_{BUS(ss)}$	-18 to 40	
Transient Input Voltage (according to ISO7637 Specification) and with External Components	$V_{BUS(dynamic)}$	-150 to 100	
ESD Voltage			V
Human Body Model L1, L2, and LIN / All Other Terminals (Note 1)	V_{ESD1}	±4000/±2000	
Machine Model (Note 2)	V_{ESD2}	±200	
Charge Device Model	V_{ESD3}	±500	

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
2. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).

MAXIMUM RATINGS (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Junction Temperature (Note 3) Analog MCU	 $T_{JAnalog}$ T_{JMCU}	 -40 to 150 -40 to 125	 °C °C
Terminal Soldering Temperature (Note 4)	T_{SOLDER}	TBD	°C
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	TBD	°C/W

Notes

3. Die temperature of analog and MCU is linked via the package. High temperature on analog die can lead to a high MCU temperature.
4. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal DC Voltage Range	V_{SUP}	5.5	–	18	V
Input Voltage During Load Dump	V_{SUPLD}	–	–	40	V
Input Voltage During Jump Start (Note 5)	V_{SUPJS}	–	–	27	V
Supply Voltage Fail Early Warning Threshold	V_{SUVew}	5.7	6.0	6.6	V
Supply Voltage Fail Flag Hysteresis	$V_{SUVhyst}$	–	1.0	–	V
Supply Voltage Overvoltage Warning Threshold	V_{SOVw}	18	19.25	20.5	V
Supply Voltage Overvoltage Flag Hysteresis	$V_{SOVhyst}$	–	220	–	mV
SUPPLY CURRENT RANGE					
Supply Current in Normal Mode (Note 6), (Note 7)	$I_{SUP(norm)}$	–	–	7.0	mA
Supply Current in SLEEP Mode (Note 6) V_{SUP} = 13.5 V	I_{SLEEP}	–	35	40	μA
Supply Current in STOP Mode (Note 6) V_{SUP} = 13.5 V	I_{STOP}	–	55	70	μA
DIGITAL INTERFACE RATINGS					
Reset Terminal (Output Terminal Only) in Normal and STOP Mode (RSTB_A)					
Reset Threshold	V_{RSTth1}	TBD	4.6	TBD	V
High-Level Output Current 0 V < V_{OUT} < 0.7V_{DD}	I_{OL}	–	-250	–	μA
Low-Level Output Voltage I_O = 1.5 mA	V_{OL}	0	–	0.9	V
Reset Pull-Down Current	I_{pdw}	1.5	–	8.0	mA
Reset Duration After V_{DD} High	t_{RST}	0.65	1.0	1.35	ms
Logic Input: PWMIN					
High-Level Input Voltage	V_{IH}	0.7$_{VDD}$	–	V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}	-0.3	–	0.3V_{DD}	V
Input Current 0 V < V_{IN} < V_{DD}	I_{IN}	-10	–	10	μA

Notes

5. Device is fully functional. All functions are operating. Overtemperature may occur.
6. Total current (I_{VSUP1} + I_{VSUP2}) measured at GND terminal.
7. Supply current of the analog die, microcontroller supply current. Refer to the MC68HC908EY16 specification.

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE RATINGS (continued)					
Logic Input: TxD					
High-Level Input Voltage	V_{IH}	3.5	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	1.5	V
Input Threshold Hysteresis	I_{IN}	50	550	800	mV
Pull-Up Current Source	I_S	-100	–	-20	μA
Logic Output: IRQB_A					
High-Level Output Voltage I_O = -250 μA	V_{OH}	V_{DD}-0.9	–	V_{DD}	V
Low-Level Output Voltage I_O = 1.5 mA	V_{OL}	0	–	0.9	V
WDCONFIG: WINDOW WATCHDOG CONFIGURATION TERMINAL					
External Resistor Range	R_{EXT}	10	–	100	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) (Note 8)	WD_{CACC}	-15	–	15	%
Watchdog Period; R = 10 kΩ (1%)	Pwd10	–	10.558	–	ms
Watchdog Period; R = 100 kΩ (1%)	Pwd100	–	99.748	–	ms
Watchdog Period Without External Resistor, WDCONF Terminal Open	Pwdoff	97	150	205	ms

Notes

8. Watchdog timing period calculation formula: Twd = 0.991 ∗ R+0.648 (R in kΩ and Twd in ms).

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR Specification with external capacitor 1.0 μF< C < 10 μF and 200 mΩ ≤ ESR ≤ 1.0 Ω. Capacitor value up to 47 μF can be used.					
VDD Output Voltage 2.0 mA < I_{DD} < 50 mA, 5.5 V < V_{SUP} < 27 V	VDD_{OUT}	4.75	5.0	5.25	V
Dropout Voltage (Note 9) I_{DD} = 50 mA	VDD_{DROP}	–	0.1	0.25	V
VDD Output Voltage Extended Range TBD < V_{SUP} < 5.5 V	VDD_{OUTex1}	TBD	–	5.25	V
VDD Output Voltage During STOP Mode (Note 10)	VDD_{STOP}	4.75	5.0	5.25	V
STOP Mode Regulator Current Limitation	I_{DDS}	–	8.0	–	mA
I_{DD} Output Current Limitation (Note 11)	IDD_{OUT}	60	110	200	mA
Overtemperature Pre-Warning (Junction)	T_{PRE}	130	–	160	°C
Thermal Shutdown (Junction)	T_{SD}	165	–	–	°C
Temperature Threshold Difference T_{SD}-T_{PRE}	$\Delta_{TSD-TPRE}$	20	30	40	°C
VSUP Range for Reset Active	V_{SUPr}	3.5	–	–	V
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA	LR	–	20	150	mV
Load Regulation 1.0 mA < I_{DD} < 50 mA	LD	–	40	150	mV
Line Regulation 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	LR-s	–	10	100	mV
Load Regulation 1.0 mA < I_{DD} < 10 mA	LD-s	–	40	150	mV

Notes

9. Measured when voltage has dropped 100 mV below its nominal value.
10. When switching from Normal to STOP mode or from STOP mode to Normal mode, the output voltage can vary within the output voltage specification.
11. Total VDD regulator current. A 5.0 mA current for operational amplifier is included. Digital output supplied from VDD.

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PHYSICAL LAYER					
Output Low Level Tx Low, Rext-Pull-up = 500 Ω	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level Tx High, I_{OUT} = 1.0 μA	$V_{LIN-HIGH}$	V_{SUP}-1	–	–	V
Pull-Up Resistor to V_{SUP}	R_{PU}	20	30	47	kΩ
Pull-Up Current Source	I_{PU}	–	10	–	μA
Output Current Shutdown Threshold	I_{OV-CUR}	50	75	150	mA
Output Current Shutdown Delay	$I_{OV-DELAY}$	–	10	–	μs
Leakage Current to GND Recessive State, V_{SUP} 8.0 V to 18 V, V_{LIN} 8.0 V to 18 V	$I_{BUS-PAS-REC}$	0	3.0	–	μA
Leakage Current GND Disconnected, V_{GND} = V_{SUP}, V_{LIN} at -18 V	$I_{BUS-NOGND}$	-1.0	–	1.0	mA
Leakage Current to GND VSUP Disconnected, V_{LIN} at 18 V	I_{BUS}	–	1.0	10	μA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} VIH	 0.6 V_{BUS} 0 0.475 –	 – – 0.5 –	 V_{SUP} 0.4 V_{BUS} 0.525 0.175	 V V V_{SUP} V_{SUP}
LIN Wake-Up Threshold V_{SUP} = 14 V	V_{WTH}	–	0.5 V_{SUP}	–	V
HIGH-SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance T_J = 25°C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 125°C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 125°C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} > 9.0 V	 $R_{DS(ON)25}$ $R_{DS(ON)125}$ $R_{DS(ON)3}$	 – – –	 2.0 – 3.0	 2.5 4.5 –	Ω
Output Current Limitation	I_{LIM}	200	–	500	mA
Overtemperature Shutdown (Note 9)	Ovt	155	–	190	°C
Leakage Current	I_{LEAK}	–	–	10	μA
Output Clamp Voltage I_{OUT} = -100 mA	V_{CL}	-6.0	–	–	V
Energy Clamp	E	–	–	TBD	mJ

Notes

12. When overtemperature occurs, switch is turned off and latched off. Flag is set in SP.I

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH-SIDE OUTPUT HS3					
Switch On Resistance					Ω
T_J = 25°C, I_{LOAD} = 50m A, V_{SUP} > 9.0 V	$R_{DS(ON)25}$	–	–	7.0	
T_J = 125°C, I_{LOAD} = 50 mA, V_{SUP} > 9.0 V	$R_{DS(ON)125}$	–	–	10	
T_J = 125°C, I_{LOAD} = 30 mA, 5.5 V < V_{SUP} > 9.0 V	$R_{DS(ON)3}$	–	–	14	
Output Current Limitation	I_{LIM}	60	–	–	mA
Overtemperature Shutdown	Ovt	155	–	190	°C
Leakage Current	I_{LEAK}	–	–	10	μA
SENSE CURRENT AMPLIFIER					
Rail to Rail Input Voltage	V_{IMC}	-0.1	–	V_{DD}+0.1	V
Output Voltage Range (I_O = 1.0 mA)	V_{OUT1}	0.1	–	V_{DD}-0.1	V
Output Voltage Range (Output Current ±5.0 mA)	V_{OUT2}	0.3	–	V_{DD}-0.3	V
Input Bias Current	I_B	–	–	250	nA
Input Offset Current	I_O	-100	–	100	nA
Input Offset Voltage	V_{IO}	-15	–	15	mV
Supply Voltage Rejection Ratio (Note 13)	SVR	60	–	–	dB
Common Mode Rejection Ratio (Note 13)	CMR	70	–	–	dB
Gain Bandwidth (Note 13)	GBP	1.0	–	–	MHz
Slew Rate	SR	0.5	–	–	V/μs
Phase Margin (for Gain = 1, Load 100 pF//5.0 kΩ (Note 13)	PHMO	40	–	–	°
Open Loop Gain	OLG	–	TBD	–	dB

Notes

13. Guaranteed by design.

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for MCU characteristics. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
L1 AND L2 INPUTS					
Negative Switching Threshold	V_{thn}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.6	
Positive Switching Threshold	V_{thp}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYST}				V
5.5 V < V_{SUP} < 27 V		0.5	–	1.3	
Input Current	I_{IN}				μA
-0.2 V < V_{IN} < 40 V		-10	–	10	
Wake-Up Filter Time (Note 14)	t_{WUF}	8.0	20	38	μs

Notes

14. Guaranteed by design.

DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the MCU chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate (Note 15)					
Dominant Propagation Delay Tx to LIN (Measurement Threshold 58.1% V_{SUP})	$t_{DOM-min}$	–	–	50	µs
Dominant Propagation Delay Tx to LIN (Measurement Threshold 28.4% V_{SUP})	$t_{DOM-max}$	–	–	50	µs
Recessive Propagation Delay Tx to LIN (Measurement Threshold 42.2% V_{SUP})	$t_{REC-min}$	–	–	50	µs
Recessive Propagation Delay Tx to LIN (Measurement Threshold 74.4% V_{SUP})	$t_{REC-max}$	–	–	50	µs
Propagation Delay Symmetry: $t_{DOM-min}$ - $t_{REC-max}$	dt1	-10.44	–	8.12	µs
Propagation Delay Symmetry: $t_{DOM-max}$ - $t_{REC-min}$	dt2	-10.44	–	8.12	µs
Driver Characteristics for Slow Slew Rate (Note 15)					
Dominant Propagation Delay Tx to LIN (Measurement Threshold 61.1% V_{SUP})	$t_{DOM-min}$	–	–	100	µs
Dominant Propagation Delay Tx to LIN (Measurement Threshold 25.1% V_{SUP})	$t_{DOM-max}$	–	–	100	µs
Recessive Propagation Delay Tx to LIN (Measurement Threshold 38.9% V_{SUP})	$t_{REC-min}$	–	–	100	µs
Recessive Propagation Delay Tx to LIN (Measurement Threshold 77.8% V_{SUP})	$t_{REC-max}$	–	–	100	µs
Propagation Delay Symmetry: $t_{DOM-min}$ - $t_{REC-max}$	dt1s	-21.88	–	17.44	µs
Propagation Delay Symmetry: $t_{DOM-max}$ - $t_{REC-min}$	dt2s	-21.88	–	17.44	µs
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	–	20	–	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay (Note 16)	t_{rL}	–	3.5	6.0	µs
Receiver Recessive Propagation Delay (Note 16)	t_{rH}	–	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{r-Sym}	-2.0	–	2.0	µs
Bus Wake-Up Deglitcher	t_{propWL}	30	50	80	µs
Bus Wake-Up Event Reported Note	t_{wake}	–	20	–	µs
HIGH-SIDE OUTPUTS HS1 AND HS2					
Turn On Time Delay (Note 18)	t_{don}	–	–	10	µs
Turn Off Time Delay (Note 18)	t_{doff}	–	–	10	µs

Notes

15. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 k, 6.8 nF/660, 10 nf/500. Measurement thresholds: 50% of Tx signal to LIN signal threshold defined at each parameter.
16. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of Rx signal.
17. t_{wake} is typically 2 internal clock cycles after LIN rising edge detected. Refer to “LIN Bus Wake-Up Behavior” figure. In SLEEP mode the V_{DD} rise time is strongly dependant upon the decoupling capacitor at VDD terminal.
18. Delay between turn on or turn off command and high-side on or high-side off, excluding rise or fall time due to external load.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 specification for characteristics of the MCU chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH-SIDE OUTPUTS HS3					
Turn On Time Delay (Note 19)	t_{don}	–	–	20	µs
Turn Off Time Delay (Note 19)	t_{doff}	–	–	20	µs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	f_{SPIOP}	0.25	–	4.0	MHz
STATE MACHINE TIMING					
Delay Between SSB Low to High Transition (at End of SPI STOP Command) and STOP Mode Activation (Note 20)	$t_{SSB-STOP}$	TBD	TBD	TBD	µs
Interrupt Low-Level Duration	t_{INT}	7.0	10	13	µs
Internal Oscillator Frequency Accuracy (Note 21)	OSC-f1	-35	–	35	%
Normal Request Mode Timeout	NR_{TOUT}	97	150	205	ms
Delay Between SPI Command and HS1/HS2 Turn On (Note 22)	t_{S-HSon}	10	–	40	µs
Delay Between SPI Command and HS1/HS2 Turn Off (Note 22)	$t_{S-HSoff}$	10	–	48	µs
Delay Between Normal Request and Normal Mode After W/D Trigger Command	t_{S-NR2N}	15	35	70	µs
Delay Between SSB Wake-Up (SSB Low to High) and Normal Request Mode (VDD On and Reset High)	t_{w-SSB}	15	40	80	µs
Delay Between SSB Wake-Up (SSB Low to High) and First Accepted SPI Command	t_{S-SPI}	90	–	N/A	µs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{S-1STSPI}$	30	–	N/A	µs
Minimum Time Between Two Rising Edges on SSB	t_{2SSB}	15	–	–	µs

Notes

19. Delay between turn on or turn off command and high-side on or high-side off, excluding rise or fall time due to external load.
20. Guaranteed by design.
21. For information only.
22. Delay starts at falling edge of clock cycle #8 of the SPI command and start of device activation/deactivation.

MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 specification.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter (4 Channels External Available, 1 Channel Reserved for Analog Die)
SPI	SPI Module
ESCI	Standard SCI Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module (25% Accuracy with Trim Capability to 2%)

TIming Diagrams

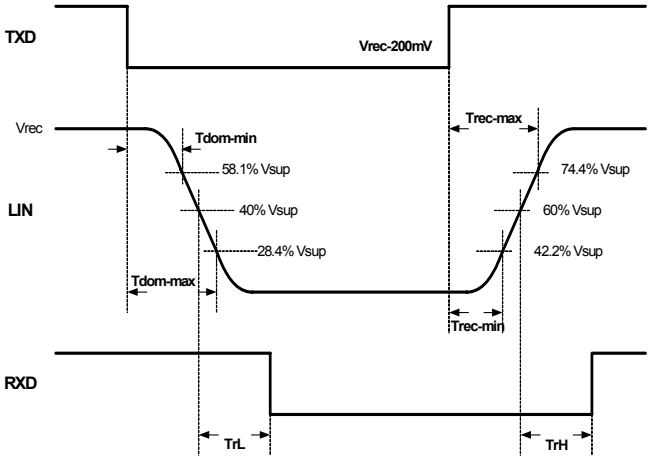


Figure 2. LIN Timing Measurements for Normal Slew Rate

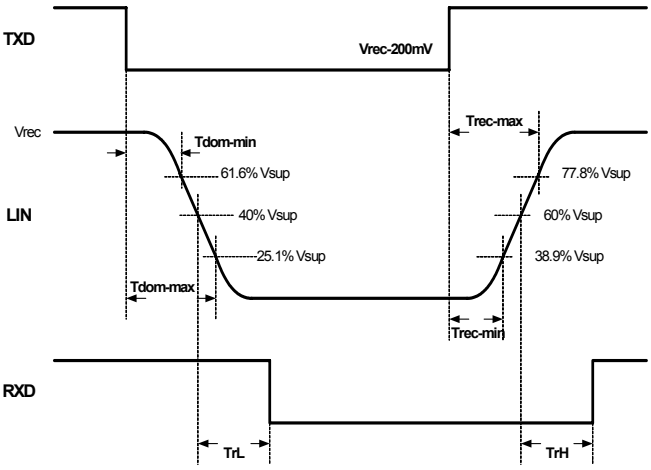


Figure 3. LIN Timing Measurements for Normal Slew Rate

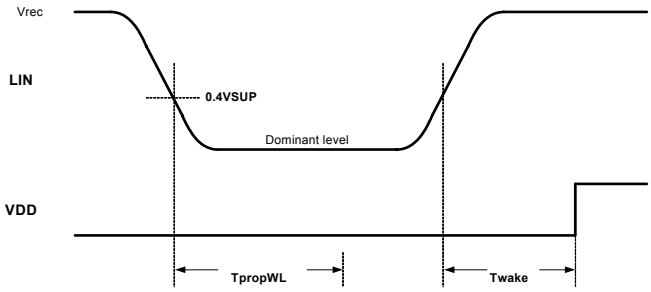


Figure 4. Wake-Up SLEEP Mode Timing

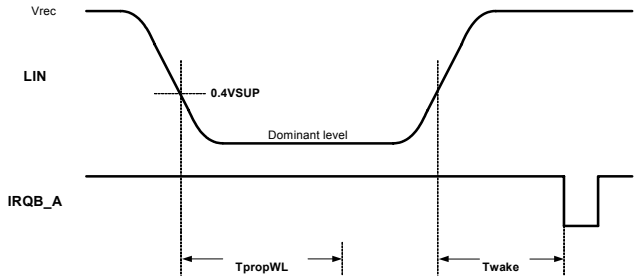


Figure 5. Wake-Up STOP Mode Timing

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

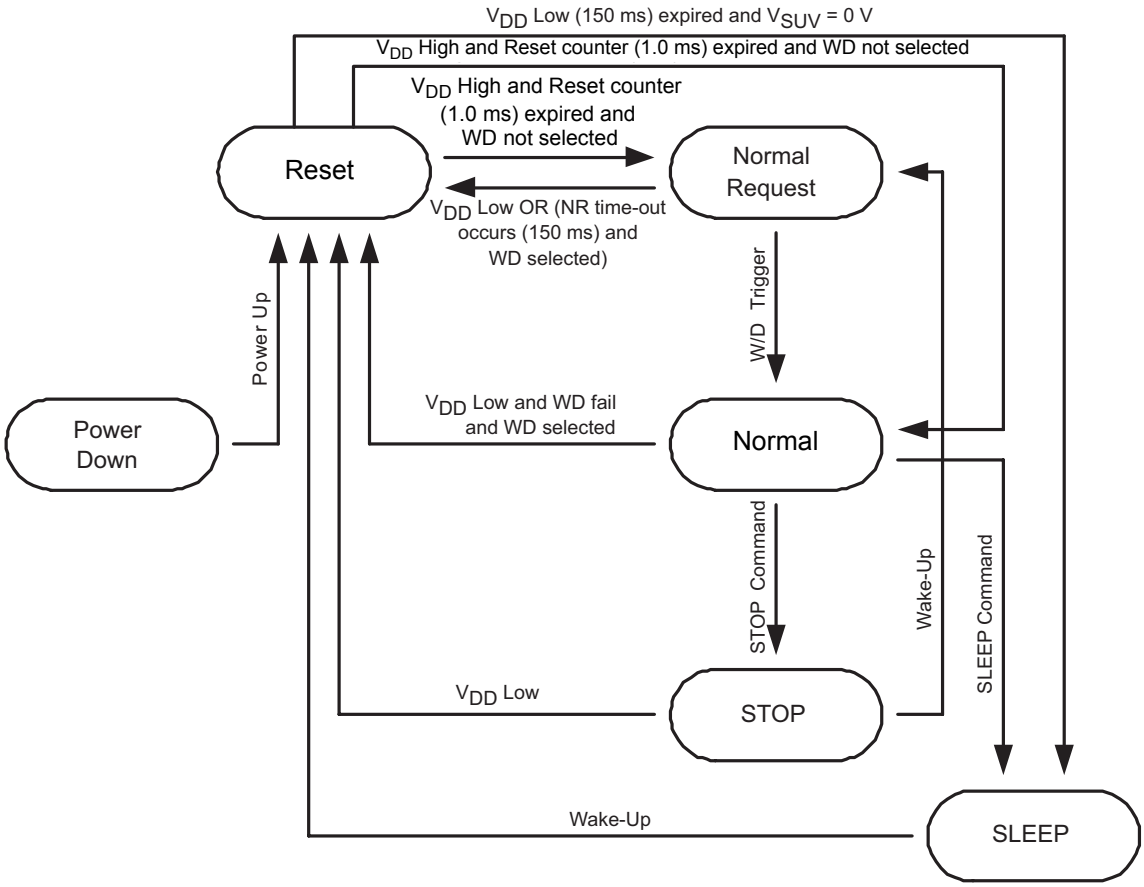
The 908E624 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E624 is well suited to perform relay control in applications like window lift, sunroof, etc., via a three-wire LIN bus.

The 908E624 combines an HC08 MCU core with flash memory together with a SmartMOS IC chip. The SmartMOS IC chip combines power and control in one chip. Power switches are provided on the SmartMOS IC configured as high-side output. Other ports are also provided, which include Operational Amplifier port and two wake-up terminals. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

STATE MACHINE DESCRIPTION

Figure 6 describes how transitions are done between the different operating modes.



WD = Watchdog
NR = Normal Request
WD selected means external resistor between WDCONF pin and GND or WDCONF pin open.
WD not selected means WDCONF pin connected to GND.
WD fail means WD trigger occurs in closed window or no SPI WD trigger command.
STOP command means STOP command sent via SPI.
SLEEP command means SPI sleep request followed by SPI SLEEP command.
Wake-up means L1 or L2 state change or LIN bus wake-up or SSB rising edge.

Figure 6. State Machine

FUNCTIONAL TERMINAL DESCRIPTION

Power Supply Terminals (VSUP1 and VSUP2)

VSUP1

This power supply terminal supplies the voltage regulator and the internal logic.

VSUP2

This power supply terminal is the positive supply for the high-side switches.

The 908E624 can be supplied from the battery line through VSUP1 and VSUP2. An external diode is required to protect against negative transients and reverse battery. It can operate from 4.5 V and under the jump start condition at 27 V DC. Device functionality is guaranteed down to 4.5 V at VSUP1 and VSUP2 terminals. These terminals sustain standard automotive voltage conditions such as load dump at 40 V.

Overvoltage and Undervoltage Pre-Warning

If the voltage at VSUP1 exceeds 20 V typical or falls below 6.0 V typical, the device generates an interrupt. VSOV or VSUV bits are set in the SPI register. Information is latched until the bit is read AND the fault has disappeared. The interrupt is not maskable.

Ground Terminal (GND)

GND is the device ground connection.

High-Side Output Terminals (HS1 and HS2)

These are two high-side switches to drive loads such as relays or lamps. They are protected against overcurrent and overtemperature and include internal clamp circuitry for inductive load drive. Control is done through SPI. PWM capability is offered through the PWMIN input.

High-Side Output HS3

This high-side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done through SPI.

LIN Bus Terminal (LIN)

This terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN Bus Specification.

Wake Up Terminals (L1 and L2)

These terminals are high-voltage inputs used to sense external switches and to wake up the device from SLEEP or STOP mode. During Normal mode the state of these terminals can be read through SPI.

Sense Amplifier E+, E-, OUT, AGND, VCC

E+, E-, and OUT are the three terminals of the current sense amplifier. In addition, the amplifier has its dedicated ground, AGND, and supply input, VCC. The operational amplifier is only operating in device Normal mode. It is not operating in SLEEP or STOP modes.

5.0 V Supply Output Terminal (VDD)

VDD is the voltage regulator output terminal. This terminal needed to place an external capacitor to stabilize the regulated output voltage. The terminal is protected against shorts to GND with an integrated current limitation (temperature shutdown could occur).

Receiver Terminal (RxD)

This terminal is the receiver terminal from the LIN physical layer. It must be connected externally to the RxD terminal of the MCU.

Interrupt Terminal (IRQB_A)

This terminal is the interrupt output terminal of the analog die. It must be connected to the IRQB terminal of the MCU.

Reset Terminal (RSTB_A)

This terminal is the reset terminal of the analog die. It must be connected to the RSTB terminal of the MCU.

Test Terminal (FLSVPP)

This is a test terminal. In the application leave this terminal open.

PWMIN Terminal

This terminal is the direct PWM input for high-side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD in order to have a high level on this input.

WDCONF Terminal

This terminal is the configuration terminal for the internal watchdog. A resistor is connected to this terminal. The resistor value defines the watchdog period. If the terminal is open, the W/D period is fixed (default value). If this terminal is tied to GND, the watchdog is disabled (for programming/debug).

Port A I/O Terminals

Port A input/output (I/O) terminals (PTA6/SS, PTA5/SPSCK, PTA4/KDB4, PTA3/KBD3, PTA2/KBD2, PTA1/KBD1, and PTA0/KBD0) are special-function, bidirectional I/O port terminals. PTA5 and PTA6 are shared with the serial peripheral interface (SPI). PTA4–PTA0 can be programmed to serve as keyboard interrupt terminals.

PTA5 is shared with the serial peripheral interface (SPI) but is not accessible in the multichip approach. This terminal is internally connected to the SPI clock of the analog die.

PTA6 is shared with the serial peripheral interface (Slave Select) but is not accessible in the multi-die approach. This terminal is internally connected to the SSB terminal of the analog die. In order to get the slave select functionality, this terminal must be used as standard output.

For details refer to the 68HC908EY16 specification.

Port B I/O Terminals

PTB7/AD7/TBCH1, PTB6/AD6/TBCH0, and PTB5/AD5–PTB0/AD0 are special-function, bidirectional I/O port terminals that can also be used for ADC inputs. PTB7/AD7/TBCH1 and PTB6/AD6/TBCH0 are special function.

PTB2 and PTB0 are not accessible in the multi-die approach.

For details refer to the 68HC908EY16 specification.

Port C I/O Terminals

PTC1/MOSI and PTC0/MISO are special-function, bidirectional I/O port terminals. PTC3/OSC2 and PTC4/OSC1 are shared with the on-chip oscillator circuit through configuration options.

For details refer to the 68HC908EY16 specification.

Depending on the application requirements:

- PTC3/OSC2 can be programmed to be OSC2.
- PTC4/OSC1 can be programmed to be OSC1.
- PTC2/MCLK is software selectable to be MCLK, or bus clock out.

PTC0 and PTC1 are not directly accessible in the multi-die approach. These terminals are internally connected to the MISO and MOSI SPI terminals of the analog die.

Port D I/O Terminals (PTD1/TACH1, PTD0/TACH0/BEMF)

PTD1/TACH1 and PTD0/TACH0 are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

Port E I/O Terminals (PTE1/RxD and PTE0/TxD)

PTE1/RxD and PTE0/TxD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TxD is internally connected to the TxD terminal of the analog die. The connection for the receiver functionality has to be done externally.

External Reset Terminal (RSTB)

A logic [0] on the RSTB terminal forces the MCU to a known startup state. RSTB is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. This terminal contains an internal pull-up resistor that is always activated, even when the reset terminal is pulled low.

For details refer to the 68HC908EY16 specification.

External Interrupt Terminal (IRQB)

IRQB is an asynchronous external interrupt terminal. This terminal contains an internal pull-up resistor that is always activated, even when the IRQB terminal is pulled low.

For details refer to the 68HC908EY16 specification.

Power Supply Terminals (EVDD and EVSS)

EVDD and EVSS are the power supply and ground terminals. The MCU operates from a single power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 specification.

Analog Power Supply/Reference Terminals (VDDA, VREFH, VSSA, and VREFL)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC).

Note VREFH is the high-reference supply for the ADC. VDDA should be tied to the same potential as VDD via separate traces. VREFL is the low-reference supply for the ADC. VSSA should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 specification.

ANALOG DIE DESCRIPTION

General Description

The 908E624 analog die is an integrated circuit dedicated to automotive applications. It includes the following functions:

- One fully protected voltage regulator with 50 mA total output current capability available at the VDD terminal
- Voltage reset function
- Configurable window watchdog function
- Interrupt output report fault or wake-up
- Wake-up from Lx wake input and LIN bus
- LIN physical interface
- Two 150 mA high-side protected switches PWM capable for relay or lamp drive
- One 50 mA high-side protected switch for Hall-effect sensor, etc.
- Operational amplifier

Operation Modes

Operating modes are controlled by the MODE1 and MODE2 bits in the SPI register. Three modes are available: Normal, STOP, and SLEEP. Operation modes are described in Table 1.

Table 1. Operation Modes

Mode	Reset	Normal Request and Normal	STOP	SLEEP
Voltage Regulator	VDD on	VDD on	VDD on. Limited current capability	VDD off. Set to 5.0 V after wake-up to enter Normal request
Wake-Up Capabilities	N/A	N/A	LIN, state change on Lx inputs, rising edge on SSB	LIN, state change on Lx inputs, rising edge on SSB
Reset Terminal (RSTB_A)	Low (1.0 ms) after VDD high	Normally high. Active low if VDD undervoltage occurs or if WD fail (if WD is enabled	Normally high. Active low if VDD undervoltage occurs	Low. Go to high after walk-up and VDD within specification
Watchdog	Not running	Running if enabled. Period selected by resistor at WDCONF terminal. WD cleared by MODE1/ MODE2 bits	Not running	Not running

Table 1. Operation Modes (continued)

Mode	Reset	Normal Request and Normal	STOP	SLEEP
HS1, HS2, HS3	OFF	ON or OFF	OFF	OFF
LIN	Recessive only	Tx/Rx	Recessive state with wake capability	Recessive state with wake capability

To safely enter SLEEP or STOP mode and to ensure that these modes are not affected by noise issue during SPI transmission, a dedicated sequence must be send twice:

Enter SLEEP Mode

Two identical SPI commands with:

D6 = 1, D7 = 1: for low-power (SLEEP or STOP) request.

D5: “1” for LIN pull-up disabled or “0” for pull-up enabled.

D1 = 0, D0 = 0: for SLEEP mode.

Enter STOP Mode

Two identical SPI commands with:

D6 = 1, D7 = 1: for low-power (SLEEP or STOP) request.

D5: “1” for LIN pull-up disabled or “0” for pull-up enabled.

D1 = 0, D0 = 1: for STOP mode.

SLEEP or STOP mode is entered after the second SPI command.

Interrupts

The IRQB_A terminal is used to report a fault to the MCU. An interrupt pulse is generated in case of any of the following: VDD regulator temperature pre-warning, high-side switch 1, 2, or 3 thermal shutdown, V_{SUP} overvoltage (19.25 V typ), and V_{SUP} undervoltage (6.0 V typ).

This terminal reports to the MCU the L1, L2, or LIN bus wake-up event when the product is in STOP mode.

After an Interrupt or a wake-up, the register bit INT SOURCE is set, indicating the source of the event. The SPI data register will be transferred once.

High-Side Outputs

High-Side Output Terminals HS1 and HS2

These are two high-side switches to drive load such as relays or lamps. They are protected against over current and over temperature and include internal clamp circuitry for inductive load drive. Control is done through SPI. PWM capability is offered through the PWMIN input.

If PWM control is required, the internal circuitry which drive the internal high-side switch is an AND function between the SPI bit HS1 (or HS2) and the PWMIN input. In order to have HS1 on PWMIN must be high and bit HS1 must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD terminal.

If overtemperature occurs on any of the three high-side switches, the faulty switch is turned off and latched off until the HS1 (or HS2 or HS3) bit is set to “1” in the SPI register. The failure is reported through SPI by HSST bit.

High-Side Output HS3

This high-side switch can be used to drive small lamps, Hall-effect sensors, or switch pull-up resistors. Control is done through SPI. No PWM control is possible on this terminal.

Window Watchdog

The window watchdog is configurable using the external resistor at the WDCONF terminal. The watchdog is cleared through an SPI write operation (MODE1 and MODE2 bit). If the WDCONF terminal is left open, a fixed watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF terminal must be connected to GND. The watchdog period is calculated using the following formula:

$$Twd\ [ms] = 0.991 * R\ [k\Omega] + 0.648$$

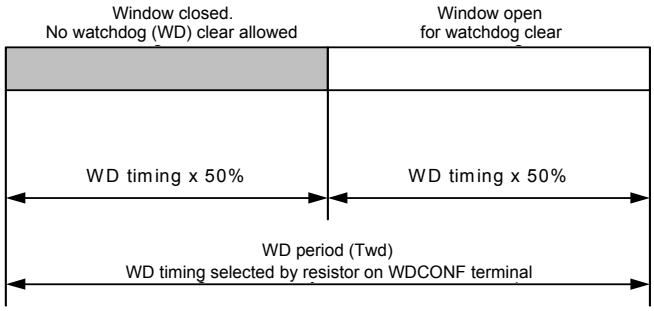


Figure 7. Window Watchdog Operation

The watchdog is cleared by an SPI write to the MODE1 and MODE2 bits (refer to Table 2).

Table 2. Mode Selection Bits

MODE2	MODE1	Description
0	0	SLEEP mode (Note 23)
0	1	STOP mode
1	0	Normal mode + watchdog clear (Note 24)
1	1	Normal mode

Notes

23. Special SPI command and sequence is implemented in order to avoid to go into SLEEP or STOP mode with a single 8-bit SPI command.
24. When a zero is written to MODE1 bit while MODE2 bit is written as a one, after the SPI command is completed MODE1 bit is set to one and product stays in Normal mode. In order to set the product in SLEEP mode, both MODE1 and MODE2 bits must be written in the same 8-bit SPI command.

The watchdog clear on Normal request mode (150 ms) has no window.

SPI Interface and Register Description

The SPI is an 8-bit SPI. All bits are in a one-data byte. The MSB (bit 7) is send first (see Figure 8). The minimum time between two rising edges on the SSB terminal is 15 μs.

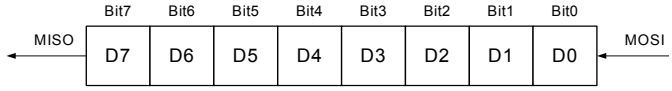


Figure 8. Data Format Description

During an SPI communication, the state of MISO reports the state of the product at time of SSB high-to-low transitions. The status flag is latched at SSB high-to-low transitions.

The following tables describe the SPI register bit meaning, reset value, and bit reset condition.

Table 3. SPI Register Overview

		D7	D6	D5	D4	D3	D2	D1	D0
SPI Register	W	LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
	R	INT SOURCE	LINWU or LINFAIL	VSOV	VSUV BATFAIL (Note 25)	VDDT	HSST	L2	L1
Write Reset Value		0	0	0	0	0	0	–	–
Write Reset Condition		POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	–	–

Notes

25. The first SPI read after reset returns the BATFAIL flag state on bit D4. D7 signals INT SOURCE.

Table 4. Control Bits Function (Write Operation)

D7	D6	D5	D4	D3	D2	D1	D0
LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1

Table 5. Control Bits Function (Read Operation)

D7	D6	D5	D4	D3	D2	D1	D0
INT SOURCE	LINWU or LINFAIL	VSOV	VSUV BATFAIL	VDDT	HSST	L2	L1

HSxON—High-Side x Enable Bit

This bit enables HSx. Reset clears the HSx bit.

- 1 = HSx switched on (refer to Note below).
- 0 = HSx switched off.

Note If no PWM on HS1 and HS2 is required, the PWMIN terminal must be connected to the VDD terminal.

LIN-PU—LIN Pull-UP Enable Bit

This bit controls the LIN pull-up resistor during SLEEP and STOP modes.

- 1 = Pull-up disconnected in SLEEP and STOP modes.
- 0 = Pull-up connected in SLEEP and STOP modes.

Note This bit is only available on the final product. All versions before MC-Qualification will not include this function.

LINSL1 and LINSL2—LIN Baud Rate and Low-Power Mode Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 6. Reset clears the LINSL1 and LINSL2 bits.

Table 6. LIN Baud Rate and Low-Power Mode Selection Bits

LINSL2	LINSL1	Description
0	0	Baud Rate up to 20 kbps (normal)
0	1	Baud Rate up to 10 kbps (slow)
1	0	Fast Program Download Baud Rate up to 100 kbps
1	1	Low-Power Mode (SLEEP or STOP) Request

L1—Input L1 Status Flag Bit

This flag reflects the status of the L1 input terminal and indicates the wake-up source.

- 1 = L1 input high or wake-up by L1 (first register read after wake-up indicated with INT SOURCE = 1).
- 0 = L1 input low.

L2—Input L2 Status Flag Bit

This flag reflects the status of the L2 input terminal and indicates the wake-up source.

- 1 = L2 input high or wake-up by L2 (first register read after wake-up indicated with INT SOURCE = 1).
- 0 = L2 input low.

HSST—High-Side Status Flag Bit

This flag is set on overtemperature conditions on one of the high-side outputs.

- 1 = HSx off due to overtemperature.
- 0 = No overtemperature.

VDDT—Voltage Regulator Status Flag Bit

This flag is set as pre-warning in case of an over-temperature condition on the voltage regulator.

- 1 = Voltage regulator overtemperature condition, pre-warning.
- 0 = No overtemperature detected.

VSUV/BATFAIL—Undervoltage Status Flag Bit

This flag is set on a V_{SUP} undervoltage condition.

- 1 = Undervoltage detected. V_{SUP} below 6.0 V
- 0 = No undervoltage detected. V_{SUP} above 6.0 V.

VSOV—Overvoltage Status Flag Bit

This flag is set on a V_{SUP} overvoltage condition.

- 1 = Overvoltage detected, V_{SUP} above 19 V.
- 0 = No overvoltage detected, V_{SUP} below 18 V.

LINWU/LINFAIL—LIN Status Flag Bit

This bit indicates a LIN wake-up condition.

- 1 = LIN bus wake-up occurred or LIN over- current/ temperature occurred.
- 0 = No LIN bus wake-up occurred.

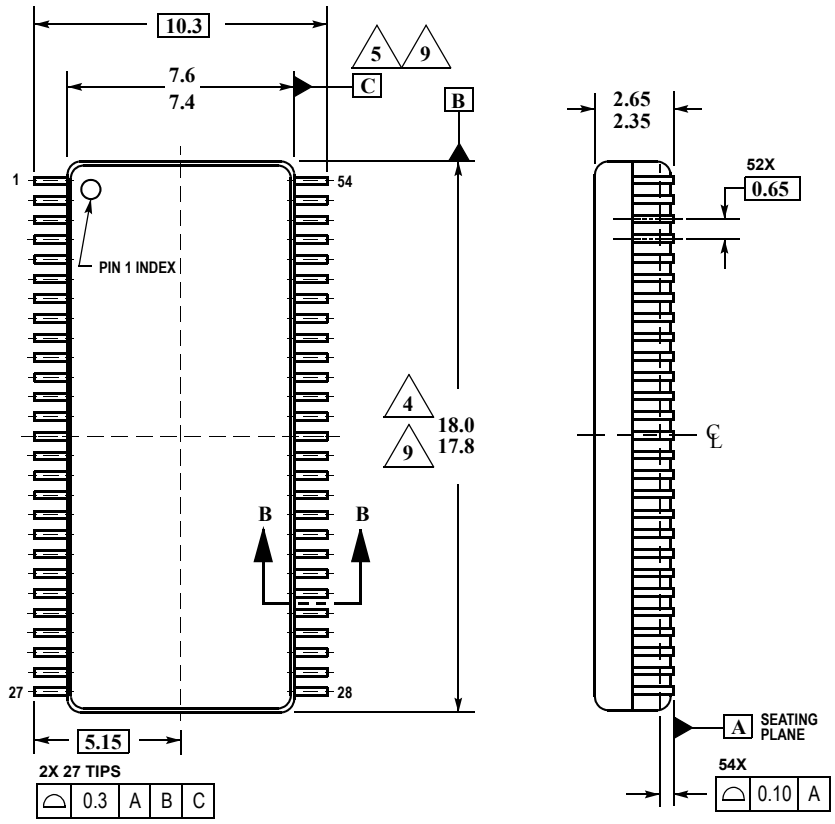
INT SOURCE—Register Content Flags or Interrupt

This bit indicates if the register contents reflect the flags or the wake-up source.

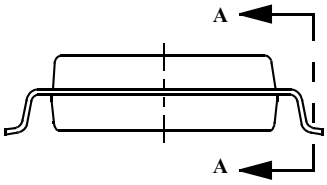
- 1 = SPI word reflects the interrupt or wake-up source.
- 0 = No interrupt occurred. Other SPI bits report real time status.

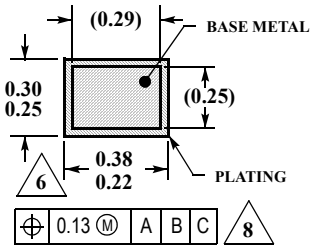
PACKAGE DIMENSIONS

DWB SUFFIX
54-TERMINAL SOIC WIDE BODY
PLASTIC PACKAGE
CASE 1365-01
ISSUE O

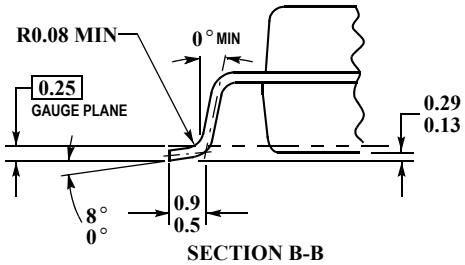


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.





SECTION A-A
ROTATED 90° CLOCKWISE



SECTION B-B

HOW TO REACH US:
USA/EUROPE/LOCATIONS NOT LISTED: Motorola Literature Distribution: P.O. Box 5405, Denver, Colorado 80217.
1-303-675-2140 or 1-800-441-2447
JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1 Minami-Azabu. Minato-ku, Tokyo 106-8573 Japan.
81-3-3440-3569
ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tao Po, N.T.,
Hong Kong. 852-26668334
TECHNICAL INFORMATION CENTER: 1-800-521-6274