Advance Information

Integrated Quad Half H-Bridge with Power Supply, Embedded MCU, and LIN Serial Communication

The 908E625 is an integrated single-package solution that includes a high-performance HC08 microcontroller with a *SMARTMOS*™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI), and an internal clock generator (ICG) module. The analog control die provides fully protected H-Bridge/high-side outputs, voltage regulator, autonomous watchdog with cyclic wake-up, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well suited for the control of automotive mirror, door lock, and light-levelling applications.

Features

- High-Performance M68HC08EY16 Core
- 16 K Bytes of On-Chip Flash Memory
- 512 Bytes of RAM
- Internal Clock Generation Module
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter
- Three 2-Terminal Hall-Effect Sensor Input Ports
- One Analog Input with Switchable Current Source
- Four Low $R_{DS(ON)}$ Half-Bridge Outputs
- One Low $R_{DS(ON)}$ High-Side Output
- 13 Microcontroller I/Os

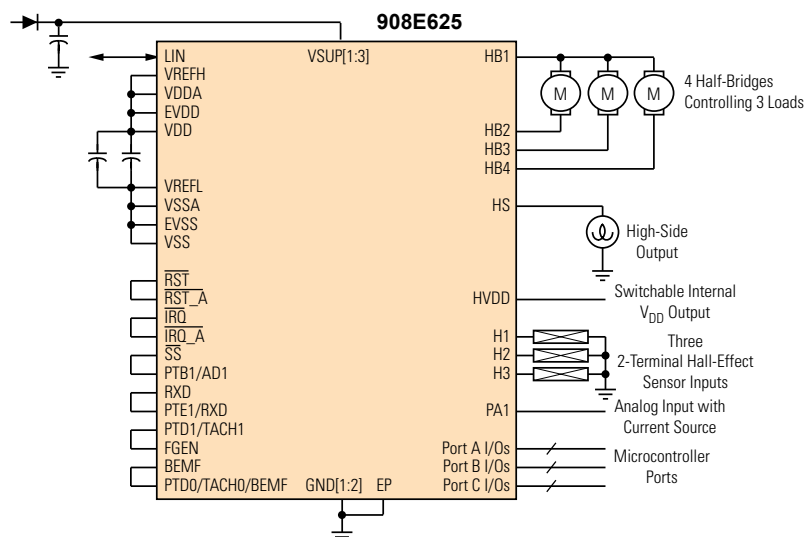**908E625**

H-BRIDGE POWER SUPPLY WITH EMBEDDED MCU AND LIN
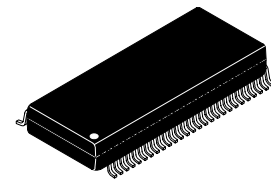
**DWB SUFFIX
CASE 1400-01
54-TERMINAL SOICWB-EP**

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MM908E625ACDWB/R2	-40°C to 85°C	54 SOIC WB-EP

908E625 Simplified Application Diagram

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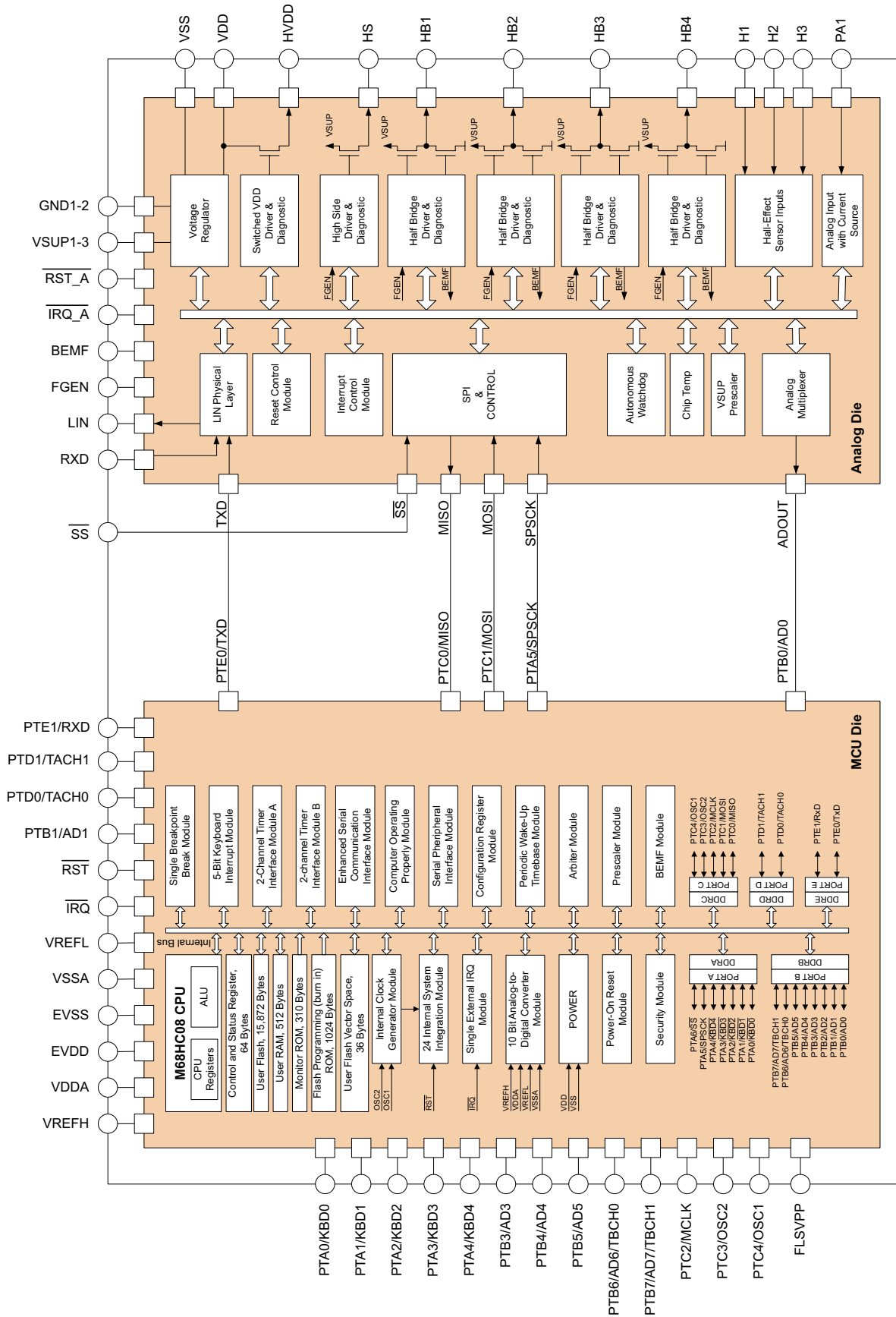
Figure 1. 908E625 Simplified Internal Block Diagram

**Transparent Top
View of Package**

PTB7/AD7/TBCH1	1 ●	54	PTA0/KBD0
PTB6/AD6/TBCH0	2	53	PTA1/KBD1
PTC4/OSC1	3	52	PTA2/KBD2
PTC3/OSC2	4	51	FLSVPP
PTC2/MCLK	5	50	PTA3/KBD3
PTB5/AD5	6	49	PTA4/KBD4
PTB4/AD4	7	48	VREFH
PTB3/AD3	8	47	VDDA
$\overline{IRQ}$	9	46	EVDD
$\overline{RST}$	10	45	EVSS
PTB1/AD1	11	44	VSSA
PTD0/TACH0/BEMF	12	43	VREFL
PTD1/TACH1	13	42	PTE1/RXD
NC	14	41	RXD
FGEN	15	40	VSS
BEMF	16	39	PA1
$\overline{RST\_A}$	17	38	VDD
$\overline{IRQ\_A}$	18	37	H1
$\overline{SS}$	19	36	H2
LIN	20	35	H3
NC	21	34	HVDD
NC	22	33	NC
HB1	23	32	HB4
VSUP1	24	31	VSUP3
GND1	25	30	GND2
HB2	26	29	HB3
VSUP2	27	28	HS

(Exposed Pad — center)

TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section beginning on page 15.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	9	$\overline{IRQ}$	External Interrupt Input	This terminal is an asynchronous external interrupt input terminal.
MCU	10	$\overline{RST}$	External Reset	This terminal is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0/BEMF PTD1/TACH1	Port D I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
–	14, 21, 22, 33	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This terminal is a special-function, bidirectional I/O port terminal that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These terminals are the reference voltage terminals for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Terminals	These terminals are the power supply terminals for the analog-to-digital converter.

TERMINAL DEFINITIONS (continued)

A functional description of each terminal can be found in the System/Application Information section beginning on page 15.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	45 46	EVSS EVDD	MCU Power Supply Terminals	These terminals are the ground and power supply terminals, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Terminal	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input terminal for the half-bridge current limitation and the high-side inrush current limiter PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This terminal gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This terminal is the bidirectional reset terminal of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This terminal is the interrupt output terminal of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This terminal is the SPI slave select terminal for the analog chip.
Analog	20	LIN	LIN Bus	This terminal represents the single-wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-Bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high-side and low-side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Terminals	These terminals are device power supply terminals.
Analog	25 30	GND1 GND2	Power Ground Terminals	These terminals are device power ground connections.
Analog	28	HS	High-Side Output	This output terminal is a low $R_{DS(ON)}$ high-side switch.
Analog	34	HVDD	Switchable V_{DD} Output	This terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-terminal Hall-effect sensors.
Analog	35 36 37	H3 H2 H1	Hall-Effect Sensor Inputs	These terminals provide inputs for Hall-effect sensors and switches.
Analog	38	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output terminal is intended to supply the embedded microcontroller.
Analog	39	PA1	Analog Input	This terminal is an analog input port with selectable source values.
Analog	40	VSS	Voltage Regulator Ground	Ground terminal for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This terminal is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board.

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MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-State)	$V_{SUP(SS)}$	-0.3 to 28	
Analog Chip Supply Voltage under Transient Conditions (Note 1)	$V_{SUP(PK)}$	-0.3 to 40	
Microcontroller Chip Supply Voltage	V_{DD}	-0.3 to 6.0	
Input Terminal Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to 5.5	
Microcontroller Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum Microcontroller Current per Terminal			mA
All Terminals Except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
Terminals PTA0:PTA6, PTC0:PTC1	$I_{PIN(2)}$	±25	
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage			V
Normal Operation (Steady-State)	$V_{BUS(SS)}$	-18 to 28	
Transient Conditions (Note 1)	$V_{BUS(DYNAMIC)}$	40	
ESD Voltage			V
Human Body Model (Note 2)	V_{ESD1}	±3000	
Machine Model (Note 3)	V_{ESD2}	±150	
Charge Device Model (Note 4)	V_{ESD3}	±500	

THERMAL RATINGS

Rating	Symbol	Value	Unit
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Case Temperature (Note 5)	T_C	-40 to 85	°C
Operating Junction Temperature			°C
Analog	$T_{J(ANALOG)}$	-40 to 150	
MCU	$T_{J(MCU)}$	-40 to 125	
Terminal Soldering Temperature (Note 6)	T_{SOLDER}	245	°C
Thermal Resistance (Junction to Ambient)			°C/W
All Outputs ON (Note 7), (Note 9)	$R_{\theta JA1}$	24	
Single Output ON (Note 8), (Note 9)	$R_{\theta JA2}$	27	

Notes
1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0 pF).
5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
7. All outputs ON and dissipating equal power.
8. One output ON and dissipating power.
9. Per JEDEC JESD51-2 at natural convection, still air condition; and 2s2p thermal test board per JEDEC JESD51-7 and JESD51-5 (thermal vias connected to top ground plane).

STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\ V \le V_{SUP} \le 16\ V$, $-40°C \le T_J \le 125°C$ unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode	I_{RUN}				mA
$\quad V_{SUP}$ = 12 V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled		–	20	–	
STOP Mode (Note 10)	I_{STOP}				μA
$\quad V_{SUP}$ = 12 V, Cyclic Wake-Up Disabled		–	–	60	
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Terminals $\overline{RST\_A}$, $\overline{IRQ\_A}$					V
$\quad$ Low-State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
$\quad$ High-State Output Voltage (I_{OUT} = 1.0 μA)	V_{OH}	3.85	–	–	
Output Terminals BEMF, RXD					V
$\quad$ Low-State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	–	–	0.4	
$\quad$ High-State Output Voltage (I_{OUT} = 1.5 mA)	V_{OH}	3.85	–	–	
Output Terminal RXD–Capacitance (Note 11)	C_{IN}	–	4.0	–	pF
Input Terminals $\overline{RST\_A}$, FGEN, $\overline{SS}$					V
$\quad$ Input Logic Low Voltage	V_{IL}	–	–	1.5	
$\quad$ Input Logic High Voltage	V_{IH}	3.5	–	–	
Input Terminals $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance (Note 11)	C_{IN}	–	4.0	–	pF
Terminals $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pullup Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Terminal $\overline{SS}$–Pullup Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Terminals FGEN, MOSI, SPSCK–Pulldown Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Terminal TXD–Pullup Current Source	I_{PULLUP}	–	35	–	μA

Notes

10. STOP mode current will increase if V_{SUP} exceeds 15 V.

11. This parameter is guaranteed by process monitoring but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\leq$ V$_{SUP}$ $\leq$ 16 V, -40°C $\leq$ T$_J$ $\leq$ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T$_A$ = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
High-Voltage Reset					V
Threshold	V$_{HVRON}$	27	30	33	
Hysteresis	V$_{HVRH}$	–	1.5	–	
Low-Voltage Reset					V
Threshold	V$_{LVRON}$	3.6	4.0	4.5	V
Hysteresis	V$_{LVRH}$	–	100	–	mV
High-Voltage Interrupt					V
Threshold	V$_{HVION}$	17.5	21	23	
Hysteresis	V$_{HVIH}$	–	1.0	–	
Low-Voltage Interrupt					V
Threshold	V$_{LVION}$	6.5	–	8.0	
Hysteresis	V$_{LVIH}$	–	0.4	–	
High-Temperature Reset (Note 12)					°C
Threshold	T$_{RON}$	–	170	–	
Hysteresis	T$_{RH}$	5.0	–	–	
High-Temperature Interrupt (Note 13)					°C
Threshold	T$_{ION}$	–	160	–	
Hysteresis	T$_{IH}$	5.0	–	–	
VOLTAGE REGULATOR					
Normal Mode Output Voltage I$_{OUT}$ = 60 mA, 6.0 V < V$_{SUP}$ < 18 V	V$_{DDRUN}$	4.75	5.0	5.25	V
Load Regulation I$_{OUT}$ = 80 mA, V$_{SUP}$ = 9.0 V, T$_J$ = 125°C	V$_{LR}$	–	–	100	mV
STOP Mode Output Voltage (Maximum Output Current 100 µA)	V$_{DDSTOP}$	4.5	4.7	4.9	V

Notes
12. This parameter is guaranteed by process monitoring but is not production tested.
13. High-Temperature Interrupt (HTI) threshold is linked to High-Temperature Reset (HTR) threshold (HTR = HTI + 10°C).

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\ V \leq V_{SUP} \leq 16\ V$, $-40°C \leq T_J \leq 125°C$ unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500 Ω Pullup to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0 µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pullup Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5 V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_rec}$	0	–	20	µA

Leakage Current to GND (V_{SUP} Disconnected)
   Including Internal Pullup Resistor, V_{LIN} @ -18 V
   Including Internal Pullup Resistor, V_{LIN} @ +18 V
	$I_{BUS\_NO\_GND}$
	I_{BUS}
		–
		–
			-600
			25
				–
				–
					µA

LIN Receiver
   Recessive
   Dominant
   Threshold
   Input Hysteresis
	V_{IH}
	V_{IL}
	V_{ITH}
	V_{IHY}
		0.6 V_{LIN}
		0
		–
		0.01 V_{SUP}
			–
			–
			V_{SUP}/2
			–
				V_{SUP}
				0.4 V_{LIN}
				–
				0.1 V_{SUP}
					V

LIN Wake-Up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HIGH-SIDE OUTPUT (HS)					
Switch ON Resistance @ T_J = 25°C with I_{LOAD} = 1.0 A	$R_{DS(ON)HS}$	–	600	700	mΩ
High-Side Overcurrent Shutdown	I_{HSOC}	3.9	–	7.0	A

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STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\leq V_{SUP} \leq$ 16 V, -40°C $\leq T_J \leq$ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HALF-BRIDGE OUTPUTS (H1:H4)					
Switch ON Resistance @ T_J = 25°C with I_{LOAD} = 1.0 A High Side Low Side	 $R_{DS(ON)HB\_HS}$ $R_{DS(ON)HB\_LS}$	 – –	 425 400	 500 500	mΩ
High-Side Overcurrent Shutdown	I_{HBHSOC}	4.0	–	7.5	A
Low-Side Overcurrent Shutdown	I_{HBLSOC}	3.5	–	7.5	A
Low-Side Current Limitation @ T_J = 25°C Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1) Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0) Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1) Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0) Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	 I_{CL1} I_{CL2} I_{CL3} I_{CL4} I_{CL5}	 – 210 300 450 600	 55 260 370 550 740	 – 315 440 650 880	mA
Half-Bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0	V
Half-Bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low-Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A]) CSA = 1 CSA = 0	 $RATIO_H$ $RATIO_L$	 7.0 1.0	 12.0 2.0	 14.0 3.0	V/A
SWITCHABLE V_{DD} OUTPUT (HVDD)					
Overcurrent Shutdown Threshold	$I_{HVDDOCT}$	24	30	40	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT})	$RATIO_{VSUP}$	4.8	5.1	5.35	–
INTERNAL DIE TEMPERATURE SENSOR					
Voltage/Temperature Slope	S_{TtoV}	–	19	–	mV/°C
Output Voltage @ 25°C	V_{T25}	1.7	2.1	2.5	V
HALL-EFFECT SENSOR INPUTS (H1:H3)					
Output Voltage V_{SUP} < 16.2 V V_{SUP} > 16.2 V	 V_{HALL1} V_{HALL2}	 – –	 V_{SUP}-1.2 –	 – 15	V
Sense Current Threshold Hysteresis	 I_{HSCT} I_{HSCH}	 6.9 –	 8.8 0.88	 11 –	mA
Output Current Limitation	I_{HL}	–	90	–	mA
Overcurrent Warning HP_OCF Flag Threshold]	V_{HPOCT}	–	3.0	–	V
Dropout Voltage @ I_{LOAD} = 15 mA	V_{HPDO}	–	0.5	–	V

STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V $\leq$ V_{SUP} $\leq$ 16 V, -40°C $\leq$ T_J $\leq$ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUT (PA1)					
Current Source PA1 CSSEL1 = 1, CSSEL0 = 1	I_{CSPA1}	570	670	770	μA

Selectable Scaling Factor Current Source PA1 (I(N) = I_{CSPA1}* N)
    CSSEL1 = 0, CSSEL0 = 0
    CSSEL1 = 0, CSSEL0 = 1
    CSSEL1 = 1, CSSEL0 = 0
	$N_{CSPA1-0}$
	$N_{CSPA1-1}$
	$N_{CSPA1-2}$
		8.5
		28.5
		58.5
			10
			30
			60
				11.5
				31.5
				61.5
					%

DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions $9.0\ V \leq V_{SUP} \leq 16\ V$, $-40°C \leq T_J \leq 125°C$ unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Propagation Delay (Note 14), (Note 15)					µs
TXD LOW to LIN LOW	$t_{TXD-LIN-low}$	–	–	6.0	
TXD HIGH to LIN HIGH	$t_{TXD-LIN-high}$	–	–	6.0	
LIN LOW to RXD LOW	$t_{LIN-RXD-low}$	–	4.0	8.0	
LIN HIGH to RXD HIGH	$t_{LIN-RXD-high}$	–	4.0	8.0	
TXD Symmetry	$t_{TXD-SYM}$	-2.0	–	2.0	
RXD Symmetry	$t_{RXD-SYM}$	-2.0	–	2.0	
Output Falling Edge Slew Rate (Note 14), (Note 16)	SR_F				V/µs
80% to 20%		-1.0	-2.0	-3.0	
Output Rising Edge Slew Rate (Note 14), (Note 16)	SR_R				V/µs
20% to 80%, $R_{BUS} > 1.0\ k\Omega$, $C_{BUS} < 10\ nF$		1.0	2.0	3.0	
LIN Rise/Fall Slew Rate Symmetry (Note 14), (Note 16)	SR_S	-2.0	–	2.0	µs
HALL-EFFECT SENSOR INPUTS (H1:H3)					
Propagation Delay	t_{HPPD}	–	1.0	–	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 t_{OSC}	t_{AWDPH}	16	22	28	ms
AWD Period High = 256 t_{OSC}	t_{AWDPL}	8.0	11	14	ms
AWD Cyclic Wake-Up On Time	$t_{AWDHPON}$	–	90	–	µs

Notes

14. All LIN characteristics are for initial LIN slew rate selection (20 kBaud) (SRS0:SRS1= 00).
15. See Figure 2, page 11.
16. See Figure 3, page 11.

MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with Two Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module (25% Accuracy with Trim Capability to 2%)
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

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MOTOROLA ANALOG INTEGRATED CIRCUIT DEVICE DATA
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Timing Diagrams

$t_{TXD-LIN-low}$ $t_{TXD-LIN-high}$

TXD

LIN

Recessive State — 0.9 V_{SUP} **Recessive State**

— 0.6 V_{SUP}

0.4 V_{SUP} —

0.1 V_{SUP}

Dominant State

RXD

$t_{LIN-RXD-low}$ $t_{LIN-RXD-high}$
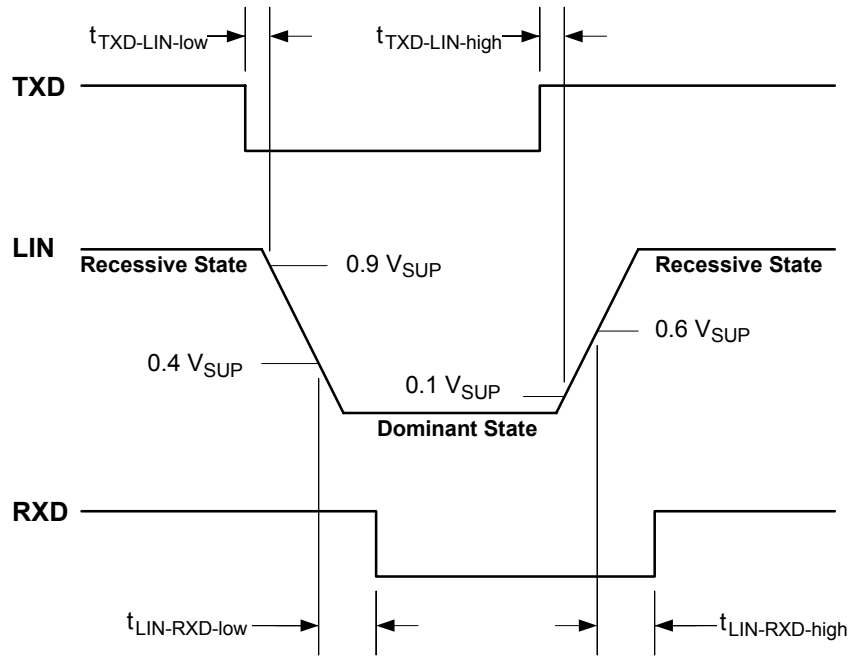
Figure 2. LIN Timing Description

Δt Fall-time Δt Rise-time

0.8 V_{SUP} 0.8 V_{SUP}

ΔV Fall ΔV Rise

0.2 V_{SUP} 0.2 V_{SUP}

Dominant State

$$SR_F = \frac{\Delta V \text{ Fall}}{\Delta t \text{ Fall-time}}$$

$$SR_R = \frac{\Delta V \text{ Rise}}{\Delta t \text{ Rise-time}}$$
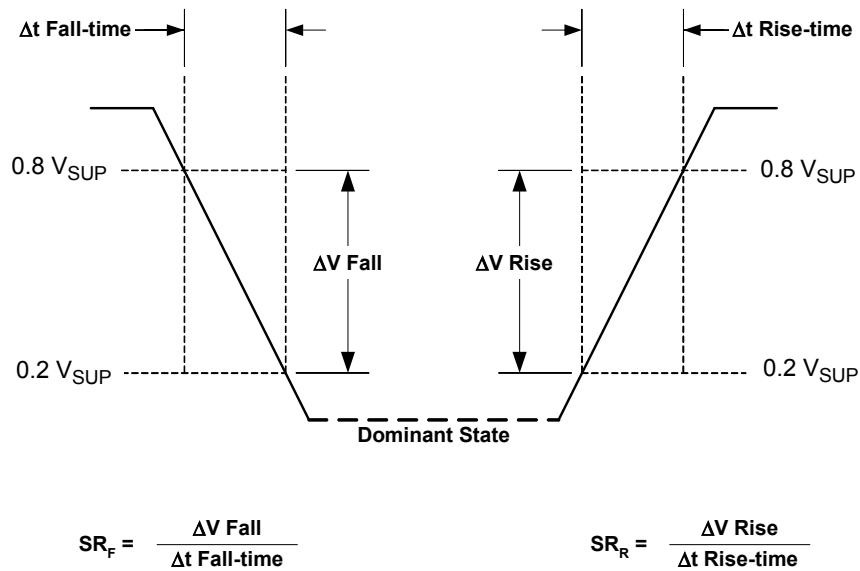
Figure 3. LIN Slew Rate Description

Functional Diagrams
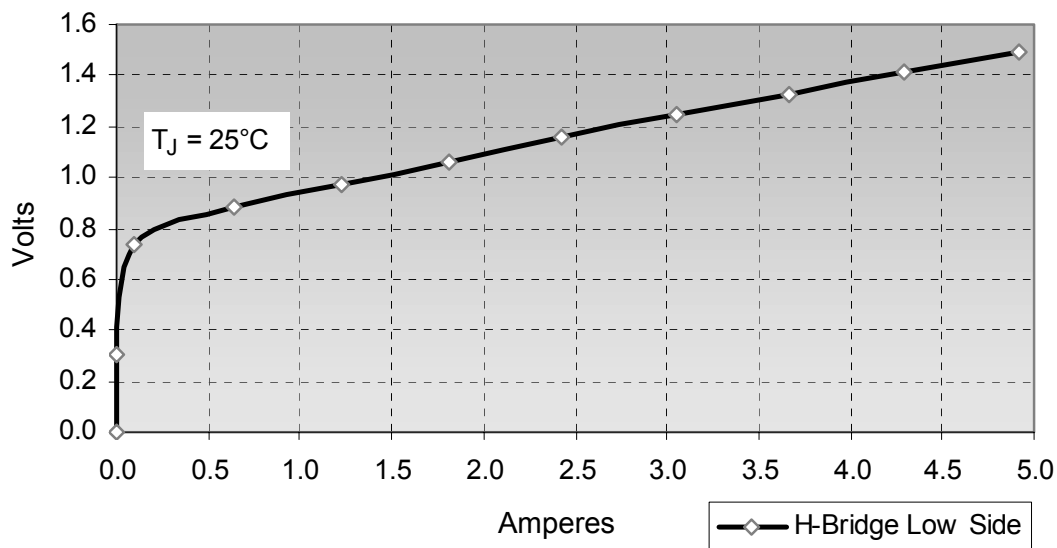
Figure 4. Free Wheel Diode Forward Voltage
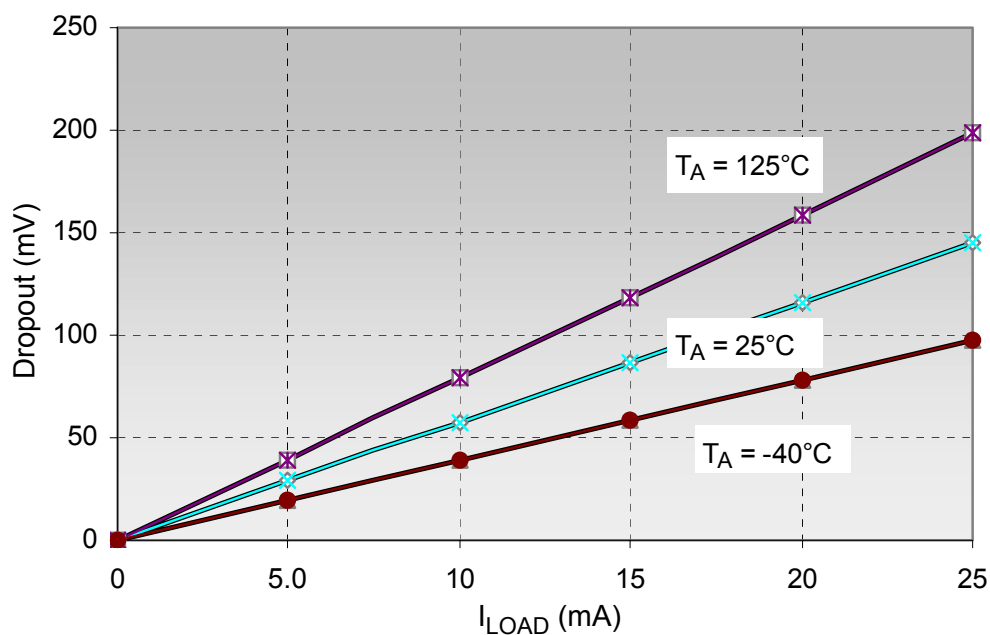
Figure 5. Dropout Voltage on HVDD

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 908E625 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E625 is well suited to perform complete mirror, door lock, and light-levelling control all via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as half-bridge outputs with one

high-side switch. Other ports are also provided; they include Hall-effect sensor input ports, analog input ports, and a selectable HVDD terminal. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL TERMINAL DESCRIPTION

See for a graphic representation of the various terminals referred to in the following paragraphs. Also, see the terminal diagram on for a depiction of the terminal locations on the package.

Port A I/O Terminals

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt terminals, KBD0:KBD4.

The PTA5/SPSCK terminal is not accessible in this device and is internally connected to the SPI clock terminal of the analog die. The PTA6/$\overline{SS}$ terminal is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

Port B I/O Terminals

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. All terminals are shared with the ADC module. The PTB6:PTB7 terminals are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT terminal of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc. The PTB2/AD2 terminal is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

Port C I/O Terminals

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI terminals of the analog die.

For details refer to the 68HC908EY16 datasheet.

Port D I/O Terminals

PTD1/TACH1 and PTD0/TACH0/BEMF are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

In step motor applications the PTD0 terminal should be connected to the BEMF output of the analog die in order to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 terminal is recommended for use as an output terminal for generating the FGEN signal (PWM signal) if required by the application.

Port E I/O Terminal

PTE1/RXD and PTE0/TXD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD terminal of the analog die. The connection for the receiver must be done externally.

External Interrupt Terminal ($\overline{IRQ}$)

The $\overline{IRQ}$ terminal is an asynchronous external interrupt terminal. This terminal contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

External Reset Terminal ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ terminal forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This terminal contains an internal pullup resistor that is always activated, even when the reset terminal is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

Current Limitation Frequency Input Terminal (FGEN)

Input terminal for the half-bridge current limitation and the high-side inrush current limiter PWM frequency. This input is not a real PWM input terminal; it should just supply the period of the PWM. The duty cycle will be generate automatically.

Important The recommended FGEN frequency should be in the range of 0.1 kHz to 20 kHz.

Back Electromagnetic Force Output Terminal (BEMF)

This terminal gives the user information about back electromagnetic force (BEMF). This feature is mainly used in step motor applications for detecting a stalled motor. In order to evaluate this signal the terminal must be directly connected to terminal PTD0/TACH0/BEMF.

Reset Terminal ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset terminal of the analog die. It is an open drain with pullup resistor and must be connected to the $\overline{\text{RST}}$ terminal of the MCU.

Interrupt Terminal ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output terminal of the analog die indicating errors or wake-up events. It is an open drain with pullup resistor and must be connected to the $\overline{\text{IRQ}}$ terminal of the MCU.

Slave Select Terminal ($\overline{\text{SS}}$)

This terminal is the SPI Slave Select terminal for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN Bus Terminal (LIN)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

Half-Bridge Output Terminals (HB1:HB4)

The 908E625 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high-side and low-side switches.

The HB1:HB4 outputs are short-circuit and overtemperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low-side MOSFETs.

Power Supply Terminals (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply terminals. The nominal input voltage is designed for operation from 12 V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high-side output driver, multiple VSUP terminals are provided.

All VSUP terminals must be connected to get full chip functionality.

Power Ground Terminals (GND1 and GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs and high-side output driver, multiple terminals are provided.

GND1 and GND2 terminals must be connected to get full chip functionality.

High-Side Output Terminal (HS)

The HS output terminal is a low $R_{DS(ON)}$ high-side switch. The switch is protected against overtemperature and overcurrent. The output is capable of limiting the inrush current with an automatic PWM generation using the FGEN module.

Switchable V_{DD} Output Terminal (HVDD)

The HVDD terminal is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0 V supply; e.g., 3-terminal Hall-effect sensors. The output is short-circuit protected.

Hall-Effect Sensor Input Terminals (H1:H3)

The Hall-effect sensor input terminals H1:H3 provide inputs for Hall-effect sensors and switches.

+5.0 V Voltage Regulator Output Terminal (VDD)

The VDD terminal is needed to place an external capacitor to stabilize the regulated output voltage. The VDD terminal is intended to supply the embedded microcontroller.

Important The VDD terminal should not be used to supply other loads; use the HVDD terminal for this purpose. The VDD, EVDD, VDDA, and VREFH terminals must be connected together.

Analog Input Terminal (PA1)

This terminal is an analog input port with selectable current source values.

Voltage Regulator Ground Terminal (VSS)

The VSS terminal is the ground terminal for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL terminals must be connected together.

LIN Transceiver Output Terminal (RXD)

This terminal is the output of LIN transceiver. The terminal must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD terminal).

908E625
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MOTOROLA ANALOG INTEGRATED CIRCUIT DEVICE DATA
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ADC Reference Terminals (VREFL and VREFH)

VREFL and VREFH are the reference voltage terminals for the ADC. It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC Supply Terminals (VDDA and VSSA)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground terminal for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU Power Supply Terminals (EVDD and EVSS)

EVDD and EVSS are the power supply and ground terminals. The MCU operates from a single power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

Test Terminal (FLSVPP)

For test purposes only. Do not connect in the application.

Exposed Pad Terminal

The exposed pad terminal on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

ANALOG DIE DESCRIPTION

Interrupts

The 908E625 has seven different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

Low-Voltage Interrupt

The Low-Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the low-voltage interrupt is enabled, an interrupt will be initiated.

With LVI the H-Bridges (high-side MOSFET only) and the high-side driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

High-Voltage Interrupt

The High-Voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the High-Voltage Interrupt is enabled, an interrupt will be initiated.

With HVI the H-Bridges (high-side MOSFET only) and the high-side driver are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

High-Temperature Interrupt

The High-Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the High-Temperature Interrupt is enabled, an interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

Autonomous Watchdog Interrupt (AWD)

Refer to Autonomous Watchdog (AWD) on page 36.

LIN Interrupt

If the LINIE bit is set, a falling edge on the LIN terminal will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

Hall-Effect Sensor Input Terminal Interrupt

If the PHIE bit is set, the enabled Hall-effect sensor input terminals H1:H3 can generate an interrupt if a current above the threshold is detected. During STOP mode this interrupt, combined with the cyclic wake-up feature of the AWD, can wake up the system (refer to Hall-Effect Sensor Input Terminals (H1:H3) on page 25).

Overcurrent Interrupt

If an overcurrent condition on a half-bridge occurs, the high-side or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

System Wake-Up

System wake-up can be initiated by any of four events:

- A falling edge on the LIN terminal.
- A wake-up signal from the AWD.
- A logic [1] at Hall-effect sensor input terminal during cyclic check via AWD.
- An LVR condition.

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake up the microcontroller as well as the main voltage regulator (MREG) (Figure 6).
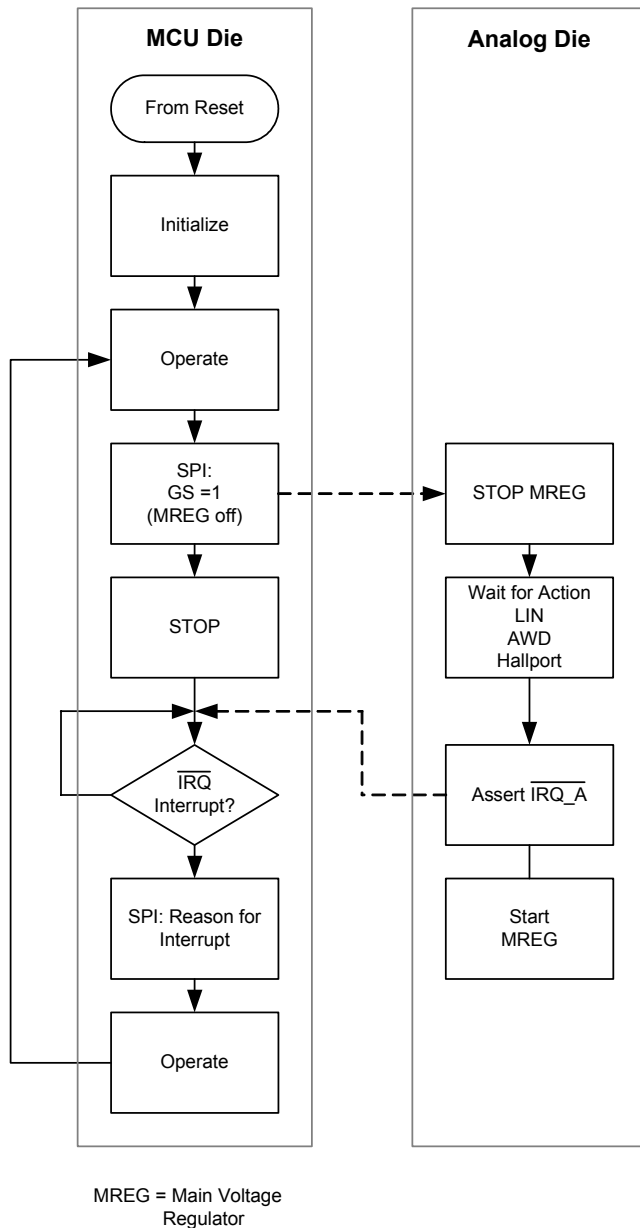

MREG = Main Voltage
Regulator

Figure 6. STOP Mode/Wake-Up Procedure

Interrupt Flag Register (IFR)

Register Name and Address: IFR - $05

	Bit7	6	5	4	3	2	1	Bit0
Read	0	HPF	LINF	HTF	LVF	HVF	OCF	0
Write								
Reset	0	0	0	0	0	0	0	0

HPF—Hall-Effect Sensor Input Terminal Flag Bit

This read/write flag is set depending on RUN/STOP mode.

RUN Mode An interrupt will be generated when a state change on any enabled Hall-effect sensor input terminal is detected. Clear HPF by writing a logic [1] to HPF. Reset clears the HPF bit. Writing a logic [0] to HPF has no effect.

- 1 = State change on the hallflags detected.
- 0 = No state change on the hallflags detected.

STOP Mode An interrupt will be generated when AWDCC is set and a current above the threshold is detected on any enabled Hall-effect sensor input terminal. Clear HPF by writing a logic [1] to HPF. Reset clears the HPF bit. Writing a logic [0] to HPF has no effect.

- 1 = One or more of the selected Hall-effect sensor input terminals had been pulled HIGH.
- 0 = None of the selected Hall-effect sensor input terminals has been pulled HIGH.

LINF—LIN Flag Bit

This read/write flag is set on the falling edge at the LIN data line. Clear LINF by writing a logic [1] to LINF. Reset clears the LINF bit. Writing a logic [0] to LINF has no effect.

- 1 = Falling edge on LIN data line has occurred.
- 0 = Falling edge on LIN data line has not occurred since last clear.

HTF—High-Temperature Flag Bit

This read/write flag is set on a high-temperature condition. Clear HTF by writing a logic [1] to HTF. If a high-temperature condition is still present while writing a logic [1] to HTF, the writing has no effect. Therefore, a high-temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High-temperature condition has occurred.
- 0 = High-temperature condition has not occurred.

LVF—Low-Voltage Flag Bit

This read/write flag is set on a low-voltage condition. Clear LVF by writing a logic [1] to LVF. If a low-voltage condition is still present while writing a logic [1] to LVF, the writing has no effect. Therefore, a low-voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low-voltage condition has occurred.
- 0 = Low-voltage condition has not occurred.

HVF—High-Voltage Flag Bit

This read/write flag is set on a high-voltage condition. Clear HVF by writing a logic [1] to HVF. If high-voltage condition is still present while writing a logic [1] to HVF, the writing has no effect. Therefore, a high-voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High-voltage condition has occurred.
- 0 = High-voltage condition has not occurred.

OCF—Overcurrent Flag Bit

This read-only flag is set on an overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 7, which shows the three signals triggering the OCF.

- 1 = High-current condition has occurred.
- 0 = High-current condition has not occurred.
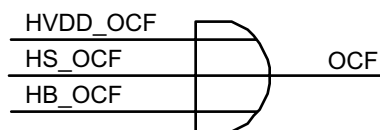
Figure 7. Principal Implementation for OCF

Interrupt Mask Register (IMR)

Register Name and Address: IMR - $04

	Bit7	6	5	4	3	2	1	Bit0
Read	0	HPIE	LINIE	HTIE	LVIE	HVIE	OCIE	0
Write								
Reset	0	0	0	0	0	0	0	0

HPIE—Hall-Effect Sensor Input Terminal Interrupt Enable Bit

This read/write bit enables CPU interrupts by the Hall-effect sensor input terminal flag, HPF. Reset clears the HPIE bit.

- 1 = Interrupt requests from HPF flag enabled.
- 0 = Interrupt requests from HPF flag disabled.

LINIE—LIN Line Interrupt Enable Bit

This read/write bit enables CPU interrupts by the LIN flag, LINF. Reset clears the LINIE bit.

- 1 = Interrupt requests from LINF flag enabled.
- 0 = Interrupt requests from LINF flag disabled.

HTIE—High-Temperature Interrupt Enable Bit

This read/write bit enables CPU interrupts by the high-temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—Low-Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the low-voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—High-Voltage Interrupt Enable Bit

This read/write bit enables CPU interrupts by the high-voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—Overcurrent Interrupt Enable Bit

This read/write bit enables CPU interrupts by the overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

Reset

The 908E625 chip has four internal reset sources and one external reset source, as explained in the paragraphs below. Figure 8 depicts the internal reset sources.

Figure 8. Internal Reset Routing

Reset Internal Sources

Autonomous Watchdog

AWD modules generates a reset because of a timeout (watchdog function).

High-Temperature Reset

To prevent damage to the device, a reset will be initiated if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high-temperature reset is disabled.

Low-Voltage Reset

The LVR is related to the internal V_{DD}. In case the voltage falls below a certain threshold, it will pull down the $\overline{RST\_A}$ terminal.

High-Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the $\overline{RST\_A}$ terminal. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high-voltage reset is disabled.

Reset External Source

External Reset Terminal

The microcontroller has the capability of resetting the *SMARTMOS* device by pulling down the $\overline{RST}$ terminal.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	Bit7	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
Write								
Reset	0	0	0	0	0	0	0	0

TTEST—High-Temperature Reset Test

This read/write bit is for test purposes only. It decreases the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low-temperature threshold enabled.
- 0 = Low-temperature threshold disabled.

HVRE—High-Voltage Reset Enable Bit

This read/write bit enables resets on high-voltage conditions. Reset clears the HVRE bit.

    1 = High-voltage reset enabled.

    0 = High-voltage reset disabled.

HTRE—High-Temperature Reset Enable Bit

This read/write bit enables resets on high-temperature conditions. Reset clears the HTRE bit.

- 1 = High-temperature reset enabled.
- 0 = High-temperature reset disabled.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E625.

The interface consists of four terminals (see Figure 9):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.
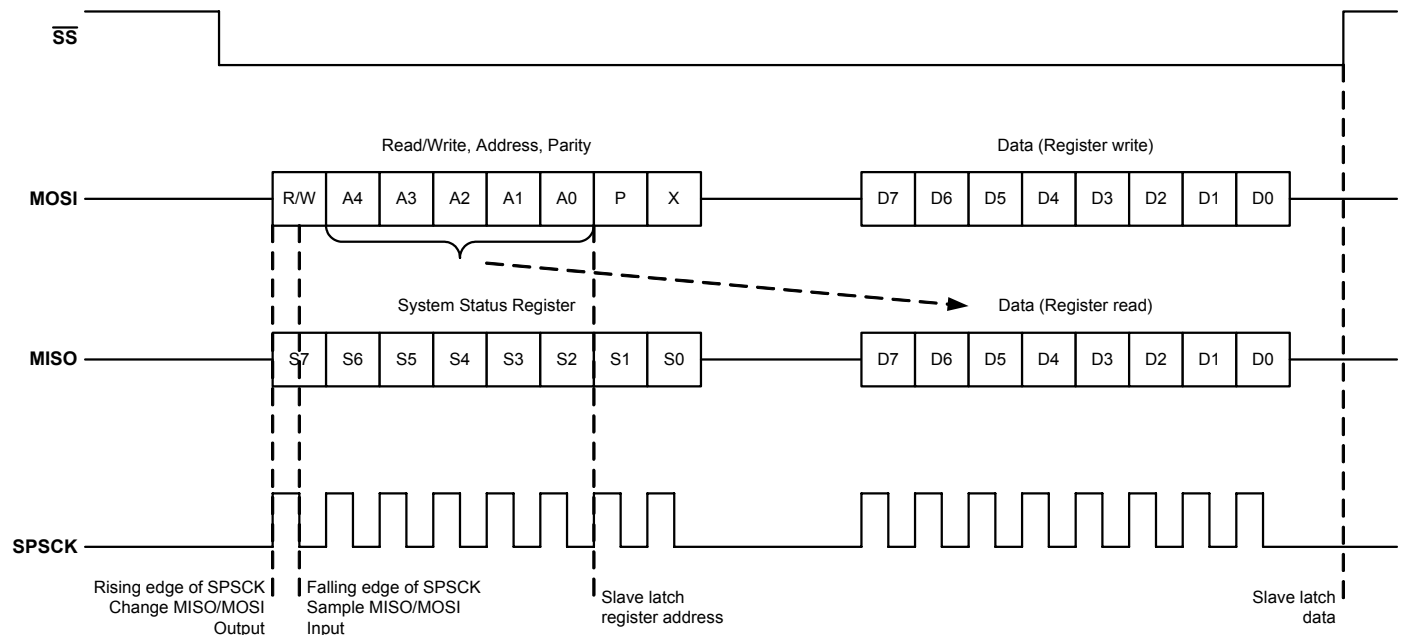
Figure 9. SPI Protocol

During the inactive phase of $\overline{SS}$, the new data transfer is prepared. The falling edge on the $\overline{SS}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The

data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{SS}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high impedance.

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Master Address Byte

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to "0" if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals "1". For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals "0."

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Contains data to be written or no valid data during a read operation.

Slave Status Byte

Contains the contents of the System Status Register ($0c) independent of whether it is a write or read operation or which register was selected.

Slave Data Byte

Contains the contents of selected register. During a write operation it includes the register content prior to a write operation.

SPI Register Overview

Table 1 summarizes the SPI Register addresses and the bit names of each register.

Table 1. List of Registers

Addr	Register Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01	H-Bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
$02	H-Bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W	OFC_EN	CSA				CLS2	CLS1	CLS0
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W	PSON	SRS1	SRS0					GS
$04	Interrupt Mask (IMR)	R	0	HPIE	LINIE	HTIE	LVIE	HVIE	OCIE	0
		W	0	HPIE	LINIE	HTIE	LVIE	HVIE	OCIE	
$05	Interrupt Flag (IFR)	R	0	HPF	LINF	HTF	LVF	HVF	OCF	0
		W	0	HPF	LINF	HTF	LVF	HVF		
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W	TTEST						HVRE	HTRE
$07	Analog Multiplexer Configuration (ADMUX)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W					SS3	SS2	SS1	SS0
$08	Hall-Effect Sensor Input Terminal Control (HACTL)	R	0	0	0	0	0	H3EN	H2EN	H1EN
		W						H3EN	H2EN	H1EN
$09	Hall-Effect Sensor Input Terminal Status (HASTAT)	R	0	0	0	0	0	H3F	H2F	H1F
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	AWDIE	AWDCC	AWDF	AWDR
		W			AWDRST	AWDRE	AWDIE	AWDCC	AWDF	AWDR
$0b	Power Output (POUT)	R	0	0	CSSEL1	CSSEL0	CSEN1	CSEN0	HVDDON	HS_ON
		W			CSSEL1	CSSEL0	CSEN1	CSEN0	HVDDON	HS_ON
$0c	System Status (SYSSTAT)	R	HP_OCF	LINCL	HVDD_OCF	HS_OCF	LVF	HVF	HB_OCF	HTF
		W	HP_OCF		HVDD_OCF	HS_OCF	LVF	HVF	HB_OCF	

Table 2. Analog Multiplexer Configuration Register

SS3	SS2	SS1	SS0	Channel
0	0	0	0	Current Recopy HB1
0	0	0	1	Current Recopy HB2
0	0	1	0	Current Recopy HB3
0	0	1	1	Current Recopy HB4
0	1	0	0	V_{SUP} Prescaler
0	1	0	1	Temperature Sensor
0	1	1	0	Not Used
0	1	1	1	PA1 Terminal
1	0	0	0	Not Used
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Analog Input PA1

The Analog input PA1 terminal provides an input for reading analog signals and is internally connected to the analog multiplexer. It can be used for reading switches, potentiometers or resistor values, etc.

Analog Input PA1 Current Source

The analog input PA1 has an additional selectable current source. It enables the reading of switches, NTC, etc., without the need of an additional supply line for the sensor (Figure 10). With this feature it is also possible to read multiple switches on one input.

Current source is enabled if the PSON bit in the System Control Register (SYSCTL) and the CSEN bit in the Power Output Register (POUT) is set.

Four different current source values can be selected with the CSSELx bits (Table 3). This function ceases during STOP mode operation.

Table 3. PA1 Current Source Level Selection Bits

CSSEL1	CSSEL0	Current Source Enable (typ.)
0	0	10%
0	1	30%
1	0	60%
1	1	100%
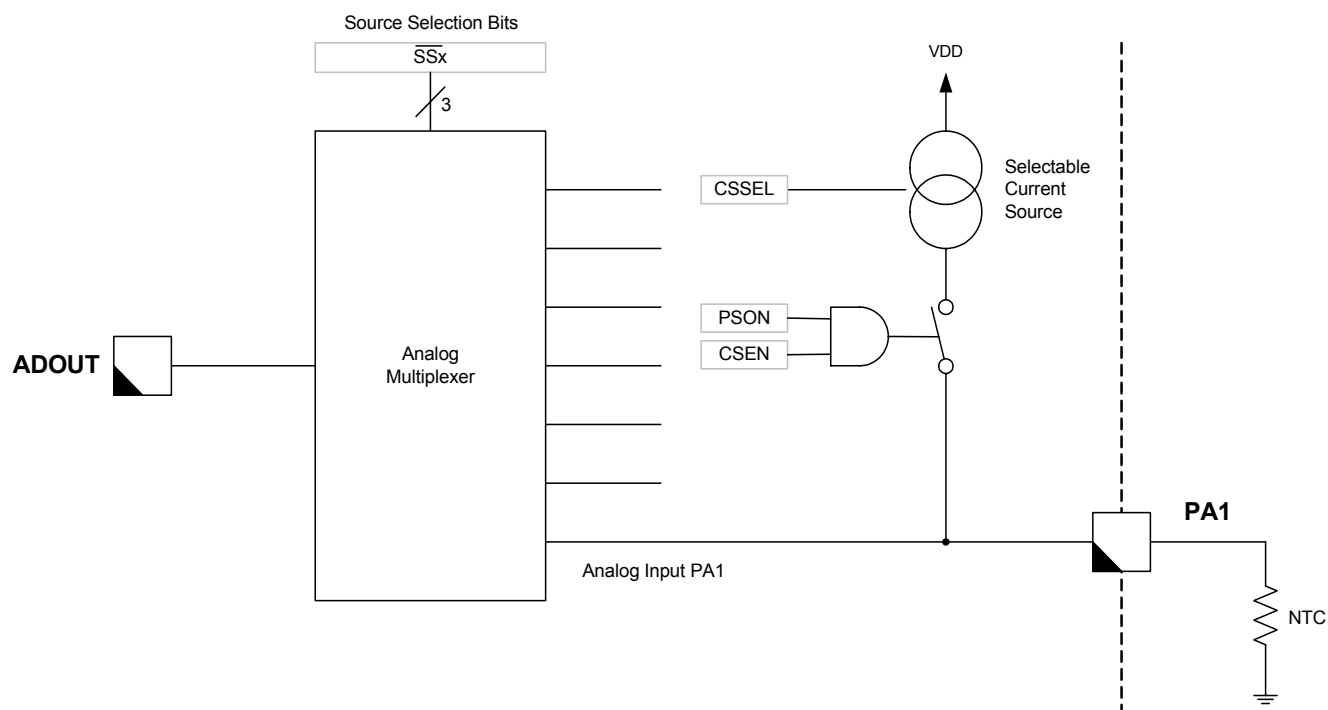
Figure 10. Analog Input PA1 and Multiplexer6

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Power Output Register (POUT)

Register Name and Address: POUT - $0b

	Bit 7	6	5	4	3	2	1	Bit 0
Read	0	0	CSSEL1	CSSEL0	CSEN	0 (Note 17)	HVDDON	HS_ON
Write			CSSEL1	CSSEL0	CSEN	0 (Note 17)	HVDDON	HS_ON
Reset	0	0	0	0	0	0	0	0

Notes
17. This bit must always be set to 0.

CSSEL0:CSSEL1—Current Source Select Bits

This read/write bit selects the current source values. Reset clears the CSSEL0:CSSEL1 bits.

CSEN—Current Source Enable Bit

This read/write bit enables the current source for PA1. Reset clears the CSEN bit (Table 4).

Table 4. PA1 Current Source Enable Bit

CSEN	Current Source Enable
0	Current Source Off
1	Current Source On

HVDDON—HVDD On Bit

This read/write bit enables HVDD output. Reset clears the HVDDON bit.

- 1 = HVDD enabled.
- 0 = HVDD disabled.

HS_ON—Lamp Driver On Bit

This read/write bit enables the Lamp driver. Reset clears the HS_ON bit.

- 1 = Lamp driver enabled.
- 0 = Lamp driver disabled.

Hall-Effect Sensor Input Terminals (H1:H3)

Function

The Hall-effect sensor input terminals provide three inputs for two-terminal Hall-effect sensors for detecting stall and position or reading Hall-effect sensor contact switches. The Hall-effect sensor input terminals are not influenced by the PSON bit in the System Control Register.

Each terminal of the Hall-effect sensor can be enabled by setting the HxEN bit in the Hall-Effect Sensor Input Terminal Control Register (HACTL). If the terminals are enabled, the Hall-effect sensors are supplied with V_{SUP} voltage and the sense circuitry is working. An internal clamp circuity limits the supply voltage to the sensor to 15 V. This sense circuitry monitors the current to VSS. The result of this sense operation is given by the HxF flags in the Hall-Effect Sensor Input Terminal Status Register (HASTAT).

The flag is set if the sensed current is higher than I_{HSCT}. To prevent noise on this flag, a hysteresis is implemented on these terminals.

After switching on the Hall-effect sensor input terminals (HxEN = 1), the Hall-effect sensors need some time to stabilize the output. In RUN mode the software must wait at least 40 μs between enabling the Hall-effect sensor and reading the hallflag.

The Hall-effect sensor input terminal works in an dynamic output voltage range from V_{SUP} down to 2.0 V. Below 2.0 V the hallflags are not functional anymore. If the output voltage is below a certain threshold, the Hall-Effect Sensor Input Terminal Overcurrent Flag (HP_OCF) in the System Status Register is set.

Figures 11 through 13, pp. 26–27, show the connections to the Hall-effect input sensors.
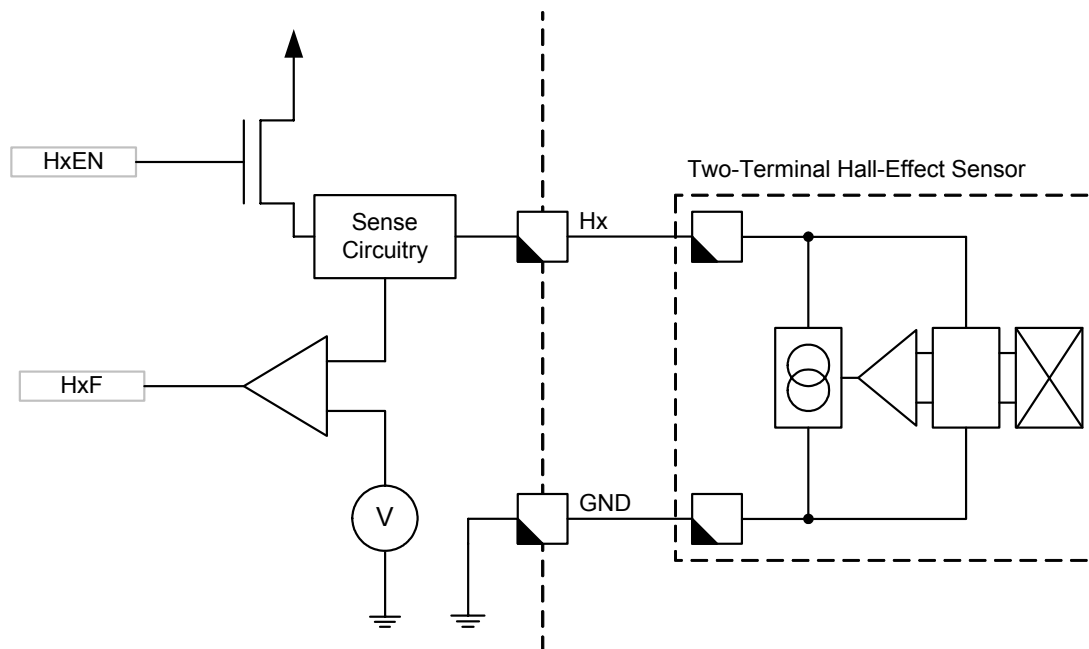
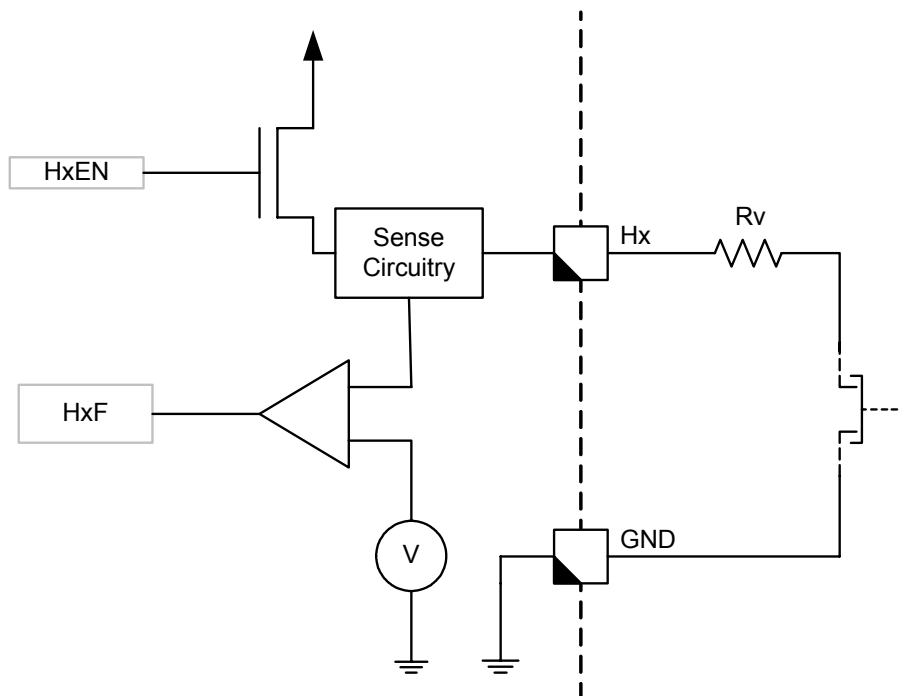**Figure 11. Hall-Effect Sensor Input Terminal Connected to Two-Terminal Hall-Effect Sensor**

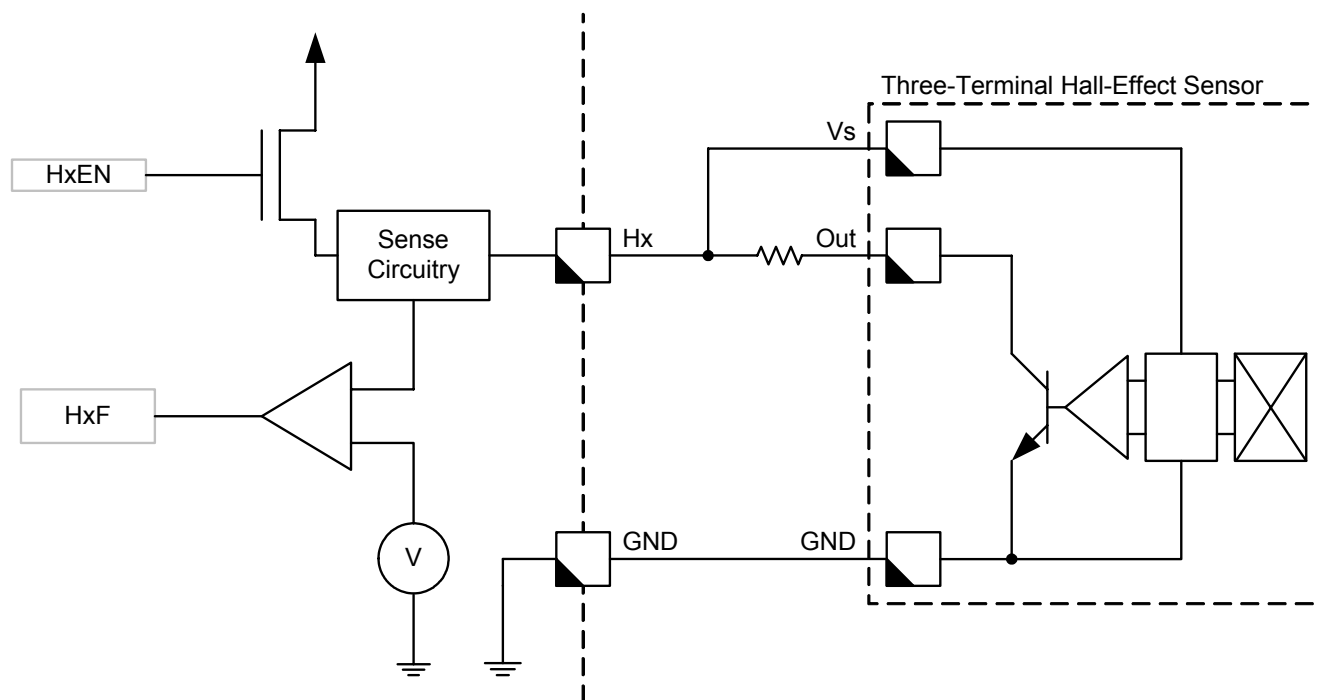**Figure 12. Hall-Effect Sensor Input Terminal Connected to Local Switch**

Figure 13. Hall-Effect Sensor Input Terminal Connected to Three-Terminal Hall-Effect Sensor

Interrupts

The Hall-effect sensor input terminals are interrupt capable. How and when an interrupt occurs is dependent on the operating mode, RUN or Stop.

RUN Mode

In RUN mode the Hall-effect sensor input terminal interrupt flag (HPF) will be set if a state change on the hallflags (HxF) is detected. The interrupt is maskable with the HPIE bit in the Interrupt Mask Register. Before enabling the interrupt, the flag should be cleared in order to prevent a wrong interrupt.

STOP Mode

In STOP mode the Hall-effect sensor input terminals are disabled independent of the state of the HxEN flags.

Cyclic Wake-Up

The Hall-effect sensor inputs can be used to wake up the system. This wake-up function is provided by the cyclic check wake-up feature of the AWD (autonomous watchdog).

If the cyclic check wake-up feature is enabled (AWDCC bit is set), the AWD switches on the enabled Hall-effect sensor terminals periodically. To ensure that the Hall-effect sensor current is stabilized after switching on, the inputs are sensed after ~40 μs. If a "1" is detected ($I_{Hall\ sensor} > I_{HSCT}$) and the interrupt mask bit HPIE is set, an interrupt is performed. This wakes up the MCU and starts the main voltage regulator.

The wake-up function via this input is available when all three conditions exist:

- The two-terminal Hall-effect sensor input is enabled (HxEN = 1).
- The cyclic wake-up of the AWD is enabled (AWDCC = 1) (see).
- The Hall-effect sensor input terminal interrupt is enabled (HPIE = 1).

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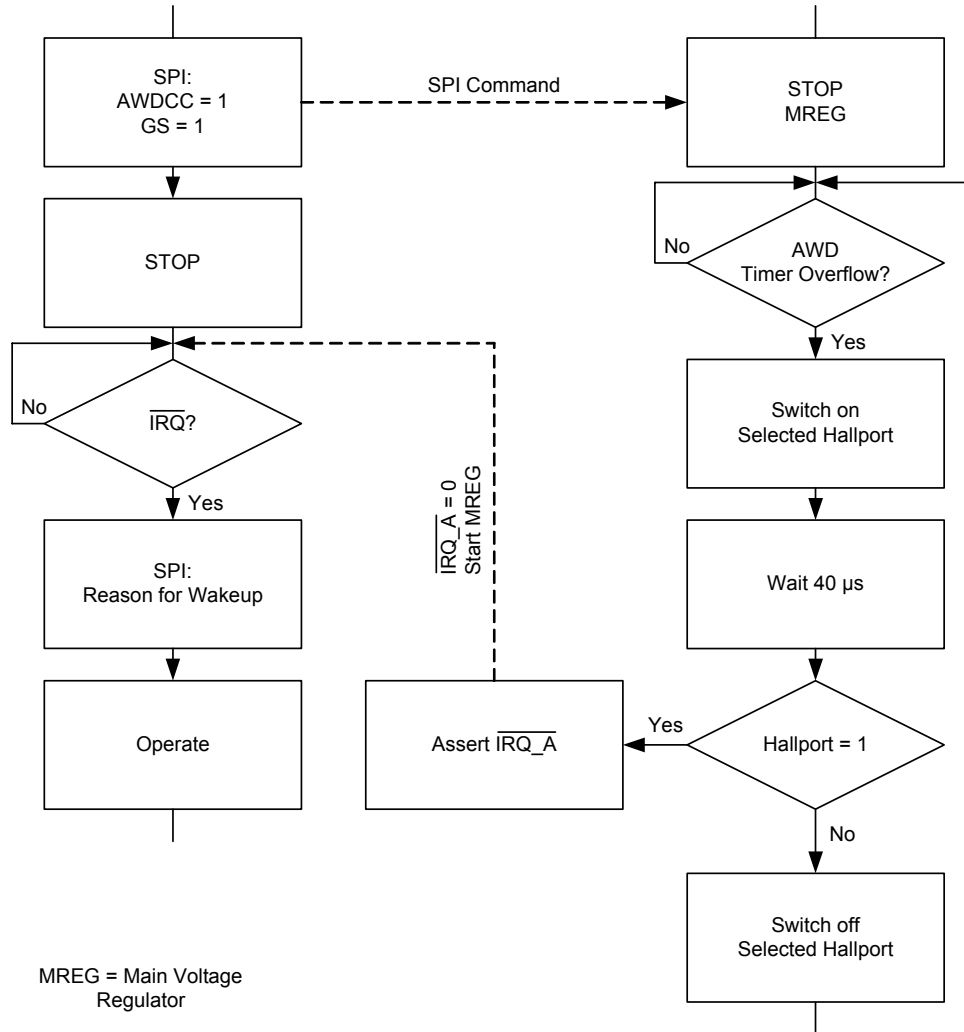
Figure 14. Hall-Effect Sensor Input Terminal Cyclic Check Wake-Up Feature

MREG = Main Voltage Regulator

Hall-Effect Sensor Input Terminal Control Register (HACTL)

Register Name and Address: HACTL - $08

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	H3EN	H2EN	H1EN
Write								
Reset	0	0	0	0	0	0	0	0

H3EN:H1EN—Hall-Effect Sensor Input Terminal Enable Bits

These read/write bits enable the Hall-effect sensor input terminals. Reset clears the H3EN:H1EN bits.

- 1 = Hall-effect sensor input terminal Hx switched on and sensed.
- 0 = Hall-effect sensor input terminal Hx disabled.

Hall-Effect Sensor Input Terminal Status Register (HASTAT)

Register Name and Address: HASTAT - $09

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	0	0	H3F	H2F	H1F
Write								
Reset	0	0	0	0	0	0	0	0

H3F:H1F—Hall-Effect Sensor Input Terminal Flag Bits

These read-only flag bits reflect the input Hx while the Hall-effect sensor input terminal Hx is enabled (HxEN = 1). Reset clears the H3F:H1F bits.

- 1 = Hall-effect sensor input terminal current above threshold.
- 0 = Hall-effect sensor input terminal current below threshold.

Half-Bridges

Outputs HB1:HB4 provide four low-resistive half-bridge output stages. The half-bridges can be used in H-Bridge, high-side, or low-side configurations.

Reset clears all bits in the H-Bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short circuit (overcurrent) protection on high-side and low-side MOSFETs.
- Current recopy feature (low side MOSFET).
- Overtemperature protection.
- Overvoltage and undervoltage protection.
- Current limitation feature (low side MOSFET).
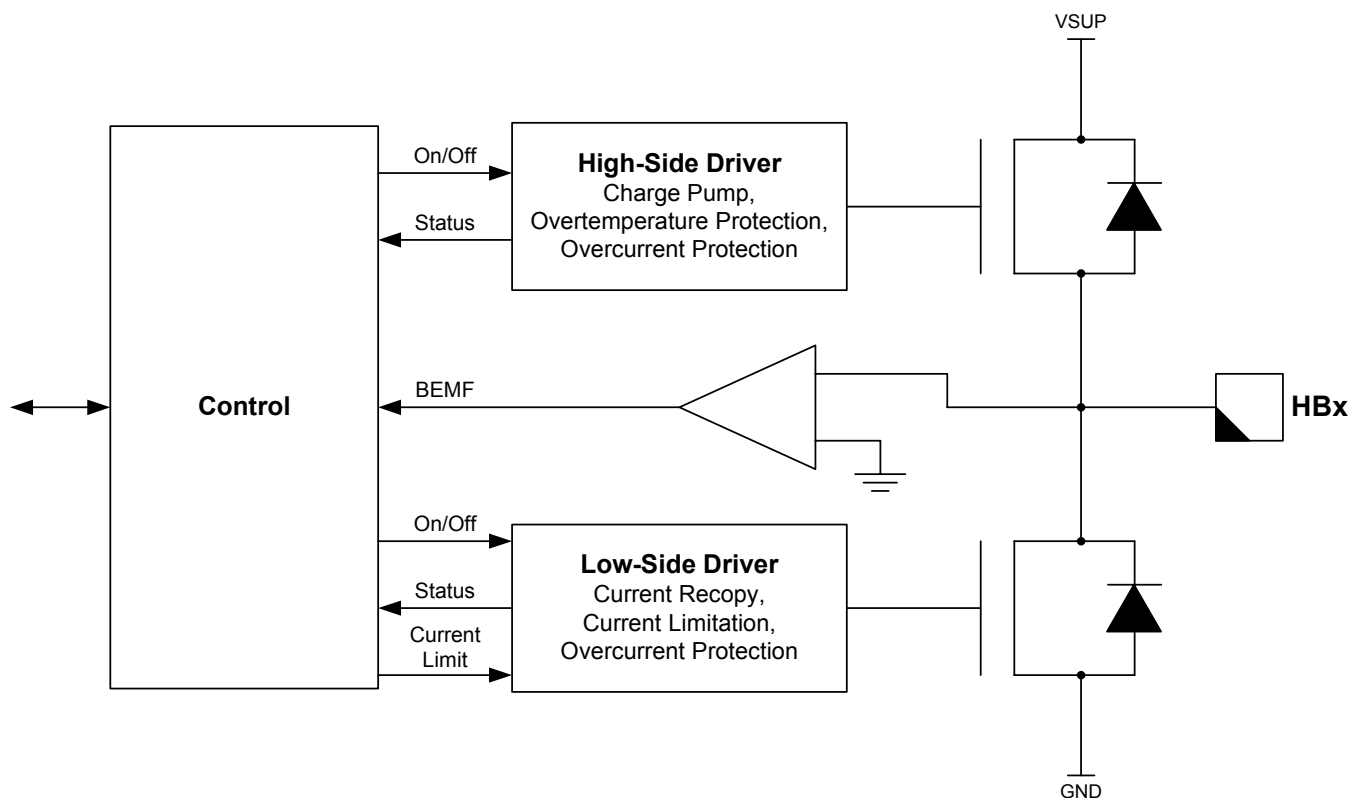
Figure 15. Half-Bridge Push-Pull Output Driver

Half-Bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high-side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists. Switching the high-side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low-side MOSFET on is blocked as long as the potential between gate and source of the high-side MOSFET did not fall below a certain threshold.

Half-Bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	Bit7	6	5	4	3	2	1	Bit0
Read Write	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low-Side On/Off Bits

These read/write bits turn on the low-side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low-side MOSFET turned on for half-bridge output x.
- 0 = Low-side MOSFET turned off for half-bridge output x.

HBx_H—High-Side On/Off Bits

These read/write bits turn on the high-side MOSFETs. Reset clears the HBx_H bits.

  1 = High-side MOSFET turned on for half-bridge output x.
  0 = High-side MOSFET turned on for half-bridge output x.

Half-Bridge Current Limitation

Each low-side MOSFET offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low-side MOSFET. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristics. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The recommended frequency range for the FGEN and the PWM is 0.1 kHz to 20 kHz.

Functionality

Each low-side MOSFET switches off if a current above the selected current limit was detected. The 908E625 offers five different current limits (refer to Table 5, page 33, for current limit values). The low-side MOSFET switches on again if a rising edge on the FGEN input was detected (Figure 16).
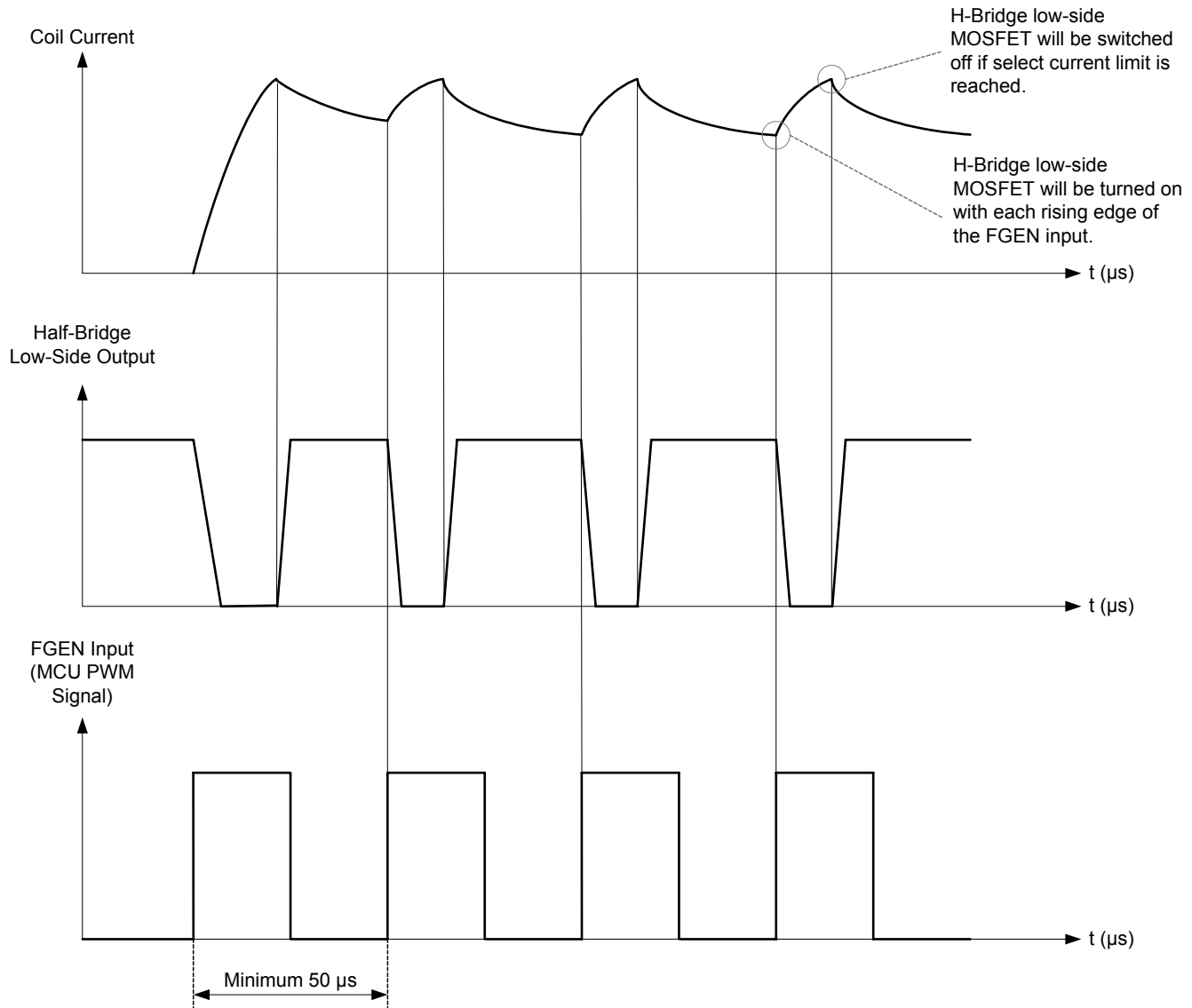
Figure 16. Half-Bridge Current Limitation

Offset Chopping

If bit OFC_EN in the H-Bridge Control Register (HBCTL) is set, HB1 and HB2 will continue to switch on the low-side MOSFETs with the rising edge of the FGEN signal and HB3 and HB4 will switch on the low-side MOSFETs with the falling edge on the FGEN input. In step motor applications this feature allows the reduction of EMI due to a reduction of the di/dt (Figure 17).

Coil1 Current

Coil2 Current

FGEN Input
(MCU PWM
Signal)

Current in
VSUP Line

HB1
Coil1
HB2

HB3
Coil2
HB4
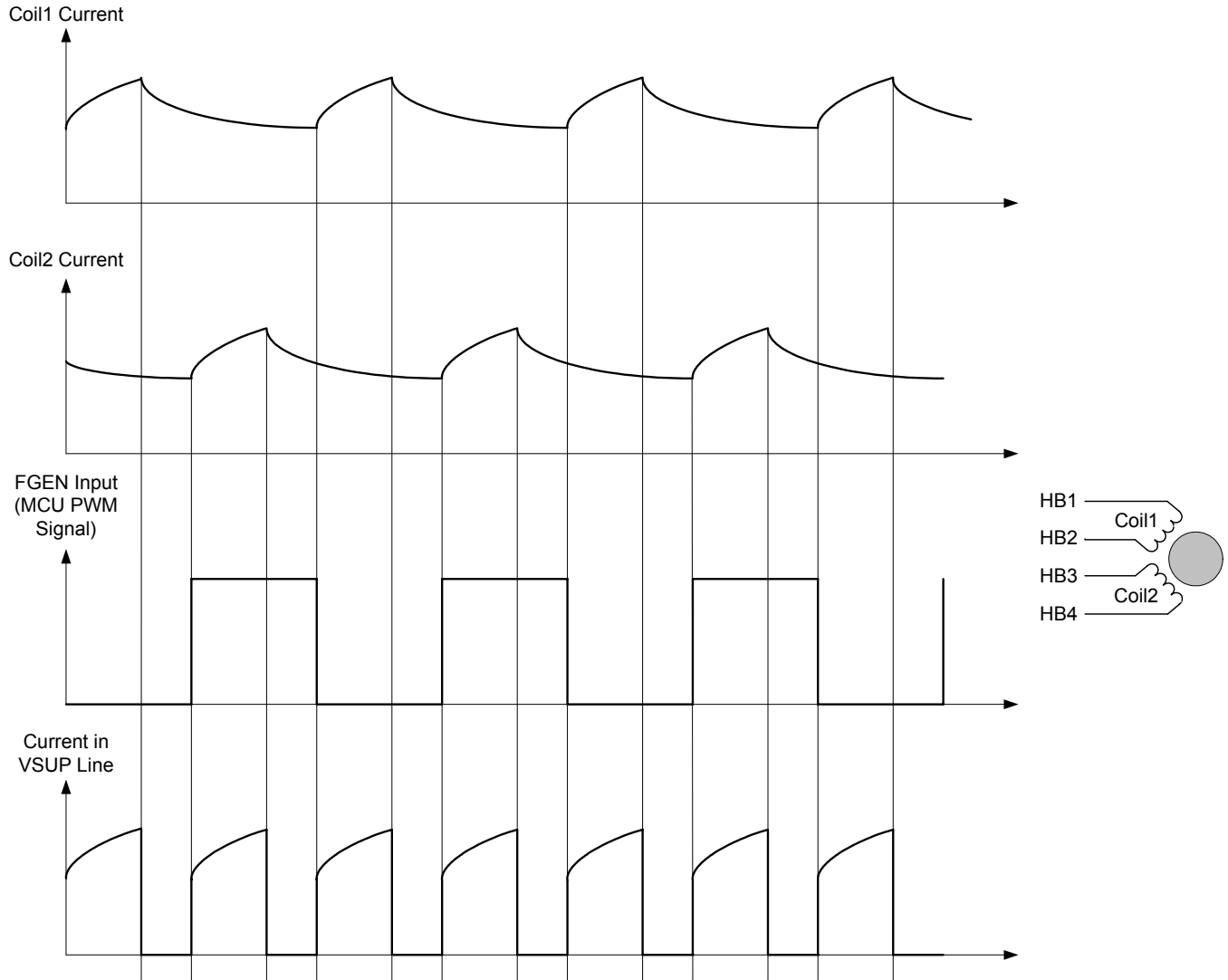
Figure 17. Offset Chopping for Step Motor Control

Half-Bridge Current Recopy

Each low-side MOSFET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the analog multiplexer.

The factor for the current sense amplification can be selected via bit CSA in the System Control Register.

- CSA = 1: Low resolution selected (500 mA measurement range).
- CSA = 0: High resolution selected (2.5 A measurement range).

Half-Bridge BEMF Generation

The BEMF output is set to "1" if a recirculation current is detected in any half-bridge. This recirculation current flows via the two freewheeling diodes of the power MOSFETs. The BEMF circuitry detects that and generates a HIGH on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in step motor applications. For this the BEMF circuitry takes advantage of the instability of the electrical and mechanical behavior of a step motor when blocked. In addition the signal can be used for open load detection (absence of this signal) (see Figure 18, page 32).
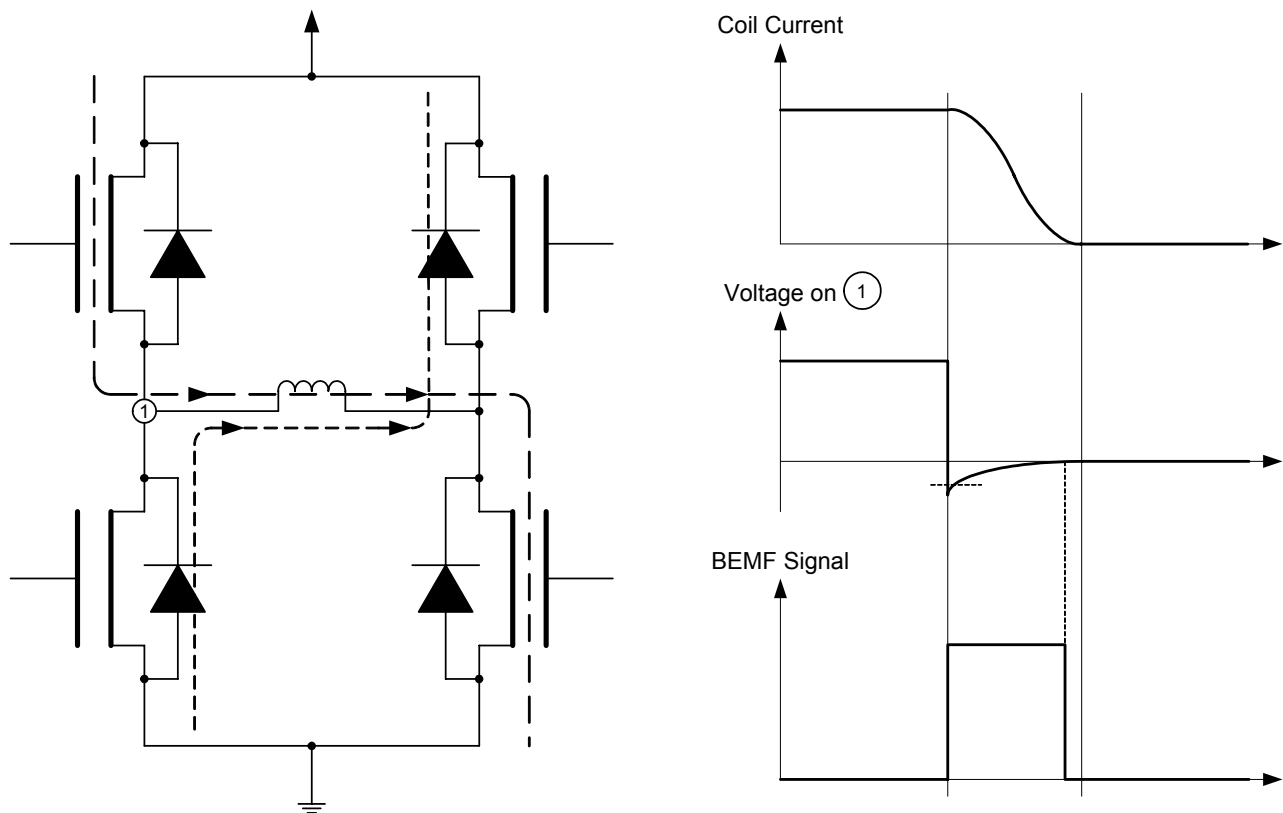
Figure 18. BEMF Signal Generation

Half-Bridge Overtemperature Protection

The half-bridge outputs provide an overtemperature pre-warning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against overtemperature, the High-Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

Half-Bridge Overcurrent Protection

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an overcurrent on the high side is detected, the high-side MOSFETs on all HB high-side MOSFETs are switched off automatically. In the event an overcurrent on the low side is detected, all HB low-side MOSFETs are switched off automatically. In both cases the overcurrent status flag HB_OCF in the System Status Register (SYSSTAT) is set.

The overcurrent status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by reset.

Half-Bridge Overvoltage/Undervoltage

The half-bridge outputs are protected against undervoltage and overvoltage conditions. This protection is done by the low- and high-voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The overvoltage/undervoltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high- or low-voltage condition is present.

Half-Bridge Control Register (HBCTL)

Register Name and Address: HBCTL - $02

	Bit7	6	5	4	3	2	1	Bit0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
Write								
Reset	0	0	0	0	0	0	0	0

OFC_EN—H-Bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

CSA—H-Bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-Bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

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CLS2:CLS0—H-Bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 5. Reset clears the CLS2:CLS0 bits.

Table 5. H-Bridge Current Limitation Value Selection Bits

CLS2	CLS1	CLS0	Current Limit
0	0	0	
0	0	1	No Limit
0	1	0	
0	1	1	55 mA (typ)
1	0	0	260 mA (typ)
1	0	1	370 mA (typ)
1	1	0	550 mA (typ)
1	1	1	740 mA (typ)

High-Side Driver

The high-side output is a low-resistive high-side switch targeted for driving lamps. The high side is protected against overtemperature. To limit the high inrush current of bulbs, overcurrent protection circuitry is used to limit the current. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HS_ON in the Power Output Register. Figure 19 depicts the high-side switch circuitry and connection to external lamp.

High-Side Overvoltage/Undervoltage Protection

The high-side output terminal, HS, is protected against undervoltage/overvoltage conditions. This protection is done by the low- and high-voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the output is disabled.

The overvoltage/undervoltage status flags are cleared and the output re-enabled by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high- or low-voltage condition is present.
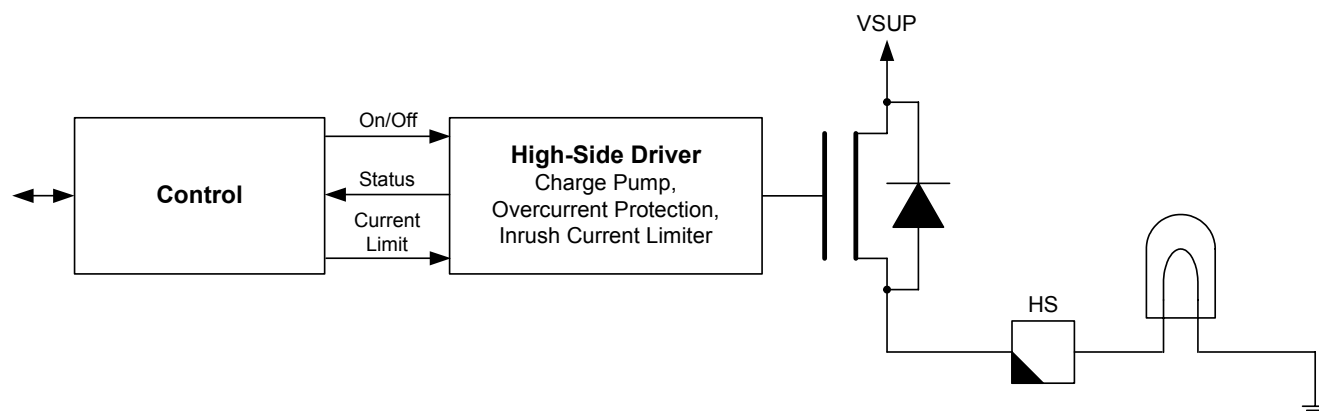
Figure 19. High-Side Circuitry

High-Side Overtemperature Protection

The high-side output provides an overtemperature pre-warning with the HTF in the Interrupt Flag Register. In order to protect the output against overtemperature, the High-Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

High-Side Overcurrent Protection

The high-side output is protected against overcurrent. In the event overcurrent limit is or was reached, the output automatically switches off and the overcurrent flag is set.

Due to the high inrush current of bulbs, a special feature of the 908E625 prevents an overcurrent shutdown during this inrush. If an PWM frequency is supplied to the FGEN output during the switching on of a bulb, the inrush current is limited to the overcurrent shutdown limit. This means if the current reaches the overcurrent shutdown, the high side will be switched off, but each rising edge on the FGEN input will enable the driver again.

To distinguish between a shutdown due to an inrush current or a real shutdown, the software must check if the overcurrent status flag (HS_OCF) in the System Status Register is set beyond a certain period of time. The overcurrent status flag is cleared by writing a logic [1] to the HS_OCF in the System Status Register (see Figure 20, page 34).
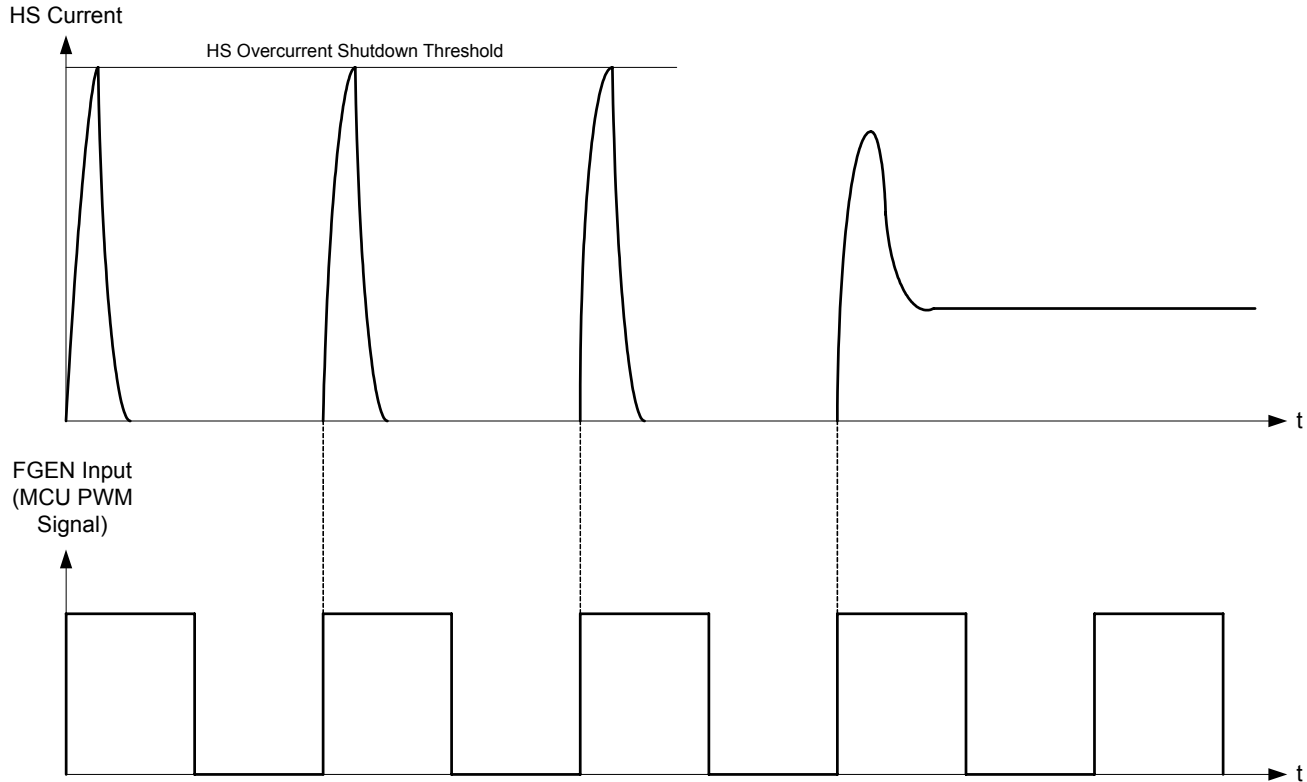
Figure 20. Inrush Current Limiter on High-Side Output

Switchable VDD Outputs

The HVDD terminal is a switchable VDD output terminal. It can be used for driving external circuitry that requires a V_{DD} voltage. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HVDDON in the Power Output Register. Low- or high-voltage conditions (LVI/HVI) have no influence on this circuitry.

HVDD Overtemperature Protection

Overtemperature protection is enabled if the high-temperature reset is enabled.

HVDD Overcurrent Protection

The HVDD output is protected against overcurrent. In the event the overcurrent limit is or was reached, the output automatically switches off and the HVDD overcurrent flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0
Write								GS
Reset	0	0	0	0	0	0	0	0

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, high side, LIN transmitter, Analog Input PA1 current sources, and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

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SRS0 : SRS1—LIN Slew Rate Selection Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 6.

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

Table 6. LIN Slew Rate Selection Bits

SRS1	SRS0	LIN Slew Rate
0	0	Initial Slew Rate (20 kBaud)
0	1	Slow Slew Rate (10 kBaud)
1	0	High Speed II (8x)
1	1	High Speed I (4x)

GS—Go to STOP Mode Bit

This write-only bit instructs the 908E625 to power down and go into STOP mode. Reset or CPU interrupt requests clear the GS bit.

- 1 = Power down and go into STOP mode.
- 0 = Not in STOP mode.

System Control Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	Bit7	6	5	4	3	2	1	Bit0
Read	HP_OCF	LINCL	HVDD_OCF	HS_OCF	LVF	HVF	HB_OCF	HTF
Write	HP_OCF		HVDD_OCF	HS_OCF			HB_OCF	
Reset	0	0	0	0	0	0	0	0

HP_OCF—Hall-Effect Sensor Input Terminal Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at one of the Hall-effect sensor input terminals. Clear HP_OCF and enable the output by writing a logic [1] to the HP_OCF flag. Reset clears the HP_OCF bit. Writing a logic [0] to HP_OCF has no effect.

- 1 = Overcurrent condition on Hall-effect sensor input terminal has occurred.
- 0 = No overcurrent condition on Hall-effect sensor input terminal has occurred.

LINCL — LIN Current Limitation Bit

This read-only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the HVDD terminal. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the HVDD_OCF bit. Writing a logic [0] to HVDD_OCF has no effect.

- 1 = Overcurrent condition on HVDD has occurred.
- 0 = No overcurrent condition on HVDD has occurred.

HS_OCF—High-Side Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the high-side driver. Clear HS_OCF and enable the high-side driver by writing a logic [1] to HS_OCF. Reset clears the HS_OCF bit. Writing a logic [0] to HS_OCF has no effect.

- 1 = Overcurrent condition on high-side drivers has occurred.
- 0 = No overcurrent condition on high-side drivers has occurred.

LVF—Low-Voltage Bit

This read only bit is a copy of the LVF bit in the Interrupt Flag Register.

- 1 = Low-voltage condition has occurred.
- 0 = No low-voltage condition has occurred.

HVF—High-Voltage Sensor Bit

This read-only bit is a copy of the HVF bit in the Interrupt Flag Register.

- 1 = High-voltage condition has occurred.
- 0 = No high-voltage condition has occurred.

HB_OCF—H-Bridge Overcurrent Flag Bit

This read/write flag is set on an overcurrent condition at the H-Bridges. Clear HB_OCF and enable the H-Bridge driver by writing a logic [1] to HB_OCF. Reset clears the HB_OCF bit. Writing a logic [0] to HB_OCF has no effect.

- 1 = Overcurrent condition on H-Bridges has occurred.
- 0 = No overcurrent condition on H-Bridges has occurred.

HTF—Overtemperature Status Bit

This read-only bit is a copy of the HTF bit in the Interrupt Flag Register.

- 1 = Overtemperature condition has occurred.
- 0 = No overtemperature condition has occurred.

Autonomous Watchdog (AWD)

The Autonomous Watchdog module consists of three functions:

- Watchdog function for the CPU in RUN mode
- Periodic interrupt function in STOP mode
- Cyclic wake-up function in STOP mode

The AWD is enabled if AWDIE, AWDRE, or AWDCC in the AWDCTL Register is set. If these bits are cleared, the AWD oscillator is disabled and the watchdog switched off.

Watchdog

The watchdog function is only available in RUN mode. On setting the AWDRE bit, watchdog functionality in RUN mode is activated. Once this function is enabled, it is not possible to disable it via software.

If the timer reaches end value and AWDRE is set, a system reset is initiated. Operations of the watchdog function cease in STOP mode. Normal operation will be continued when the system is back to RUN mode.

To prevent a watchdog reset, the watchdog timeout counter must be reset before it reaches the end value. This is done by a write to the AWDRST bit in the AWDCTL Register.

Periodic Interrupt

Periodic interrupt is only available in STOP mode. It is enabled by setting the AWDIE bit in the AWDCTL Register. If AWDIE is set, the AWD wakes up the system after a fixed period of time. This time period can be selected with bit AWDR in the AWDCTL Register.

Cyclic Wake-Up

The cyclic wake-up feature is only available in STOP mode. If this feature is enabled, the selected Hall-effect sensor input terminals are switched on and sensed. If a "1" is detected on one of these inputs and the interrupt for the Hall-effect sensors is enabled, a system wake-up is performed. (Switch on main voltage regulator and assert $\overline{IRQ\_A}$ to the microcontroller).

Autonomous Watchdog Control Register (AWDCTL)

Register Name and Address: AWDCTL - $0a

	Bit7	6	5	4	3	2	1	Bit0
Read	0	0	0	ADRE	AWDIE	AWDCC	AWDF	AWDR
Write			AWDRST	ADRE	AWDIE	AWDCC	AWDF	AWDR
Reset	0	0	0	0	0	0	0	0

AWDRST—Autonomous Watchdog Reset Bit

This write-only bit resets the Autonomous Watchdog timeout period. AWDRST always reads 0. Reset clears AWDRST bit.

- 1 = Reset AWD and restart timeout period.
- 0 = No effect.

AWDRE—Autonomous Watchdog Reset Enable Bit

This read/write bit enables resets on AWD timeouts. A reset on the $\overline{RST\_A}$ is only asserted when the device is in RUN mode. AWDRE is one-time setable (write once) after each reset. Reset clears the AWDRE bit.

- 1 = Autonomous watchdog enabled.
- 0 = Autonomous watchdog disabled.

AWDIE—Autonomous Watchdog Interrupt Enable Bit

This read/write bit enables CPU interrupts by the Autonomous Watchdog timeout flag, AWFD. $\overline{IRQ\_A}$ is only asserted when the device is in STOP mode. Reset clears the AWDIE bit.

- 1 = CPU interrupt requests from AWDF enabled.
- 0 = CPU interrupt requests from AWDF disabled.

AWDCC— Autonomous Watchdog Cyclic Check

This read/write bit enables the cyclic check of the two-terminal Hall-effect sensor and the analog inputs. Reset clears the AWDCC bit.

- 1 = Cyclic check of the Hall-effect sensor and analog port.
- 0 = No cyclic check of the Hall-effect sensor and analog port.

AWDF—Autonomous Watchdog Timeout Flag Bit

This read/write flag is set when the Autonomous Watchdog has timed out. Clear AWDF by writing a logic [1] to AWDF. Clearing AWDF also resets the AWD counter and starts a new timeout period. Reset clears the AWDF bit. Writing a logic [0] to AWDF has no effect.

- 1 = AWD has timed out.
- 0 = AWD has not yet timed out.

AWDR—Autonomous Watchdog Rate Bit

This read/write bit selects the clock rate of the Autonomous Watchdog. Reset clears the AWDR bit.

- 1 = Fast rate selected (10 ms).
- 0 = Slow rate selected (20 ms).

Voltage Regulator

The 908E625 chip contains a low-power, low-drop voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts a unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

RUN Mode

During RUN mode the main voltage regulator is on. It provides a regulated supply to all digital sections.

STOP Mode

During STOP mode the STOP mode regulator supplies a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower than the output voltage of the main voltage regulator.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E625, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the "empty" (0xFF) state:

- 0xFD80 0xFDDF Trim and Calibration Values
- 0xFFFE : 0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

PACKAGE THERMAL PERFORMANCE

Figure 21 shows a thermal response curve for a package mounted onto a thermally enhanced PCB.

Note The PCB board is a multi-layer with two inner copper planes (2s2p). The board conforms to JEDEC EIA/JESD 51-5 and JESD51-7. Substrate thickness is 1.60 mm. Top and bottom copper trace layers are 0.7 mm thick, with two inner copper planes of 0.35 mm thickness. Thermal vias have 0.35 mm thick plating.
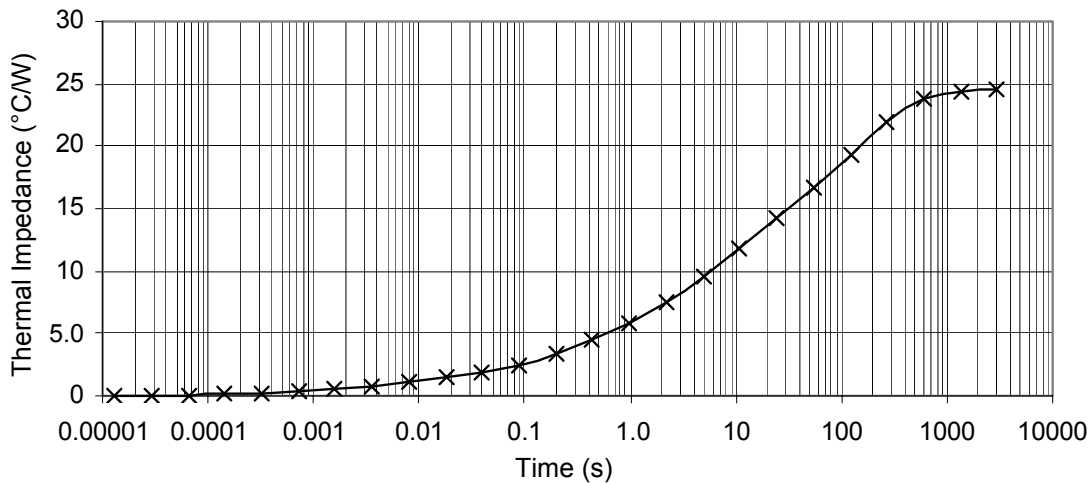
Figure 21. Thermal Response of H-Bridge Driver with Package Soldered to a JEDEC PCB Board

PACKAGE DIMENSIONS

DWB SUFFIX
54-TERMINAL SOIC WIDE BODY EXPOSED PAD
PLASTIC PACKAGE
CASE 1400-01
ISSUE B

Freescale Semiconductor, Inc.
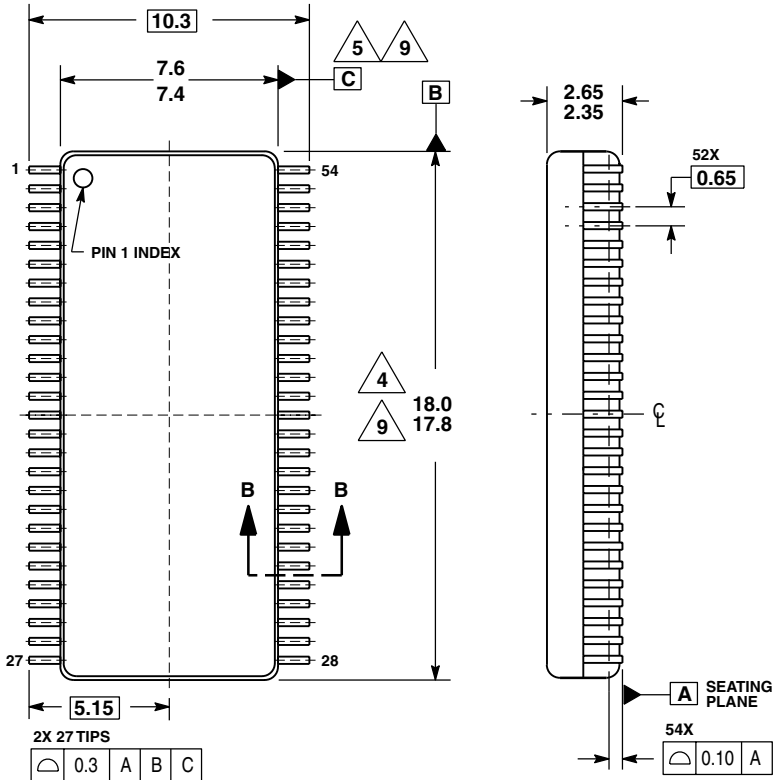
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF HTE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTOM OF THE PLASTIC BODY.

PIN 1 INDEX

10.3
7.6 / 7.4
C
B
18.0 / 17.8
B B
27 28
54 1
5.15
2X 27 TIPS
0.3 A B C

2.65 / 2.35
52X 0.65
54X 0.10 A
A SEATING PLANE

A A
C C

R0.08 MIN
0.25 GAUGE PLANE
0° MIN
(1.43)
8° / 0°
0.9 / 0.5
0.1 / 0.0
SECTION B-B

10.9 / 9.7
0.30 A B C
5.3 / 4.8
0.30 A B C
VIEW C-C

(0.29) BASE METAL
0.30 / 0.25
(0.25)
0.38 / 0.22
PLATING
6
0.13 Ⓜ A B C 8
SECTION A-A
ROTATED 90° CLOCKWISE

908E625
38

MOTOROLA ANALOG INTEGRATED CIRCUIT DEVICE DATA
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NOTES

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