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MOTOROLA

MC33219A

Voice Switched Speakerphone

VOICE SWITCHED SPEAKERPHONE CIRCUIT

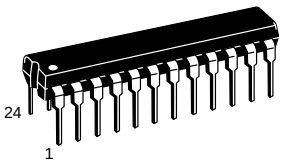
SEMICONDUCTOR TECHNICAL DATA

The Motorola MC33219A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with mute, transmit and receive attenuators, a background monitoring system for both the transmit and receive paths, and level detectors for each path. An AGC system reduces the receive gain on long lines where loop current and power are in short supply. A dial tone detector prevents fading of dial tone. A Chip Disable pin permits conserving power when the circuit is not in use. The volume control can be implemented with a potentiometer.

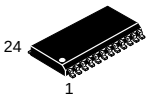
The MC33219A can be operated from a power supply, or from the telephone line, requiring typically 3.2 mA. It can be used in conjunction with a variety of speech networks. Applications include not only speakerphones, but intercoms and other voice switched devices.

The MC33219A is available in a 24 pin narrow body DIP, and a wide body SOIC package.

- Supply Voltage Range: 2.7 to 6.5 V
- Attenuator Range: 53 dB
- Background Noise Monitor for Each Path
- 2 Point Signal Sensing
- Volume Control Range: Typically 40 dB
- Microphone and Receive Amplifiers Pinned Out for Flexibility
- Microphone Amplifier can be Muted
- Mute and Chip Disable are Logic Level Inputs
- Chip Deselect Pin Powers Down the Entire IC
- Ambient Operating Temperature: –40 to +85°C
- 24 Pin Narrow Body (300 mil) DIP and 24 Pin SOIC

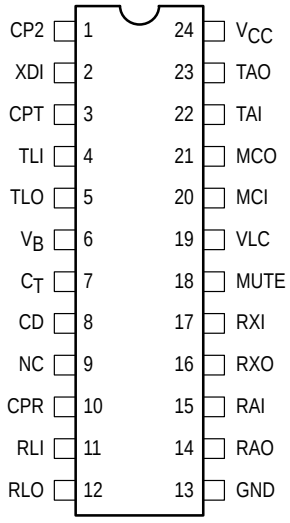


P SUFFIX
PLASTIC PACKAGE
CASE 724



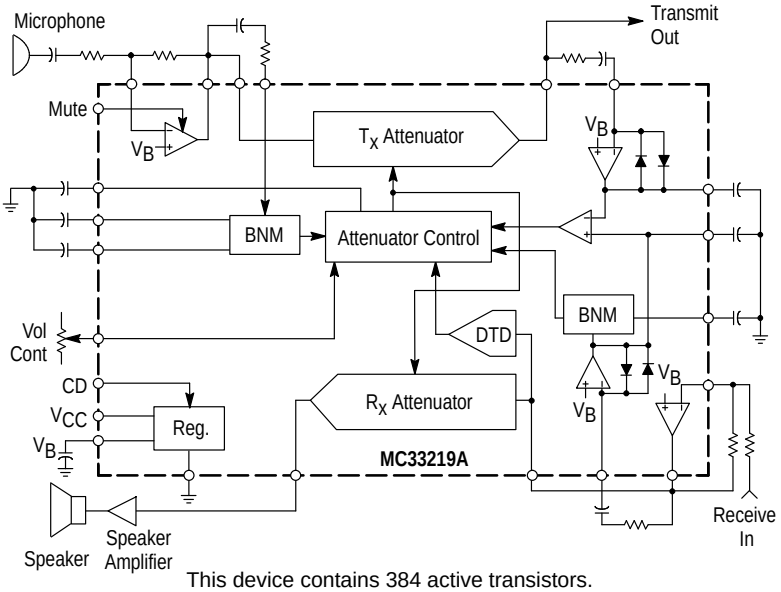
DW SUFFIX
PLASTIC PACKAGE
CASE 751E

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



This device contains 384 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33219ADW	T_A = – 40° to +85°C	SOIC
MC33219AP		Plastic DIP

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MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	–0.5	7.0	Vdc
Any Input	V_{in}	–0.4	V_{CC} + 0.4	Vdc
Maximum Junction Temperature	T_J	–	+150	°C
Storage Temperature Range	T_{stg}	–65	+150	°C

NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (Non–AGC Range) (AGC Range)	V_{CC}	3.5 2.7	– –	6.5 3.5	Vdc
Maximum Attenuator Input Signal	$V_{in(max)}$	–	–	300	mVrms
Volume Control Input (Pin 19)	V_{INVLC}	V_B – 1.1	–	V_B	Vdc
Logic Input Voltage (Pins 8, 18) Low High	V_{INL}	 0 2.0	 – –	 0.8 V_{CC}	Vdc
Operating Temperature Range	T_A	–40	–	85	°C
V_B Output Current (V_{CC} = 5.0 V)	I_{VB}	–	See Figure 12	–	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Current (Enabled, CD ≤ 0.8, V_B Open) Idle Mode T_X Mode R_X Mode	I_{CCE}	 2.0 – –	 3.2 4.2 4.0	 5.0 – –	mA
Supply Current (Disabled, CD = 2.0 V, V_B Open) V_{CC} = 3.0 V V_{CC} = 5.0 V V_{CC} = 6.5 V	I_{CCD}	 – 50 –	 65 110 145	 – 170 –	μA
V_B Output Voltage (I_{VB} = 0, CD = 0) V_{CC} = 2.7 V V_{CC} = 5.0 V V_{CC} = 6.5 V	V_B	 – 2.1 –	 0.9 2.2 3.0	 – 2.3 –	Vdc
V_B Output Resistance (I_{VB} ≤ –1.0 mA)	R_{OVB}	–	600	–	Ω
PSRR @ V_B versus V_{CC}, f = 1.0 kHz, C_{VB} = 100 μF	PSRR	–	57	–	dB
ATTENUATOR CONTROL					
C_T Voltage (with Respect to V_B) R_X Mode (VLC = V_B) Idle Mode T_X Mode	$V_{CT} - V_B$	 – – –	 150 0 –100	 – – –	mV
C_T Source Current (Switching to R_X Mode)	I_{CTR}	–110	–90	–70	μA
C_T Sink Current (Switching to T_X Mode)	I_{CTT}	35	50	65	μA
C_T Idle Current	I_{CTI}	–3.0	0	3.0	μA
Dial Tone Detector Threshold (with Respect to V_B at RAI)	V_{DT}	–40	–20	–8.0	mV
VLC Input Current @ VLC = V_B VLC = V_B – 1.0 V	I_{VLC}	 – –8.0	 0 –6.0	 – –3.0	μA
VLC Input Resistance	R_{VLC}	–	167	–	kΩ

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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2.)

Characteristic	Symbol	Min	Typ	Max	Unit
ATTENUATORS					
Receive Attenuator Gain (f = 1.0 kHz)					dB
Full Volume					
R_X Mode	G_{RX}	3.0	6.7	9.0	
T_X Mode	G_{RXT}	–49	–46	–43	
Idle Mode	G_{RXI}	–28	–25	–22	
Range (R_X to T_X Mode)	ΔG_{RX}	50	53	56	
Volume Control Range (R_X Mode Only, VLC Varied from V_B to (V_B – 1.0 V))	V_{CR}	34	40	46	dB
AGC Attenuation Range (V_{CC} = 3.5 to 2.7 V, Receive Mode Only, VLC = V_B)	G_{AGC}	20	26	36	dB
Transmit Attenuator Gain (f = 1.0 kHz)					dB
T_X Mode	G_{TX}	3.0	6.7	9.0	
R_X Mode	G_{TXR}	–49	–46	–43	
Idle Mode	G_{TXI}	–19	–16	–13	
Range (T_X to R_X Mode)	ΔG_{TX}	50	53	56	
RAO, TAO Output Current Capability	I_{OATT}				mA peak
$V_{CC} \geq 3.0$ V		–	2.5	–	
$V_{CC} < 3.0$ V		–	0.7	–	
RAO Offset Voltage with Respect to V_B	V_{RAO}				mVdc
R_X Mode		–	120	–	
Idle Mode		–	0	–	
T_X Mode		–	–10	–	
TAO Offset Voltage with Respect to V_B	V_{TAO}				mVdc
R_X Mode		–	0	–	
Idle Mode		–	–8.0	–	
T_X Mode		–	70	–	
RAI, TAI Input Impedance (V_{in} < 300 mVrms)	R_{INATT}	–	100	–	kΩ
RAI, TAI Input Offset Voltage with Respect to V_B	V_{INATT}	–	0	–	mVdc
MICROPHONE AMPLIFIER (Pins 20, 21)					
Output Offset with Respect to V_B (RF = 300 kΩ)	MCO_{VOS}	–	–9.0	–	mVdc
Input Bias Current (Pin 20)	I_{MBIAS}	–	–30	–	nA
Open Loop Gain (f < 100 Hz)	V_{VOLM}	–	70	–	dB
Gain Bandwidth	GBW_M	–	1.5	–	MHz
Maximum Output Voltage Swing (1% THD)	V_{OMAX}	–	4.1	–	Vp–p
Maximum Output Current Capability	I_{OMCO}	–	2.0	–	mA peak
Muting (Δ Gain) – RF = 300 kΩ	GMT	70	78	–	dB
RF = 100 kΩ		–	68	–	
RECEIVE AMPLIFIER (Pins 16, 17)					
Output Offset with Respect to V_B (RF = 10 kΩ)	RXO_{VOS}	–	–1.0	–	mVdc
Input Bias Current (Pin 17)	I_{RBIAS}	–	–30	–	nA
Open Loop Gain (f < 100 Hz)	A_{VOLR}	–	70	–	dB
Gain Bandwidth	G_{BWR}	–	1.5	–	MHz
Maximum Output Voltage Swing (1% THD)	V_{OMAX}	–	4.1	–	Vp–p
Maximum Output Current Capability	I_{ORXO}	–	2.0	–	mA peak

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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted. See Figure 2)

Characteristic	Symbol	Min	Typ	Max	Unit
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
T_X–R_X Switching Threshold (Pins 4, 11)	I_{TH}	0.8	1.0	1.2	µA
CPR, CPT Output Resistance (for Pulldown)	R_{CP}	–	5.0	–	Ω
CPR, CPT Leakage Current	I_{CPLK}	–	–0.2	–	µA
CPR, CPT Nominal DC Voltage (No Signal)	V_{CP}	–	1.9	–	Vdc
TLO, RLO, CP2 Source Current (@ V_B – 1.0 V)	I_{LDOH}	–	–2.0	–	mA
TLO, RLO, CP2 Output Resistance	R_{LD}	–	500	–	Ω
TLO, RLO, CP2 Sink Current (@ V_B + 1.0 V)	I_{LDOL}	–	2.0	–	µA
MUTE INPUT (Pin 18)					
Switching Threshold (See Text)	V_{THMT}	–	1.0–1.4	–	Vdc
Input Resistance (V_{in} = 0.85 V)	R_{MT}	70	115	160	kΩ
Input Current (V_{in} = 5.0 V)	I_{MT}	–	75	–	µA
Timing To Mute To Enable	 t_{MT} t_{ENM}	 – –	 1.5 5.0	 – –	µs
CD INPUT (Pin 8)					
Switching Threshold	V_{THCD}	–	1.5	–	Vdc
Input Resistance (V_{in} = 0.8 V)	R_{CD}	150	235	350	kΩ
Input Current (V_{in} = 5.0 V)	I_{CD}	–	40	–	µA
Timing To Disable To Enable	 t_{CD} t_{ENC}	 – –	 5.0 See Figure 22	 – –	µs
SYSTEM DISTORTION (See Figure 1)					
Microphone Amplifier + T_X Attenuator Distortion	THD_T	–	0.05	3.0	%
Receive Amplifier + R_X Attenuator Distortion	THD_R	–	0.05	3.0	%

TYPICAL TEMPERATURE PERFORMANCE

Characteristic	–40°C	0°C	25°C	85°C	Unit
Power Supply Current Enabled, V_B Open Disabled, V_B Open	 3.18 131	 3.23 119	 3.23 110	 3.12 121	 mA µA
V_B Output Voltage (I_{VB} = 0)	2.09	2.17	2.22	2.31	Vdc
CT Source Current Switching to R_X Mode	–80	–87	–90	–90	µA
CT Sink Current Switching to T_X Mode	43	47	50	51	µA
Attenuator “On” Gain	6.9	6.8	6.7	6.6	dB
Attenuator Range	53	53	53	53	dB
Volume Control Range (R_X Mode Only, V_{LC} Varied from V_B to (V_B – 1.0 V))	36	39	40	41	dB
AGC Attenuation Range	32	24	26	30	dB

Temperature data is typical performance only, based on sample characterization, and does not provide guaranteed limits over temperature.

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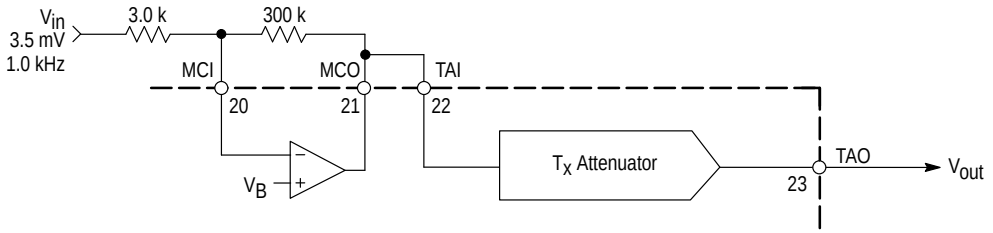
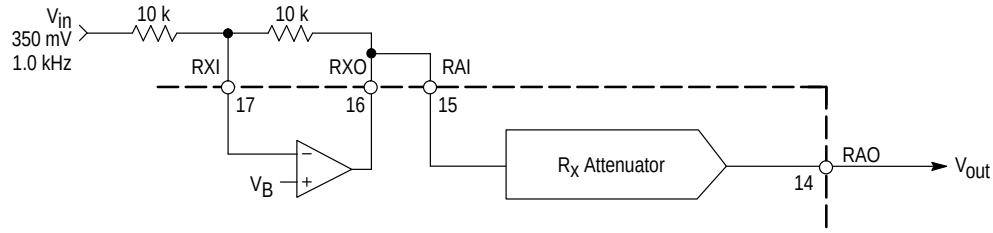
Figure 1. System Distortion Test



NOTE: T_X Attenuator forced to transmit mode.



NOTE: R_X Attenuator forced to receive mode.

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PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	CP2	A capacitor at this pin stores voltage representing the transmit background noise and speech levels for the background noise monitor.
2	XDI	Input to the transmit background noise monitor.
3	CPT	An RC sets the time constant for the transmit background noise monitor.
4	TLI	Input to the transmit level detector.
5	TLO	Output of the transmit level detector.
6	V_B	A mid–supply reference voltage, and analog ground for the amplifiers. This must be well bypassed for proper power supply rejection.
7	C_T	An RC sets the switching time between transmit, receive and idle modes.
8	CD	Chip Disable (Logic Input). When low, the IC is active. When high, the entire IC is powered down and non–functional, except for V_B. Input impedance is nominally 125 kΩ.
9	NC	No internal connection.
10	CPR	An RC sets the time constant for the receive background noise monitor.
11	RLI	Input to the receive level detector.
12	RLO	Output of the receive level detector.
13	GND	Ground pin for the entire IC.
14	RAO	Output of the receive attenuator.
15	RAI	Input to the receive attenuator and the dial tone detector. Input impedance is nominally 100 kΩ.
16	RXO	Output of the receive amplifier.
17	RXI	Inverting input of the receive amplifier. Bias current flows out of the pin.
18	MUTE	Mute Input (Logic Input). A logic low sets normal operation. A logic high mutes the microphone amplifier only. Input impedance is nominally 67 kΩ.
19	VLC	Volume control. When VLC = V_B, maximum receive gain is set when in the receive mode. When VLC = V_B – 1.0 V, receive gain is down ≈ 40 dB. No effect in the transmit or idle mode. Current flow is out of the pin. Input impedance is nominally 167 kΩ.
20	MCI	Inverting input of the microphone amplifier. Bias current flows out of the pin.
21	MCO	Output of the microphone amplifier.
22	TAI	Input of the transmit attenuator. Input impedance is nominally 100 kΩ.
23	TAO	Output of the transmit attenuator.
24	V_{CC}	Power Supply Pin. Operating Range is 2.7 V to 6.5 Vdc. Bypassing is required.

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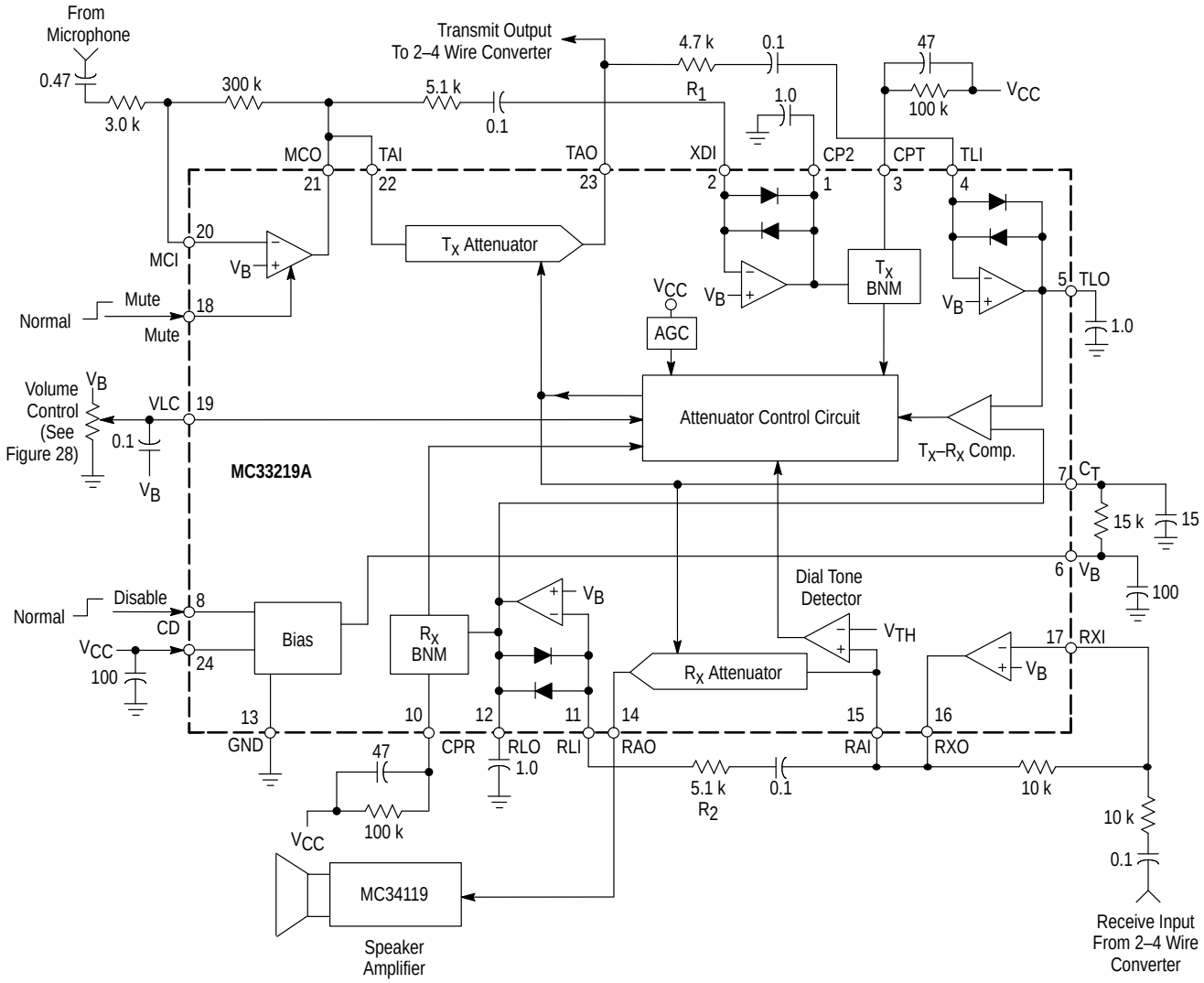
Figure 2. MC33219A Block Diagram and Test Circuit



NOTES: 1. All capacitors are in µF unless otherwise noted.
2. Values shown are suggested initial values only. See Applications Information for circuit adjustments.

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Figure 3. Attenuator Gain versus V_{CT} (Pin 7)

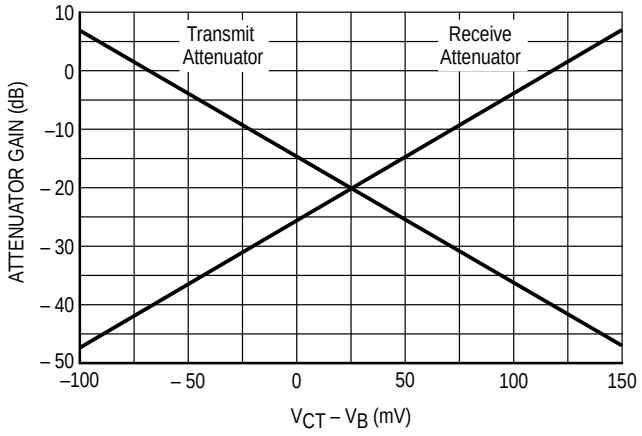

Figure 4. Receive Attenuator versus Volume Control

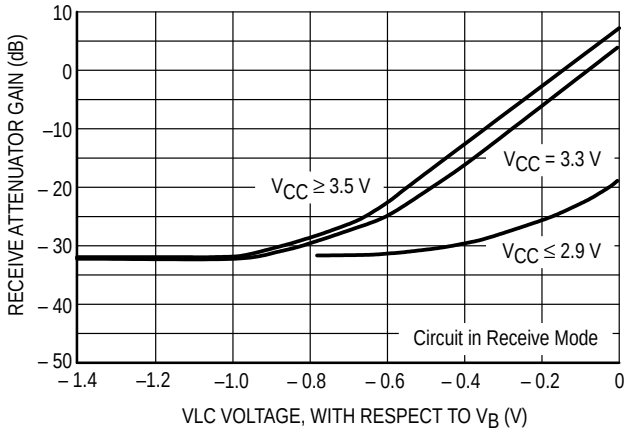

Figure 5. Receive Gain versus V_{CC}

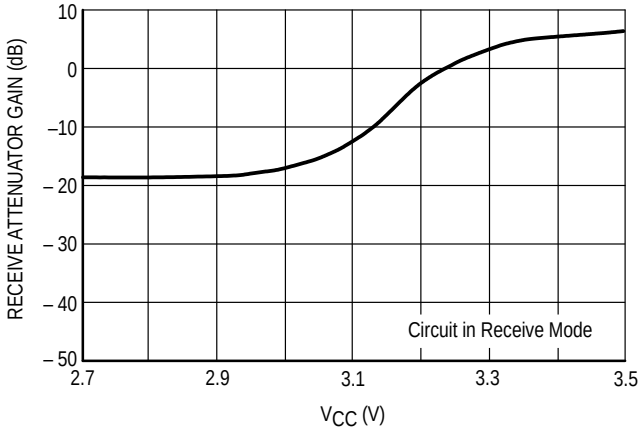

Figure 6. Level Detector DC Transfer Characteristics

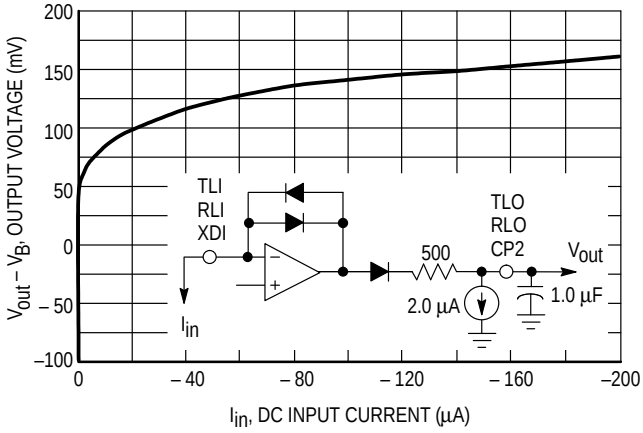

Figure 7. Level Detector AC Transfer Characteristics

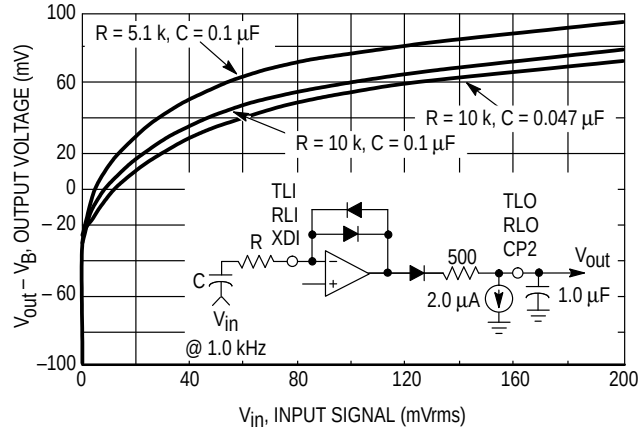

Figure 8. Level Detector AC Transfer Characteristics versus Frequency

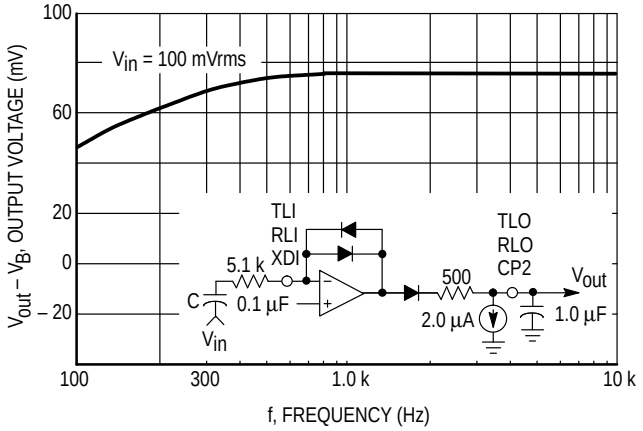

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Figure 9. CD Input Characteristics (Pin 8)

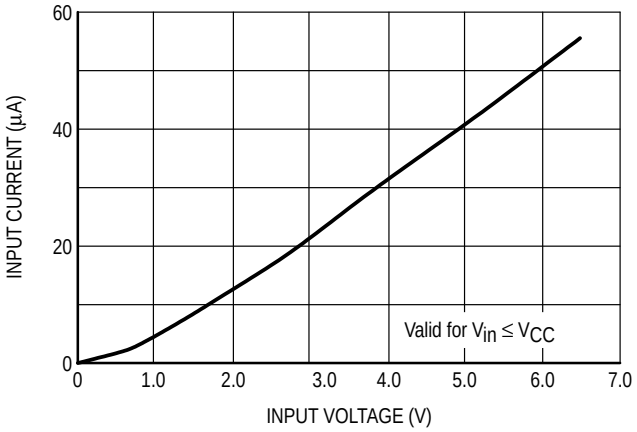

Figure 10. Mute Input Characteristics (Pin 18)

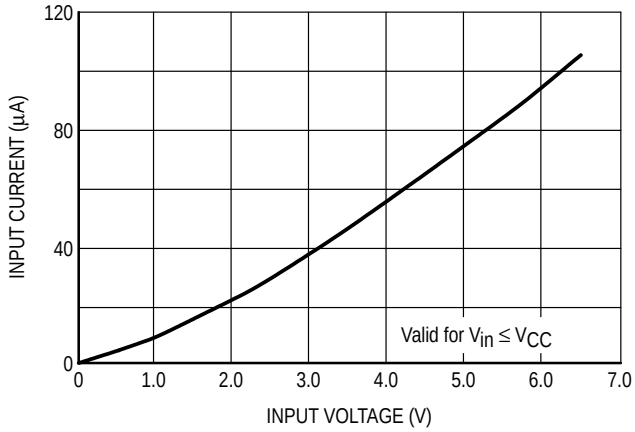

Figure 11. Power Supply Current

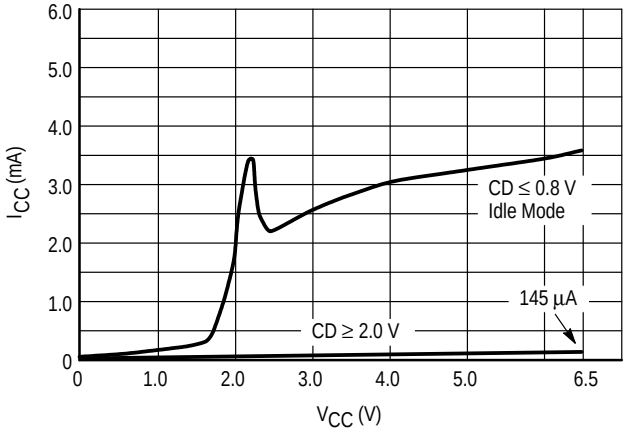

Figure 12. V_B Output Characteristics

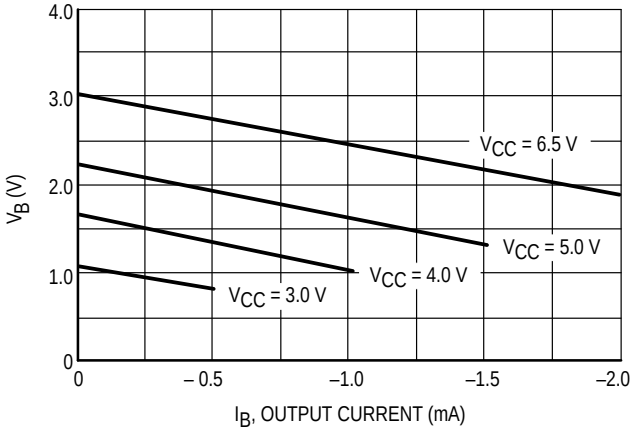

Figure 13. V_B Power Supply Rejection versus Frequency and V_B Capacitor

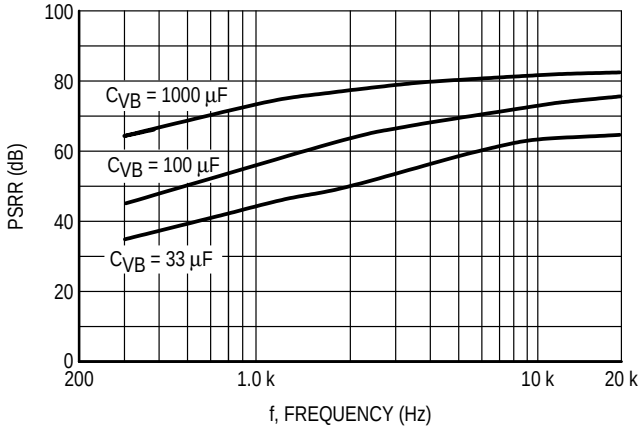

Figure 14. Receive Amp and Microphone Amp Output Swing

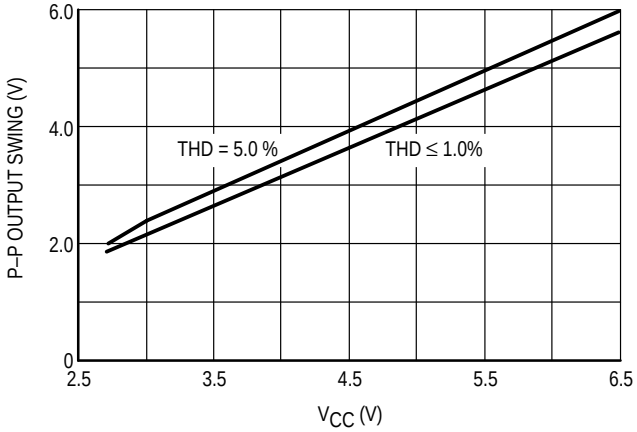

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Figure 15. Microphone Amplifier Muting versus Feedback Resistor

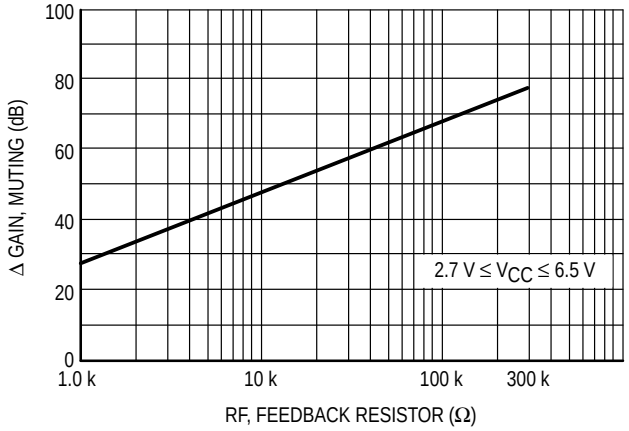


Figure 16. VLC Input Current (Pin 19)

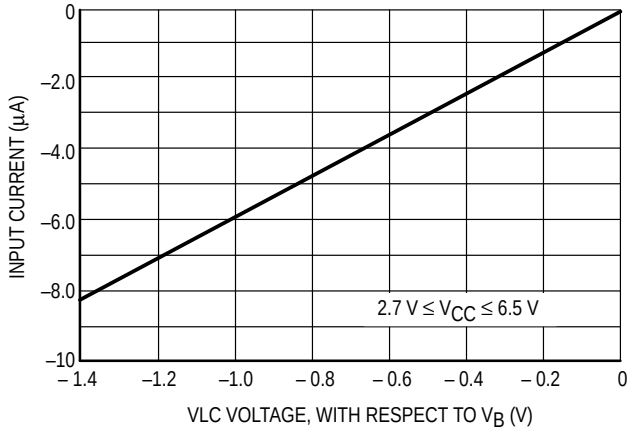
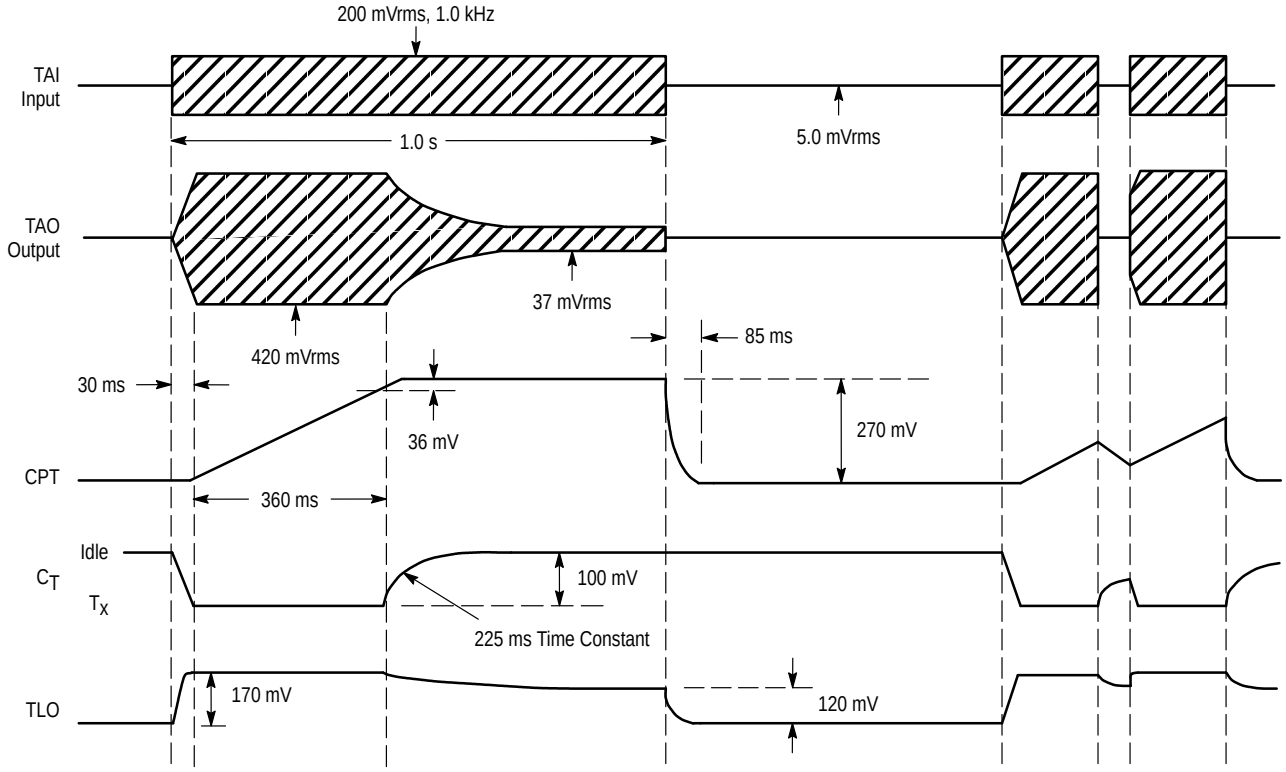


Figure 17. Idle ⟷ Transmit Timing



NOTE: Refer to Figure 2 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

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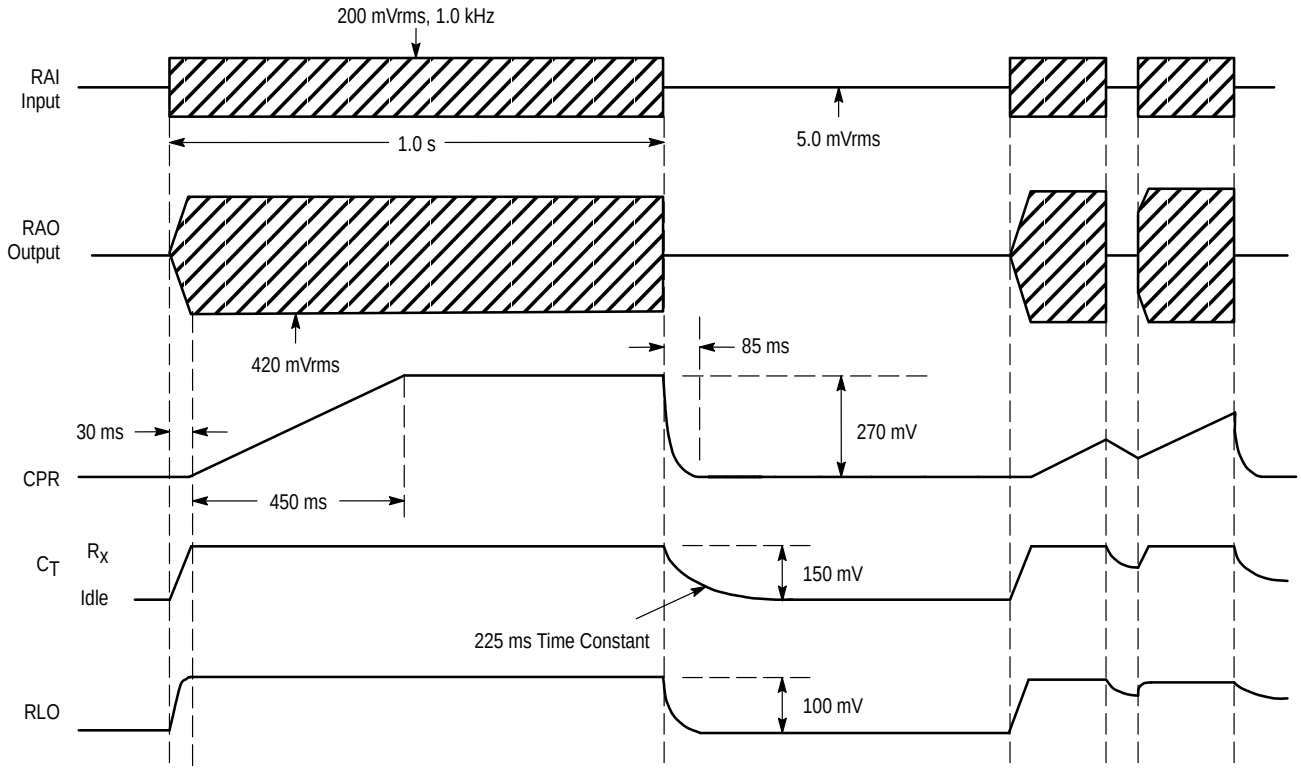
Figure 18. Idle ⟷ Receive Timing



NOTE: Refer to Figure 2 for component values. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

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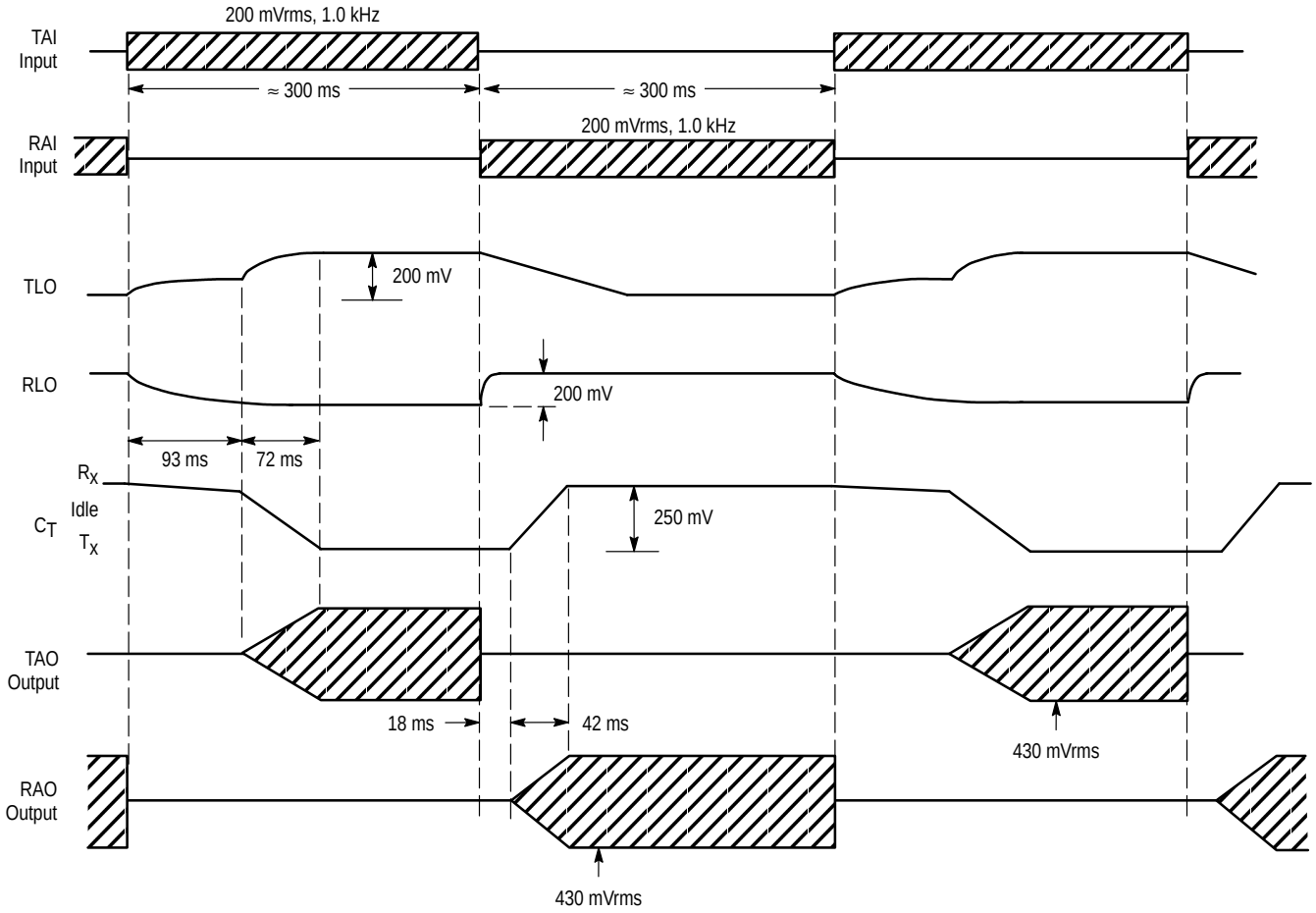
Figure 19. Transmit ⟷ Receive Timing (Short Cycle Timing)



NOTE: 1. External component values are those shown in Figure 2.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.

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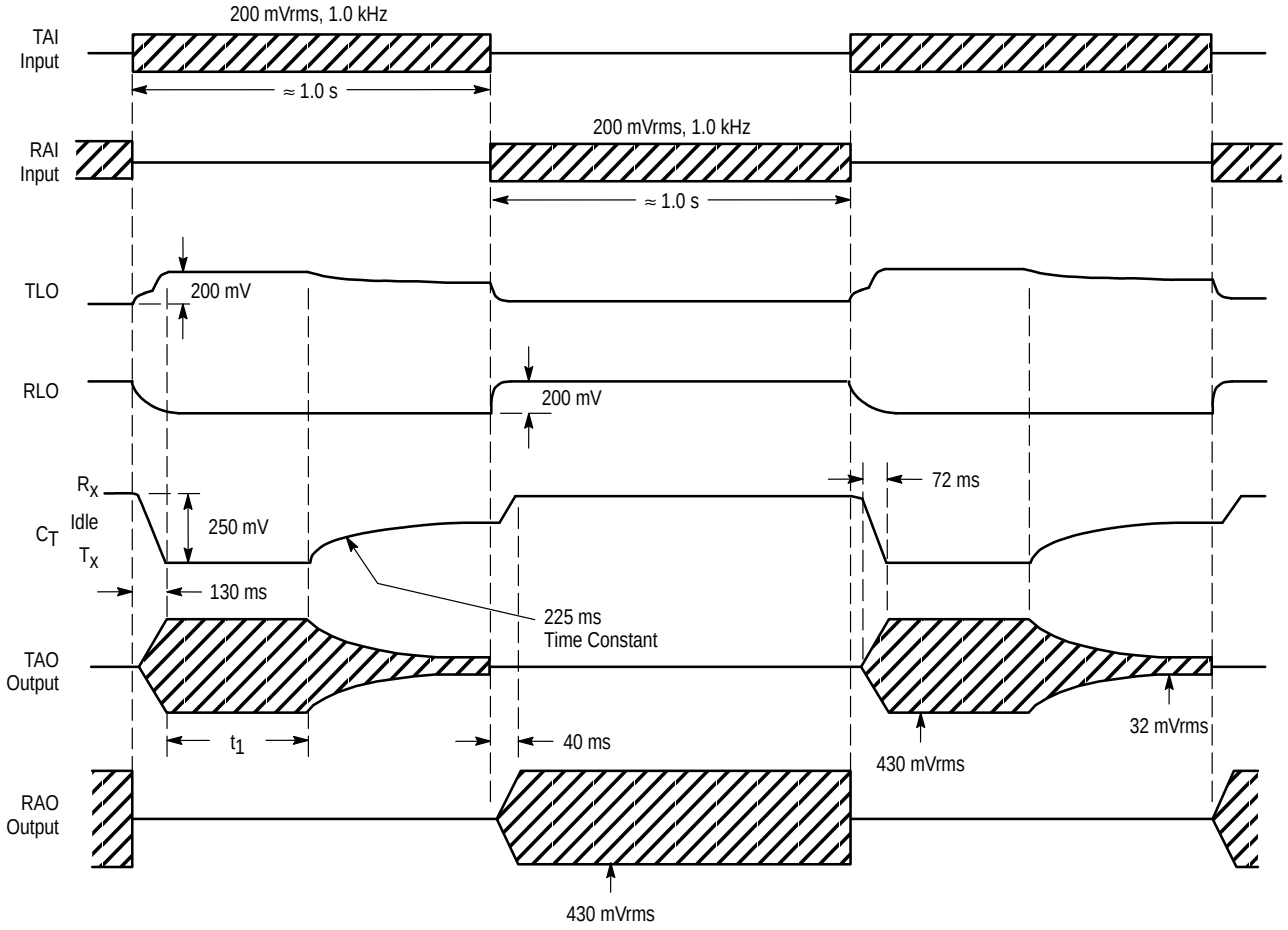
Figure 20. Transmit ⟷ Receive Timing (Long Cycle Timing)



NOTE: 1. External component values are those shown in Figure 2.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.
3. Time t_1 depends on the ratio of the on–off amplitude of the signal at TAI.

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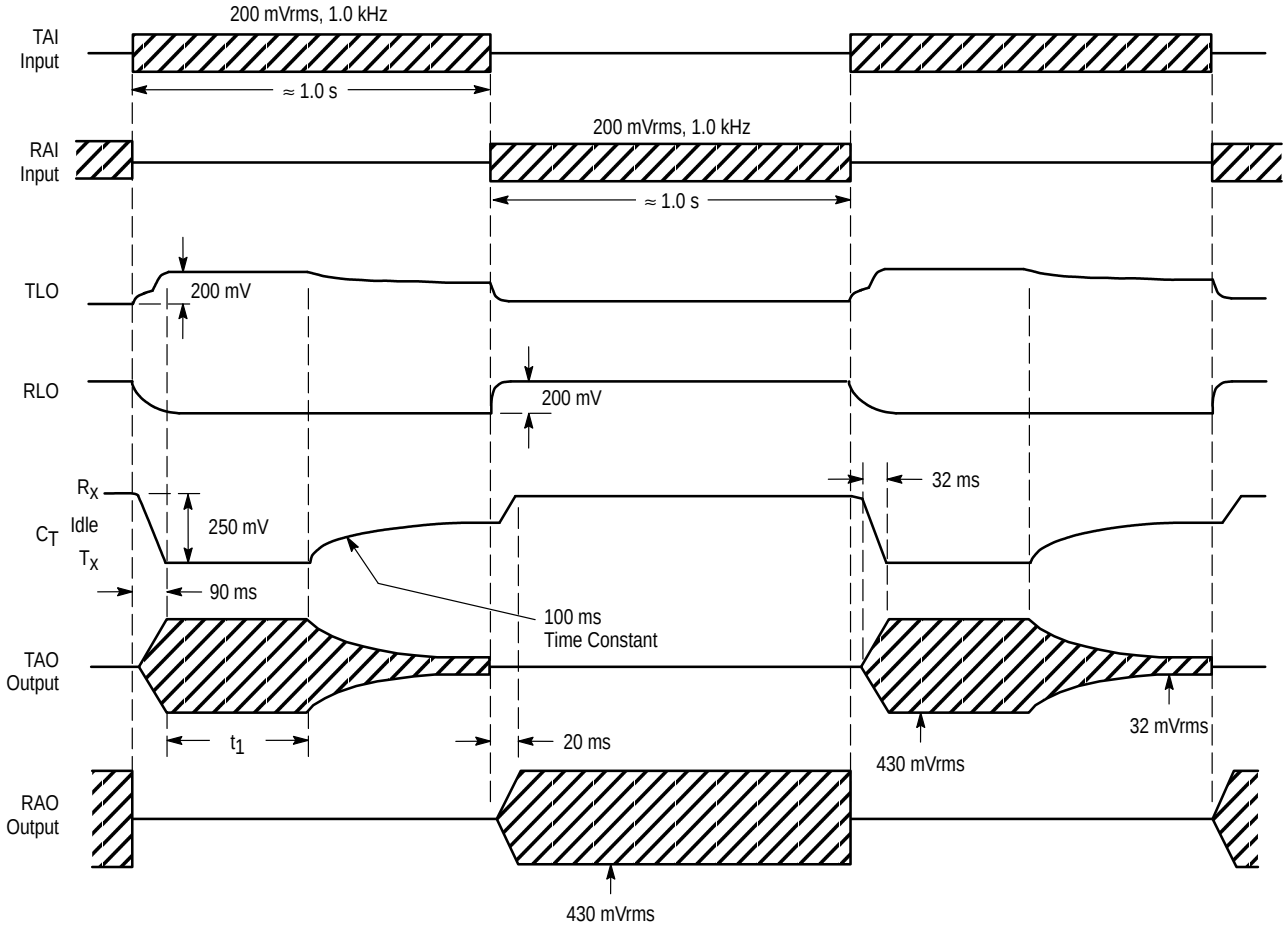
Figure 21. Transmit ⟷ Receive Timing
(Long Cycle Timing)



NOTE: 1. External component values are those shown in Figure 2, except the capacitor at C_T is 6.8 μF.
2. Timing and output amplitudes shown are nominal, and are for the indicated input signal and component values. Actual timing and outputs will vary with the application.
3. Time t_1 depends on the ratio of the on–off amplitude of the signal at TAI.

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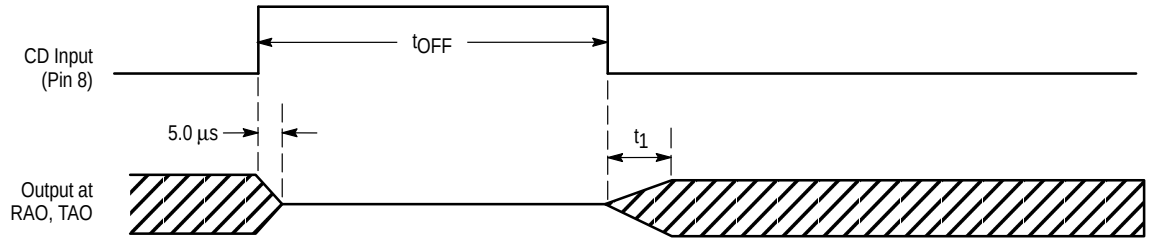
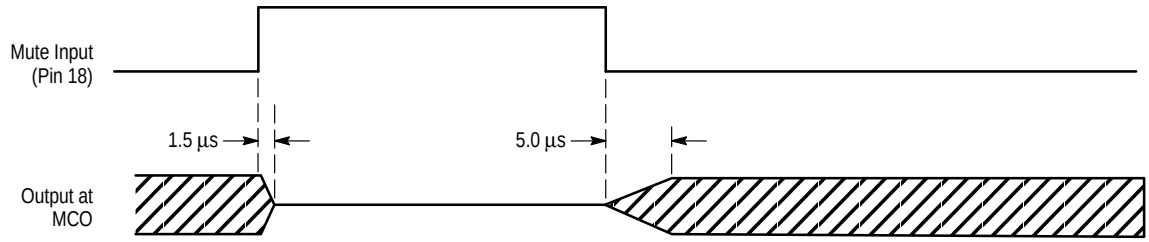
Figure 22. Chip Disable Timing



NOTE: Enable time t_1 depends on the length of t_{OFF} according to the following chart:

	t_1	
t_{OFF}	to 60%	to 100%
≤ 50 ms	–	5.0 µs
100 ms	5.0 µs	14 ms
500 ms	64 ms	72 ms
5.0 s	80 ms	100 ms

Figure 23. Mute Timing



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FUNCTIONAL DESCRIPTION

Introduction

The fundamental difference between the operation of a speakerphone and a telephone handset is that of half–duplex versus full–duplex. The handset is full duplex, meaning conversation can occur in both directions (transmit and receive) simultaneously. This is possible due to both the low sound level at the receiver, and the fact that the acoustic coupling from the earpiece to the mouthpiece is almost non–existent (the receiver is normally held against a person's ear). The loop gain from the receiver to the microphone and through the circuit is well below that needed to sustain oscillations.

A speakerphone, on the other hand, has higher gain levels in both the transmit and receive paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the speakerphone circuit. The loop is formed by the hybrid, the acoustic coupling (speaker to microphone), and the transmit and receive paths (between the hybrid and the speaker/microphone). The only practical and economical method used to date is to design the speakerphone to function in a half duplex mode; i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking (in reality, who is talking louder), switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands–free" mode, eliminating the need for a "push–to–talk" switch.

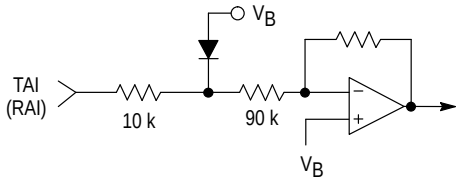
The MC33219A provides the necessary circuitry to perform a voice switched, half duplex, speakerphone function. The IC includes transmit and receive attenuators, pre–amplifiers, level detectors and background noise monitors for each path. An attenuator control circuit automatically adjusts the gain of the transmit and receive attenuators based on the relative strengths of the voice signals present, the volume control, and the supply voltage (when low). The detection sensitivity and timing are externally controllable. Please refer to the Block Diagram (Figure 2) when reading the following sections.

Transmit and Receive Attenuators

The transmit and receive attenuators are complementary, performing a log–antilog function. When one is at maximum gain (≈ 6.7 dB), the other is at maximum attenuation (≈ –46 dB); they are never both fully on or fully off. Both attenuators are controlled by a single output from the Attenuator Control Circuit which ensures the sum of their gains will remain constant at a typical value of –40 dB. Their purpose is to provide the half–duplex operation required in a speakerphone.

The attenuators are non–inverting, and have a usable bandwidth of 50 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 100 kΩ (see Figure 24), and the input signal should be limited to 300 mVrms (850 mV p–p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. Both the input and output are biased at ≈ V_B. The output impedance is <10 Ω until the output current limit (see specs) is reached.

Figure 24. Attenuator Input Stage



The attenuators are controlled by the single output of the Attenuator Control Circuit, which is measurable at C_T (Pin 7). When the circuit detects speech signals directing it to the receive mode (by means of the level detectors described below), an internal current source of 90 μA will charge the C_T capacitor to a voltage positive with respect to V_B (see Figure 25). At the maximum volume control setting, this voltage will be approximately 150 mV, and the receive attenuator will have a gain of 6.7 dB. When the circuit detects speech signals directing it to the transmit mode, an internal current source of 50 μA will take the capacitor to approximately –100 mV with respect to V_B (the transmit attenuator will have a gain of 6.7 dB). When there is no speech present in either path, the current sources are shut off, and the voltage at C_T will decay to be equal to V_B. This is the idle mode, and the attenuators' gains are nearly halfway between their fully ON and fully OFF positions (–25 dB for the R_X attenuator, –16 dB for the T_X attenuator). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode, and its response.

The inputs to the Attenuator Control Section are six: The T_X–R_X comparator operated by the level detectors, two background noise monitors, the volume control, the dialtone detector, and the AGC circuit. These six functions are described as follows.

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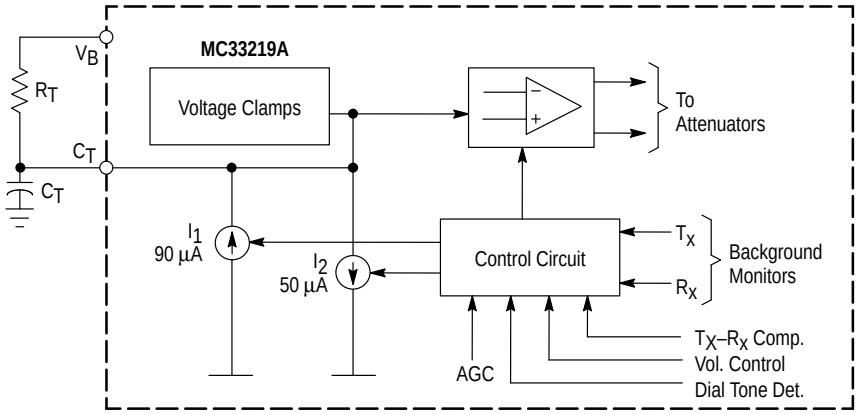
Figure 25. C_T Attenuator Control Circuit

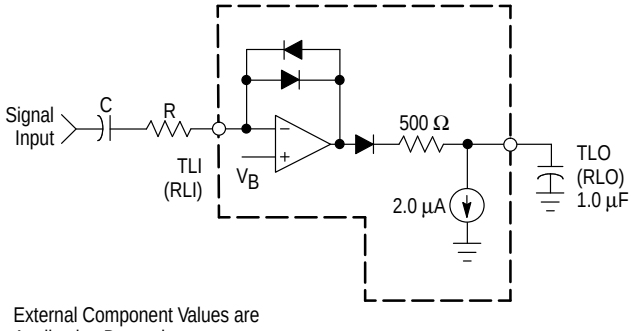


Level Detectors

There are two identical level detectors: one on the receive side and one on the transmit side (refer to Figure 26). Each level detector is a high gain amplifier with back–to–back diodes in the feedback path, resulting in non–linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 6, 7 and 8 for their DC and AC transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at their input (TLI and RLI). The output charges an external capacitor through a diode and limiting resistor, thus providing a DC representation of the input AC signal level. The outputs have a quick rise time (determined by the capacitor and an internal 500 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the two outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, the outputs of the two level detectors drive the T_X–R_X comparator. The comparator's output state depends on whether the transmit or receive speech signal is stronger, as sensed by the level detectors. The Attenuator Control Circuit uses this signal, along with the background noise monitors, to determine which mode to set.

Figure 26. Level Detector



External Component Values are Application Dependent.

Background Noise Monitors

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal). There are two background noise monitors: one for the receive path and one for the transmit path. Refering to Figure 27, each is operated on by a level detector, which provides a DC voltage representative of the combined speech and noise level. However, the peaks, valleys, and bursts, which are characteristic of speech, will cause the DC voltage (at CP2 or RLO) to increase relatively quickly, causing the output of the next amplifier to also rise quickly. If that increase exceeds the 36 mV offset, and at a speed faster than the time constant at CPT (CPR), the output of the last comparator will change, indicating the presence of speech to the attenuator control circuit. This will keep the circuit in either the transmit or the receive mode, depending on which side has the stronger signals. When a new continuous signal is applied, the time constant at CPT (CPR) determines how long it takes the circuit to decide that the new sound is continuous, and is therefore background noise. The system requires that the average speech signal be stronger than the background noise level (by 6.0–7.0 dB) for proper speech detection.

When only background noise is present in both paths, the output of the monitors will indicate the absence of speech, allowing the circuit to go to the idle mode.

AGC Circuit

In the receive mode only, the AGC circuit decreases the gain of the receive attenuator when the supply voltage at V_{CC} falls below 3.5 V, according to the graph of Figure 5. The gain of the transmit path changes in a complementary manner.

The purpose of this feature is to reduce the power (and current) used by the speaker when the speakerphone is powered by the phone line, and is connected to a long telephone line, where the available power is limited. Reducing the speaker power controls the voltage sag at V_{CC}, reduces clipping and distortion at the speaker output, and prevents possible erratic operation.

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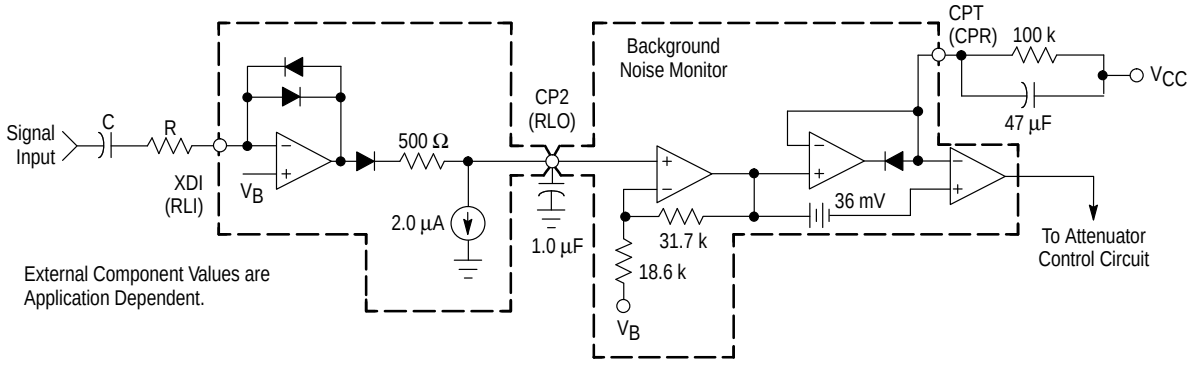
Figure 27. Background Noise Monitor



Volume Control

The volume control input at VLC (Pin 19) is sensed as a voltage with respect to V_B. The volume control affects the attenuators in the receive mode ***only***. It has no effect in the idle or transmit modes.

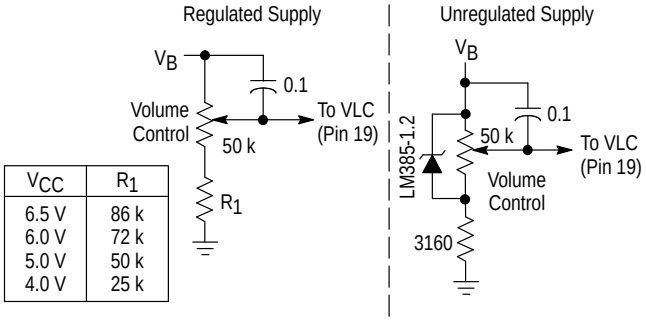
By varying the voltage at the VLC pin (Pin 19), the volume control varies the gain of the attenuators. Maximum receive attenuator gain (6.7 dB) occurs when VLC = V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced, and the transmit attenuator gain increases in a complementary manner. The usable range of the VLC pin is ≈ 1.1 V for $V_{CC} \geq 3.5$ V, providing a range of ≈ 40 dB (see Figure 4). At $V_{CC} < 3.5$ V, the range is reduced due to the lower V_B voltage, and the AGC function.

The configuration of the external volume control potentiometer circuit depends on whether the V_{CC} supply voltage is regulated or if it varies, such as in a phone line powered circuit (see Figure 28). If the supply voltage is regulated, the circuit on the left can be used. The value of the lower resistor (R_1) depends on the value of V_{CC}, so that Pin 19 can be varied from V_B to ≈ 1.1 V below V_B.

In a phone line powered circuit, the value of V_{CC}, and consequently V_B, will vary with line length and with the amount of sound at the speaker. In this case, the circuit on the right side of Figure 28 must be used to provide a fixed reference voltage for the potentiometer. With this circuit, the volume setting will not vary when V_{CC} is ≥ 3.5 V. As V_{CC} falls below 3.5 V, the zener diode will drop out of regulation, but the AGC circuit will ensure that instabilities do not occur.

The bias current at VLC flows out of the pin and depends on the voltage at the pin (see Figure 16). The capacitor from VLC to V_B helps reduce any effects of ripple or noise on V_B.

Figure 28. Volume Control



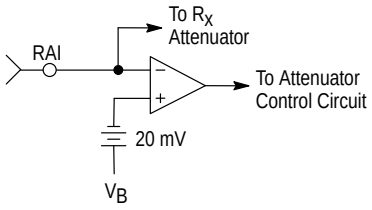
V_{CC}	R_1
6.5 V	86 k
6.0 V	72 k
5.0 V	50 k
4.0 V	25 k

Dial Tone Detector

When the speakerphone is initially taken off–hook, the dial tone signal will switch the circuit to the receive mode. However, since the dial tone is a continuous signal, the MC33219A would consider it as background noise rather than speech, and would therefore switch from receive to idle, causing the dial tone sound level to fade. The dial tone detector prevents the fading by disabling the background noise monitor.

The dial tone detector is a comparator with one side connected to the receive attenuator input (RAI), and the other input connected to V_B with a –20 mV offset (see Figure 29). If the circuit is in the receive mode and the incoming signal has peaks greater than 20 mV (14 mV rms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control. **NOTE:** The dial tone detector is **not** a frequency discriminating circuit.

Figure 29. Dial Tone Detector



Microphone Amplifier, Mute

The microphone amplifier (Pins 20, 21) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op amps, the amplifier has an all NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 70 dB (f < 100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing, for 1.0% or less distortion, is shown in Figure 14. The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at MCI is typically 30 nA out of the pin.

The mute function (Pin 18), when activated, will reduce the gain of the amplifier by shorting the external feedback resistor (RMF in Figure 30). The amplifier is not disabled in this mode; MCO remains a low impedance output, and MCI remains a virtual ground at V_B. The amount of muting (the

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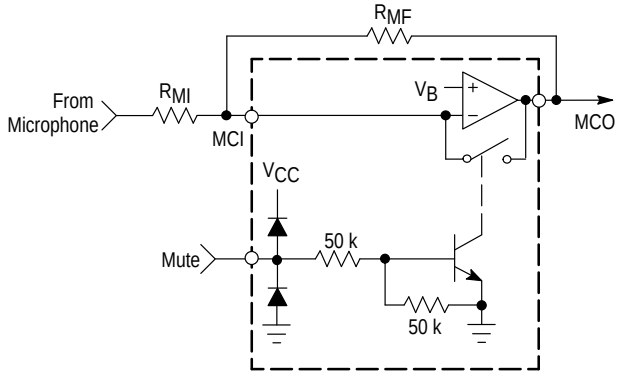
change in gain) depends on the value of the external feedback resistor, according to the graph of Figure 15. Muting occurs as the mute input pin is taken from ≈ 1.0 V to ≈ 1.4 V. The voltage on this pin must be ≤ 0.8 V for normal operation, and ≥ 2.0 V for muting. See Figure 10 for input current requirements. The input must be kept within the range of V_{CC} and GND. If the input is taken more than 0.4 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. If the mute function is not used, the pin should be grounded.

Figure 30. Microphone Amplifier and Mute



Receive Amplifier

The receive amplifier (Pins 16, 17) has the non–inverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op amps, the amplifier has an all NPN output stage, which maximizes phase margin and gain–bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 70 dB (f < 100 Hz), and the gain–bandwidth is typically 1.5 MHz. The maximum p–p output swing for 1.0% or less distortion is shown in Figure 14. The output impedance is <10 Ω until current limiting is reached (typically 2.0 mA peak). The input bias current at RXI is typically 30 nA out of the pin.

Power Supply, V_B and Chip Disable

The power supply voltage at Pin 24 is to be between 3.5 and 6.5 V for normal operation, and down to 2.7 V with the AGC in effect (see AGC section). The supply current required is typically 3.2 mA in the idle mode, and ≈ 4.0 mA in the transmit and receive modes. Figure 11 shows the supply current for both the normal and disabled modes.

The output voltage at V_B (Pin 6) is approximately equal to $(V_{CC} - 0.7)/2$, and provides an AC ground for the internal amplifiers and the system. The output impedance at V_B is approximately 600 Ω, and in conjunction with the external capacitor at V_B forms a low pass filter for power supply noise rejection. The choice of the V_B capacitor size is application dependent based on whether the circuit is powered by the telephone line or a regulated supply. See Figure 13 for PSRR information. Since V_B biases the microphone and receive amplifiers, the amount of supply rejection at their outputs is a function of the rejection at V_B, as well as the gains of the amplifiers.

The amount of current which can be sourced out of the V_B pin depends on the V_{CC} voltage (see Figure 12). Drawing current in excess of that shown in Figure 12 will cause V_B to drop low enough to disrupt the circuit's operation. This pin can sink ≈ 100 μA when enabled, and 0 μA when disabled.

The Chip Disable (Pin 8) permits powering down the IC for power conservation. With CD between 0 and 0.8 V, normal operation is in effect. With CD between 2.0 V and V_{CC}, the IC is powered down, and the supply current drops to about 110 μA (at V_{CC} = 5.0 V, see Figure 11). When CD is high, the microphone and receive amplifiers, the level detectors, and the two attenuators are disabled (their outputs go to a high impedance). The background noise monitors are disabled, and Pins 3 and 10 will go to V_{CC}. The V_B output, however, remains active, except that it cannot sink any current.

The CD input must be kept within the range of V_{CC} and GND. See Figure 9 for input current requirements. If the input is taken more than 0.4 V above V_{CC} or below GND excessive currents will flow, and the device's operation will be distorted. If the disable function is not used, the pin should be connected to ground.

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APPLICATIONS INFORMATION

Switching and Response Time Theory

The switching time of the MC33219A circuit is dominated first by the components at C_T (Pin 7, see Figure 2), and second by the capacitors at the level detector outputs (RLO, TLO).

The transition time to receive or to transmit mode from either idle or the other mode is determined by the capacitor at CT, along with the internal current sources (refer to Figure 25). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

When switching from idle to receive, ΔV = 150 mV, I = 90 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 25 ms. When switching from idle to transmit, ΔV = 100 mV, I = 50 μA, the C_T capacitor is 15 μF, and ΔT calculates to ≈ 30 ms.

When the circuit switches to idle, the internal current sources are shut off, and the time constant is determined by the C_T capacitor and RT, the external resistor (see Figure 25). With C_T = 15 μF, and RT = 15 kΩ, the time constant is ≈ 225 ms, giving a total switching time of ≈ 0.68 s (for 95% change). The switching period to idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the "decay to idle" period, the quicker the switching time, since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

When the circuit switches directly from receive to transmit (or vice versa), the total switching time depends not only on the components and currents at the C_T pin, but also on the response of the level detectors, the relative amplitude of the two speech signals, and the mode of the circuit, since the two level detectors are connected differently to the two attenuators.

The rise time of the level detector's outputs (RLO, TLO) is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit (in transmit or receive) during the normal pauses in speech. The capacitors at the two outputs must be equal value (±10%) to prevent problems in timing and level response.

The components at the inputs of the level detectors (RLI, TLI) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors. They must be adjusted for proper switching response as described later in this section.

Switching and Response Time Measurements

Using burst of 1.0 kHz sine waves to force the circuit to switch among its modes, the timing results were measured and are indicated in Figures 17–21.

a) In Figure 17, when a signal is applied to the transmit attenuator only (normally via the microphone and the microphone amplifier), the transmit background noise monitor immediately indicates the "presence of speech" as evidenced by the fact that CPT begins rising. The slope of the rising CPT signal is determined by the external resistor and capacitor on that pin. Even though the transmit attenuator is initially in the idle mode (–16 dB), there is sufficient signal at its output to cause TLO to increase. The attenuator control circuit then forces the circuit to the transmit mode, evidenced by the change at the C_T pin. The attenuator output signal is then 6.7 dB above the input.

With the steady sine wave applied to the transmit input, the circuit will stay in the transmit mode until the CPT pin gets to within 36 mV of its final value. At that point, the internal comparator (see Figure 27) switches, indicating to the attenuator control circuit that the signal is not speech, but rather it is a steady background noise. The circuit now begins to decay to idle, as evidenced by the change at C_T and TLO, and the change in amplitude at TAO.

When the input signal at TAI is removed (or reduced), the CPT pin drops quickly, allowing the circuit to quickly respond to any new speech which may appear afterwards. The voltage at C_T decays according to the time constant of its external components, if not already at idle.

The voltage change at CP2, CPT, and TAO depends on the input signal's amplitude and the components at XDI and TLI. The change at C_T is internally fixed at the level shown. The timing numbers shown depend both on the signal amplitudes and the components at the C_T and CPT pins.

b) Figure 18 indicates what happens when the same signal is applied to the receive side only. RLO and CPR react similarly to TLO and CPT. However, the circuit does not switch to idle when CPR finishes transitioning since the dial tone detector disables the background noise monitor, allowing the circuit to stay in the receive mode as long as there is a signal present. If the input signal amplitude had been less than the dial tone detector's threshold, the circuit response would have been similar to that shown in Figure 17. The voltage change at C_T depends on the setting of the volume control (Pin 19). The 150 mV represent maximum volume setting.

c) Figure 19 indicates the circuit response when transmit and receive signals are alternately applied, with relatively short cycle times (300 ms each) so that neither attenuator will begin to go to idle during its "on" time. Figure 20 indicates the circuit response with longer cycle times (1.0 s each), where the transmit side is allowed to go to idle. Figure 21 is the same as Figure 20, except the capacitor at C_T has been reduced from 15 μF to 6.8 μF, providing a quicker switching time. The reactions at the various pins are shown. The response times at TAO and RAO are different, and typically slightly longer than what is shown in Figures 17 and 18 due to:

– the larger transition required at the C_T pin,

– the greater difference in the levels at RLO and TLO due to the positions of the attenuators as well as their decay time, and

– response time of the background noise monitors.

The timing responses shown in these three figures are representative for those input signal amplitudes and burst durations. Actual response time will vary for different signal conditions.

NOTE: While it may seem desirable to decrease the switching time between modes by reducing the capacitor at C_T, this should be done with caution for two reasons:

1) If the switching time is too short, the circuit response may appear to be "too quick" to the user, who may consider its operation erratic. The recommended values in this data sheet, along with the accompanying timings, provide what

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experience has shown to be a “comfortable response” by the circuit.

2) The distortion in the receive attenuator will increase as the C_T capacitor value is decreased. The extra THD will be most noticeable at the lower frequencies and at the lower ampitudes. Table 1 provides a guideline for this issue.

Table 1. THD versus C_T Capacitor

C_T Capacitor	Idle – R_X Transition	Input @ RAI	Freq.	THD @ RAO
15 µF	25 ms	20 mVrms	300 Hz	1.2%
			1.0 KHz	0.25%
		100 mVrms	300 Hz	0.5%
			1.0 KHz	0.2%
6.8 µF	12 ms	20 mVrms	300 Hz	5.0%
			1.0 KHz	0.7%
		100 mVrms	300 Hz	1.3%
			1.0 KHz	0.35%
3.0 µF	5.0 ms	20 mVrms	300 Hz	11%
			1.0 KHz	1.8%
		100 mVrms	300 Hz	2.6%
			1.0 KHz	0.7 %

Considerations in the Design of a Speakerphone

The design and adjustment of a speakerphone involves human interface issues as well as proper signal levels. Because of this fact, it is not practical to do all of the design mathematically. Certain parts of the design must be done by trial and error, most notably the switching response and the “How does it sound?” part of the testing. Among the recommendations for a successful design are:

1) Design the enclosure **concurrently** with the electronics. Do not leave the case design to the end as its properties are just as important (just as *equally* important) as the electronics. One of the major issues involved in a speakerphone design is the acoustic coupling of the speaker to the microphone, which must be minimized. This parameter is dependent entirely on the design of the enclosure, the mounting of the speaker and the microphone, and their characteristics.

2) Ensure the speaker is optimally mounted. This fact alone can make a difference of several dB in the sound level from the speaker, as well as the sound quality. The speaker manufacturer should be consulted for this information.

3) Do not breadboard the circuit with the microphone and speaker hanging out in midair. It will not work. The speaker and microphone must be in a suitable enclosure, preferably one resembling the end product. If this is not feasible, temporarily use some other properly designed enclosure, such as one of the many speakerphones on the market.

4) Do not breadboard the circuit on a wirewrapped board or a plug–in prototyping board. Use a PC board, preferably with a ground plane. Proper filtering of the supply voltage at the V_{CC} pin is essential.

5) The speakerphone must be tested with the intended hybrid and connected to a phone line or phone line simulator. The performance of the hybrid is just as important as the enclosure and the speakerphone IC.

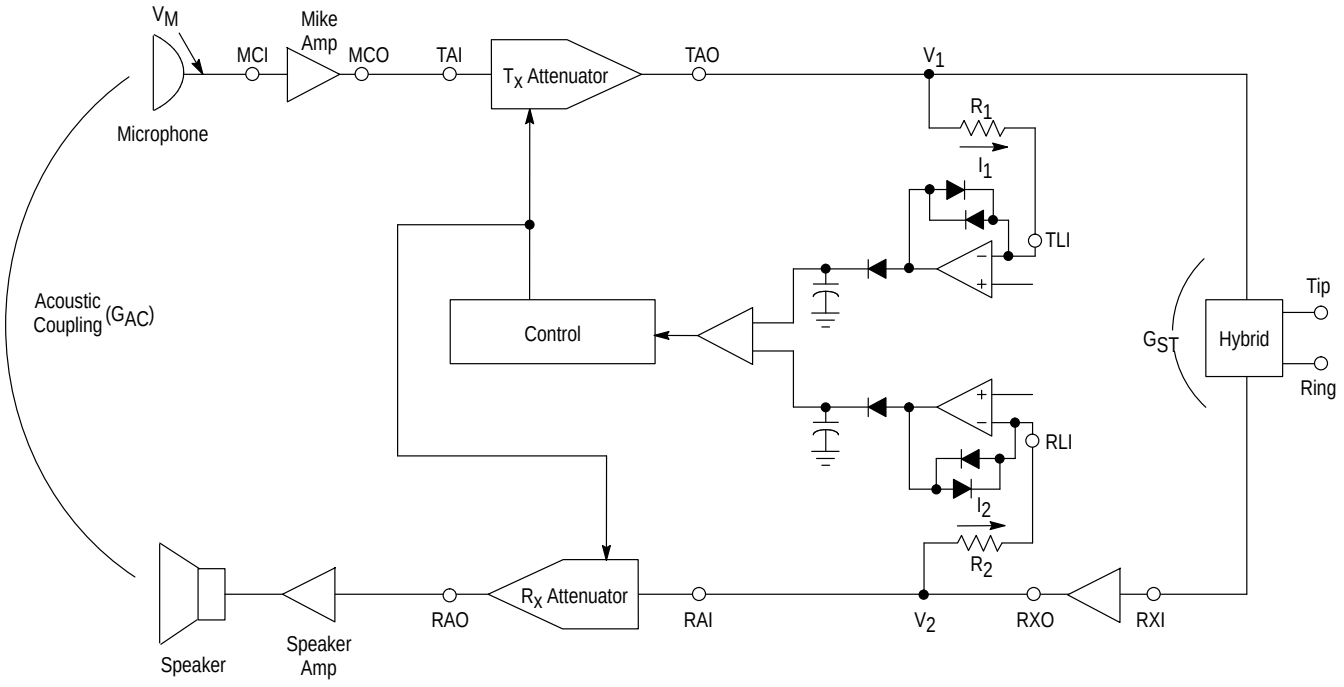
6) When testing the speakerphone, be conscious of the environment. If the speakerphone is in a room with large windows and tile floors, it will sound different than if it is in a carpeted room with drapes. Additionally, be conscious of the background noise in a room.

7) When testing the speakerphone on a phone line, make sure the person at the other end of the phone line is **not** in the same room as the speakerphone.

Design Procedure

A recommended sequence follows in Figure 31, assuming the end product enclosure is available, with the intended production microphone and speaker installed, and the PC boards or temporary substitutes installed.

Figure 31. Basic Block Diagram for Design Purposes



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1) Design the hybrid, ensuring proper interface with the phone line for both DC and AC characteristics. The return loss must be adjusted to comply with the appropriate regulatory agency. The sidetone should then be adjusted according to the intent of the product. If the product is a speakerphone only (without a handset), the sidetone gain (GST) should be adjusted for maximum loss. If a handset is part of the end product, the sidetone must be adjusted for the minimum acceptable sidetone levels in the handset. Generally, for the speakerphone interface, 10–20 dB sidetone loss is preferred for GST.

2) Check the acoustic coupling of the enclosure (GAC in Figure 31). With a steady sound coming out of the speaker, measure the rms voltage on the speaker terminals and the rms voltage out of the microphone. Experience has shown that the loss should be at least 40 dB, preferably 50 dB. This should be checked over the frequency range of 20 Hz to 10 kHz.

3) Adjust the transmit path for proper signal levels, based on the lowest speech levels as well as the loudest. Based on the typical levels from commonly available microphones, a gain of about 35–45 dB is required from the microphone terminals to Tip and Ring. Most of that gain should be in the microphone amplifier to make best use of the transmit attenuator, but the maximum input level at TAI must not be exceeded. If a signal generator is used instead of a microphone for testing, the circuit can be locked into the transmit mode by grounding CPT (Pin 3). Frequency response can generally be tailored with capacitors at the microphone amplifier.

4) Adjust the receive path for proper signal levels based on the lowest speech levels as well as the loudest. A gain of about 30 dB is required from Tip and Ring to the speaker terminals for most applications (at maximum volume). Most of that gain should be in the receive amplifier (at RXI, RXO) to make best use of the receive attenuator, but the maximum input level at RAI must not be exceeded. If a signal generator is used for signal injection during testing, the circuit can be locked into the receive mode by grounding CPR (Pin 10), although this is usually not necessary since the dial tone detector will keep the circuit in the receive mode. Frequency response can generally be tailored with capacitors at the receive amplifier.

5) Check that the loop gain (i.e., the receive path gain + acoustic coupling gain + transmit path gain + sidetone gain) is less than 0 dB over all frequencies. If not, “singing” will occur: a steady oscillation at some audible frequency.

6) a) The final step is to adjust the resistors at the level detector inputs (RLI and TLI) for proper switching response (the switchpoint occurs when $I_1 = I_2$). This has to be the last step, as the resistor values depend on all of the above adjustments, which are based on the mechanical, as well as the electrical, characteristics of the system. **NOTE:** An extreme case of level detector misadjustment can result in “motorboating”. In this condition, with a receive signal applied, sound from the speaker enters the microphone, and causes the circuit to switch to the transmit mode. This causes the speaker sound to stop (as well as the sound into the microphone), allowing the circuit to switch back to the receive mode. This sequence is then repeated, usually, at a rate of a few Hz. The first thing to check is the acoustic coupling, and then the level detectors.

b) Starting with the recommended values for R_1 and R_2 (in Figure 2), hold a normal conversation with someone on another phone. If the resistor values are not optimum, one of the talkers will dominate, and the other will have difficulty getting through. If, for example, the person at the speakerphone is dominant, the transmit path is overly sensitive, and the receive path is not sensitive enough. In this case, R_1 (at TLI) should be increased, or R_2 (at RLI) decreased, or both. Their exact value is not critical at this point, only their relative value. Keeping R_1 and R_2 in the range of 2.0–20 k, adjust them until a suitable switching response is found.

c) Then have the person at the other end of the phone line speak loud continuously, or connect to a recording which is somewhat strong. Monitor the state of the circuit (by measuring the C_T versus V_B pins, and by listening carefully to the speaker) to check that the sound out of the speaker is not attempting to switch the circuit to the transmit side (through acoustic coupling). If it is, increase R_1 (at TLI) in small steps just enough to stop the switching (this desensitizes the transmit side). If R_1 has been changed a large amount, it may be necessary to readjust R_2 for switching response. If this cannot be achieved in a reasonable manner, the acoustic coupling is too strong.

d) Next, have the person at the speakerphone speak somewhat loudly, and again monitor the state of the circuit, primarily by having the person at the other end listen carefully for fading. If there is obvious fading of the sound, increase R_2 so as to desensitize the receive side. Increase R_2 just enough to stop the fading. If this cannot be achieved in a reasonable manner, the sidetone coupling is too strong.

e) If necessary, readjust R_1 and R_2 a small amount relative to each other, to further optimize the switching response.

Transmit/Receive Detection Priority

Although the MC33219A was designed to have an idle mode such that the transmit side has a small priority (the idle mode position is closer to the full transmit side), the idle mode position can be moved with respect to the transmit or the receive side. With this done, the ability to gain control of the circuit by each talker will be changed.

By connecting a resistor from C_T (Pin 7) to ground, the circuit will be biased more towards the transmit side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_B}{\Delta V} - 1 \right]$$

where R is the added resistor, R_T is the resistor normally between Pins 6 and 7 (typically 15 kΩ), and ΔV is the desired change in the C_T voltage at idle.

By connecting a resistor from C_T (Pin 7) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_{CC} - V_B}{\Delta V} - 1 \right]$$

R, R_T, and ΔV are the same as above. Switching response and the switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 50 mV.

Disabling the Idle Mode

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the ON position, even with steady signals applied, by disabling the background noise monitors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the “presence

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of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

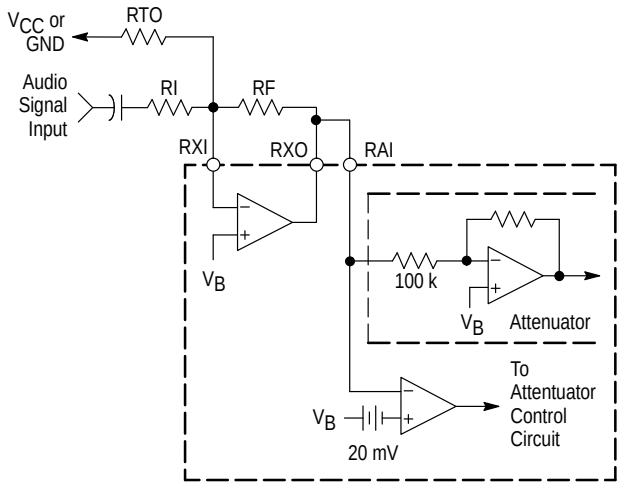
Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

Dial Tone Detector Threshold

The threshold for the dial tone detector is internally set at ≈ 20 mV (14 mVrms) below V_B (see Figure 29). That threshold can be adjusted if desired by changing the bias at RAI. The method used depends on how the input of the receive attenuator is connected to other circuitry.

a) If the attenuator input (RAI) is DC coupled to the receive amplifier (Pins 15 to 16 as in Figure 2), or to some other amplifier in the system, then the threshold is changed by forcing a small offset on that amplifier. As shown in Figure 32, connect a resistor (RTO) from the summing node to either ground or V_{CC}, depending on whether the dial tone detector threshold is to be increased or decreased. RF and RI are the resistors normally used to set the gain of that amplifier.

Figure 32. Adjusting Dial Tone Detector Threshold (DC Coupled)



Adding RTO and connecting it to ground will shift RXO and RAI upward, thereby increasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{V_B \times RF}{\Delta V}$$

V_B is the voltage at Pin 6, and ΔV is the amount that the detector's threshold is increased. For example, if V_B = 2.2 V, and RF = 10 k, and the threshold is to be increased by 20 mV, RTO calculates to 1.1 MΩ.

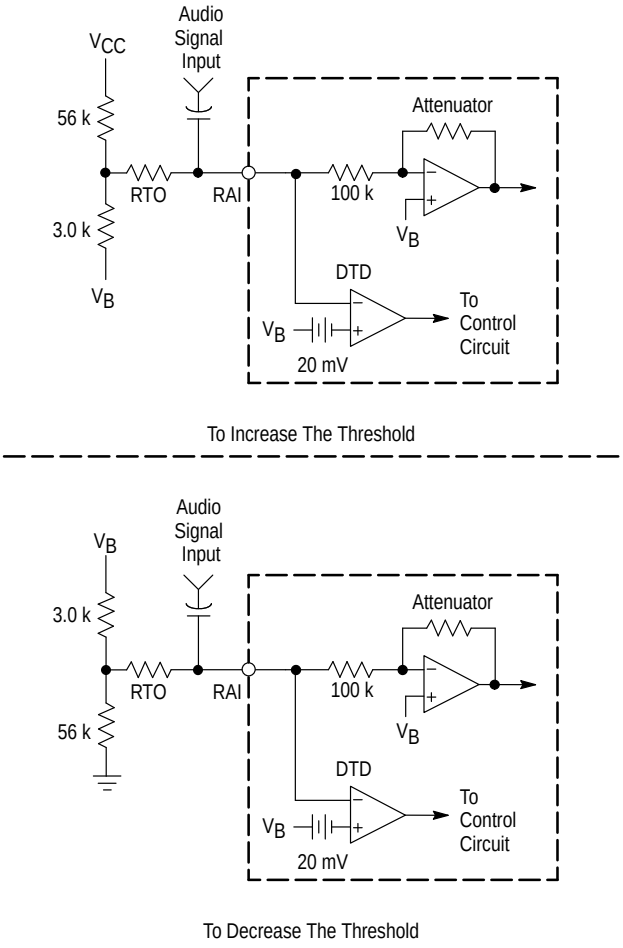
Connecting RTO to V_{CC} will shift RXO downward, thereby decreasing the dial tone detector threshold. In this case, RTO is calculated from:

$$RTO = \frac{(V_{CC} - V_B) \times RF}{\Delta V}$$

For example, if V_{CC} = 5.0 V, V_B = 2.2 V, and RF = 10 k and the threshold is to be decreased by 10 mV, RTO calculates to 2.8 MΩ.

b) If the receive attenuator input is AC coupled to the receive amplifier or to other circuitry, then the offset is set at RAI. The circuits in Figure 33 are suggested for changing the threshold.

Figure 33. Adjusting Dial Tone Detector Threshold (AC Coupled)



To increase the threshold, use the first circuit in Figure 33. The voltage at the top of the 3.0 k resistor is between 90 and 180 mV above V_B (depending on V_{CC}). RTO and the 100 k input impedance form a voltage divider to create the desired offset at RAI. RTO is calculated from:

$$RTO = \left[\frac{((V_{CC} - V_B) \times 0.05)}{\Delta V} - 1\right] (100\ k)$$

For example, if V_{CC} = 5.0 V, and the threshold is to be increased by 20 mV (ΔV), RTO calculates to ≈ 600 kΩ.

If the threshold is to be decreased, use the second circuit in Figure 33. RTO is calculated from:

$$RTO = \left[\frac{(V_B \times 0.05)}{\Delta V} - 1\right] (100\ k)$$

RFI Interference

Potential radio frequency interference (RFI) problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the microphone amplifier (which should be short), or through any of the PC board traces. The most sensitive pins on the MC33219A are the inputs to the level detectors (RLI, TLI, XDI) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open–loop condition. The board traces to these pins should be kept

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short, and the resistor and capacitor for each of these pins should be physically close to the pins. All other input pins should also be considered sensitive to RFI signals.

In The Final Analysis ...

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design in addition to proper electronic design.The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, low microphone quality, or any combination of these items. Proper acoustic separation of the speaker and microphone is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuit will have to be fine–tuned to match the acoustics of the enclosure, the specific hybrid, and the specific speaker and microphone selected. The components shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and receive amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs (TLI, RLI) until satisfactory operation is obtained for both long and short lines.

For additional information on speakerphone design please refer to The Bell System Technical Journal, Volume XXXIX (March 1960, No. 2).

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GLOSSARY

Attenuation – A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth – The range of information carrying frequencies of a communication system.

Battery – The voltage which provides the loop current to the telephone from the CO. The name is derived from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

C–Message Filter – A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office – Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A CO can handle up to 10,000 subscriber numbers.

CO – See Central Office.

CODEC – Coder/Decoder – In the Central Office, it converts the transmit signal to digital, and converts the digital receive signal to analog.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \times \log (P_1/P_2)$$

for power measurements, and

$$20 \times \log(V_1/V_2)$$

for voltage measurements.

dBm – An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp – Indicates dBm measurement using a psophometric weighting filter.

dBrn – Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC – Indicates a dBrn measurement using a C–message weighting filter.

DTMF – Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

Four Wire Circuit – The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path, and one pair is for the Receive path.

Full Duplex – A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

Gain – The change in signal amplitude (increase or decrease) after passing through an amplifier or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

Half Duplex – A transmission system which permits communication in one direction at a time. CB radios, with "push–to–talk" switches, and voice activated speakerphones are half duplex.

Hookswitch – A switch within the telephone which connects the telephone circuit to the subscriber loop. The name is derived from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Hybrid – A two–to–four wire converter.

Idle Channel Noise – Residual background noise when transmit and receive signals are absent.

Line Card – The printed circuit board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber or a number of subscribers.

Longitudinal Balance – The ability of the telephone circuit to reject longitudinal signals on Tip and Ring.

Longitudinal Signals – Common mode signals.

Loop – The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or AC power.

Loop Current – The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20–120 mA.

Mute – Reducing the level of an audio signal, generally so that it is inaudible. Partial muting is used in some applications.

OFF Hook – The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON Hook – The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an ON hook phone as available for ringing.

PABX – Private Automatic Branch Exchange. In effect, a miniature central office; it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Power Supply Rejection Ratio – The ability of a circuit to reject outputting noise or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Protection, Primary – Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient on the phone line by clamping the voltages to less than ±1500 V.

Protection, Secondary – Usually located within the telephone, it protects the phone circuit from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

Pulse Dialing – A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones and many new pushbutton phones use pulse dialing.

Receive Path – Within the telephone, it is the speech path from the phone line (Tip and Ring) towards the receiver or speaker.

REN – Ringer Equivalence Number. An indication of the impedance (or loading factor) of a telephone bell or ringer circuit. An REN of 1.0 equals ≈ 8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

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Return Loss – Expressed in dB, it is a measure of how well the telephone's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \times \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

Ring – One of the two wires connecting the central office to a telephone. The name is derived from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone Rejection – The rejection (in dB) of the reflected signal in the receive path resulting from a transmit signal applied to the phone and phone line.

SLIC – Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

Subscriber – The customer at the telephone end of the line.

Subscriber Line – The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip – One of the two wires connecting the central office to a telephone. The name is derived from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Transmit Path – Within the telephone it is the speech path from the microphone towards the phone line (Tip and Ring).

Two Wire Circuit – Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Two–to–Four Wire Converter – A circuit which has four wires (on one side): two (signal and ground) for the outgoing signal and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side, and incoming differential signals received on the two wire side are directed to the receive path of the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

Voiceband – That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

Suggested Vendors

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
1–800–76–PRIMO

Telecom Transformers

Microtran Co., Inc.
Valley Stream, NY 11528
516–561–6050
Various models – ask for catalog
and Application Bulletin F232

PREM Magnetics, Inc.
McHenry, IL 60050
815–385–2700
Various models – ask for catalog

Stancor Products
Logansport, IN 46947
219–722–2244
Various models – ask for catalog

Motorola does not endorse or warrant the suppliers referenced.

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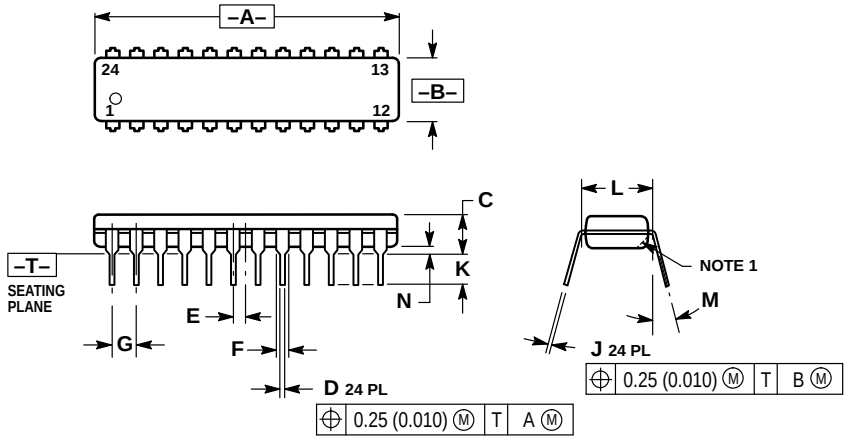
OUTLINE DIMENSIONS

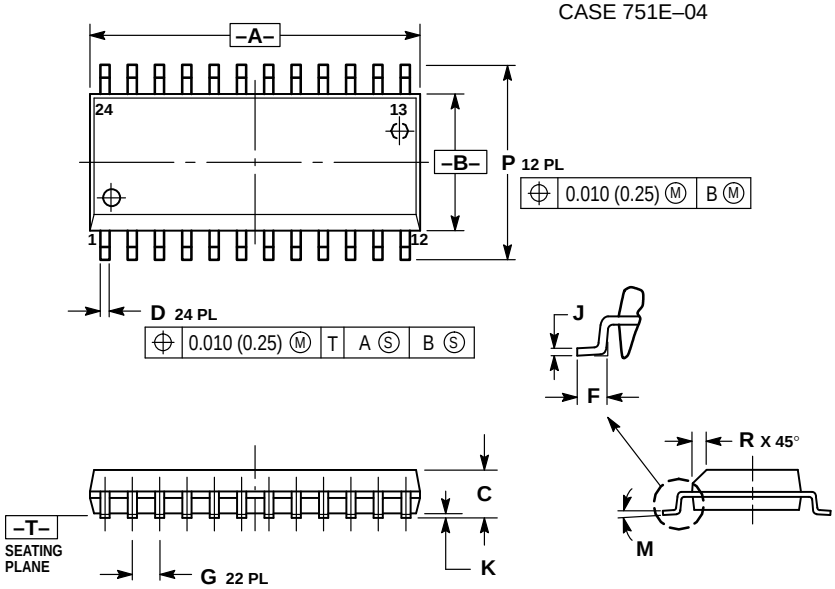
P SUFFIX
PLASTIC PACKAGE
CASE 724–03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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