Low Voltage 2.5/3.3V Differential ECL/PECL/HSTL Fanout Buffer

MC100ES6210

LOW VOLTAGE DUAL 1:5 DIFFERENTIAL PECL/ECL/HSTL CLOCK FANOUT BUFFER

FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A

The Motorola MC100ES6210 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6210 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low clock skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features:

- Dual 1:5 differential clock distribution
- 30 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3V, -3.3V, 2.5V or -2.5V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP210

Functional Description

The MC100ES6210 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz. The device consists of two independent 1:5 clock fanout buffers. The input signal of each fanout buffer is distributed to five identical, differential ECL/PECL outputs. Both CLKA and CLKB inputs can be driven by ECL/PECL compatible signals.

If VBB is connected to the CLKA or CLKB input and bypassed to GND by a 10 nF capacitor, the MC100ES6210 can be driven by single-ended ECL/PECL signals utilizing the VBB bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6210 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6210 supports positive (PECL) and negative (ECL) supplies. The is function and pin compatible to the MC100EP210.

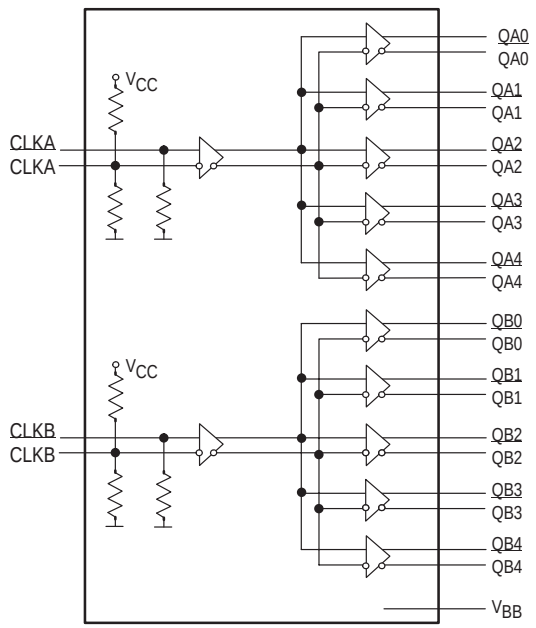


Figure 1.MC100ES6210 Logic Diagram

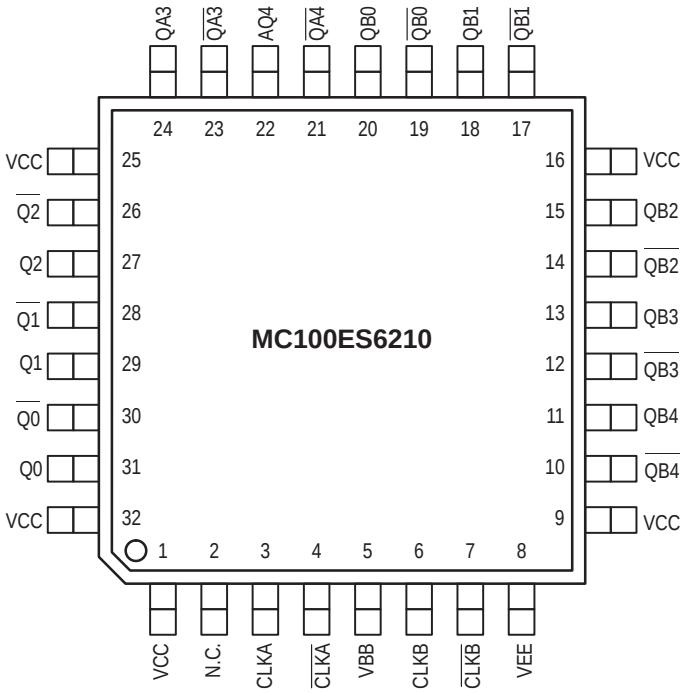


Figure 2.32–Lead Package Pinout (Top View)

Table 1. Pin configuration

Pin	I/O	Type	Function
CLKA, CLKA	Input	ECL/PECL	Differential reference clock signal input (fanout buffer A)
CLKB, CLKB	Input	ECL/PECL	Differential reference clock signal input (fanout buffer B)
QA[0-4], QA[0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer A)
QB[0-4], QB[0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer B)
VEE[a]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation

a. In ECL mode (negative power supply mode), VEE is either -3.3V or -2.5V and VCC is connected to GND (0V).
In PECL mode (positive power supply mode), VEE is connected to GND (0V) and VCC is either +3.3V or +2.5V .
In both modes, the input and output levels are referenced to the most positive supply (VCC).

Table 2. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} - 2[a]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model				V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient JESD 51-3, single layer tes board		 83.1 73.3 68.9 63.8 57.4	 86.0 75.4 70.9 65.3 59.6	 °C/W °C/W °C/W °C/W °C/W	 Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0 54.4 52.5 50.4 47.8	60.6 55.7 53.8 51.5 48.8	°C/W °C/W °C/W °C/W °C/W	Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating junction temperature[b] (continuous operation) MTBF = 9.1 years			110	°C	

a. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase
b. Operating junction temperature impacts device life time. Maximum continues operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6210 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6210 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics (V_{CC} = 2.5V ± 5% or V_{CC} = 3.3V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (PECL differential signals)							
V_{PP}	Differential input voltage[a]		0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[b]		1.0		V_{CC} - 0.3	V	Differential operation
I_{IN}	Input Current[a]				±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA0-4, $\overline{QA0-4}$, QB0-4, $\overline{QB0-4}$)							
V_{OH}	Output High Voltage		V_{CC}-1.2	V_{CC}-1.005	V_{CC}-0.7	V	I_{OH} = –30 mA[c]
V_{OL}	Output Low Voltage	V_{CC} = 3.3V±5% V_{CC} = 2.5V±5%	V_{CC}-1.9 V_{CC}-1.9	V_{CC}-1.705 V_{CC}-1.705	V_{CC}-1.5 V_{CC}-1.3	V	I_{OL} = –5 mA[c]
Supply current and V_{BB}							
I_{EE}	Maximum Quiescent Supply Current without output termination current			60	100	mA	V_{EE} pin
V_{BB}	Output reference voltage		V_{CC}-1.38	V_{CC}-1.26	V_{CC}-1.14	V	I_{BB} = 0.2 mA

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality
b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
c. Equivalent to a termination of 50Ω to V_{TT}.

Table 5. ECL DC Characteristics (V_{EE} = -2.5V ± 5% or V_{EE} = -3.3V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{CLKA}$, CLKB, $\overline{CLKB}$ (ECL differential signals)							
V_{PP}	Differential input voltage[a]		0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[b]		V_{EE} + 1.0		-0.3	V	Differential operation
I_{IN}	Input Current[a]				±100	µA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA0-4, $\overline{QA0-4}$, QB0-4, $\overline{QB0-4}$)							
V_{OH}	Output High Voltage		–1.2	-1.005	–0.7	V	I_{OH} = –30 mA[c]
V_{OL}	Output Low Voltage	V_{CC} = 3.3V±5% V_{CC} = 2.5V±5%	–1.9 –1.9	-1.705 -1.705	–1.5 –1.3	V	I_{OL} = –5 mA[c]
Supply current and V_{BB}							
I_{EE}	Maximum Quiescent Supply Current without output termination current			60	100	mA	V_{EE} pin
V_{BB}	Output reference voltage		-1.38	-1.26	-1.14	V	I_{BB} = 0.2 mA

a. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality
b. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
c. Equivalent to a termination of 50Ω to V_{TT}.

Table 6. AC Characteristics (ECL: V_{EE} = -3.3V ± 5% or V_{EE} = -2.5V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[a b]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL or ECL differential signals)						
V_{PP}	Differential input voltage[c] (peak-to-peak)	0.3	0.3	1.3	V	
V_{CMR}	Differential input crosspoint voltage[d] PECL ECL	 1.2 V_{EE}+1.2		 V_{CC} - 0.3 -0.3V	 V V	
ECL clock outputs (Q0-9, $\overline{\text{Q0-9}}$)						
f_{CLK}	Input Frequency	0		3000	MHz	Differential
t_{PD}	Propagation Delay CLKA to QAx or CLKB to QBx	 175	 260	 350	 ps	 Differential
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) f_O < 1.1 GHz f_O < 2.5 GHz f_O < 3.0 GHz	 0.45 0.35 0.20	 0.70 0.55 0.35		 V V V	
$t_{sk(O)}$	Output-to-output skew (per bank)		13	30	ps	Differential
$t_{sk(PP)}$	Output-to-output skew (part-to-part)			175	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
$t_{SK(P)}$	Output pulse skew[e]			50	ps	
DC_Q	Output Duty Cycle f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz	49.5 45.0	50 50	50.5 55.0	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	30		250	ps	20% to 80%

a. AC characteristics are design targets and pending characterization.
b. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
c. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
d. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
e. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

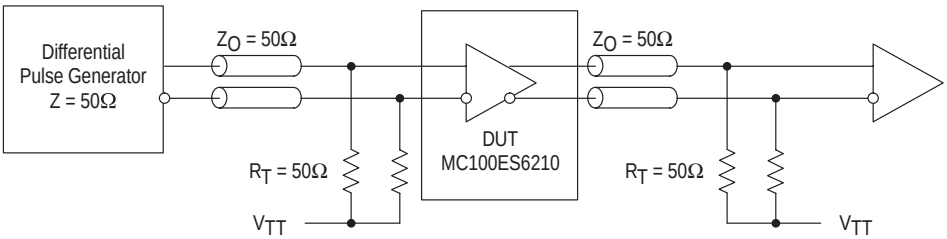
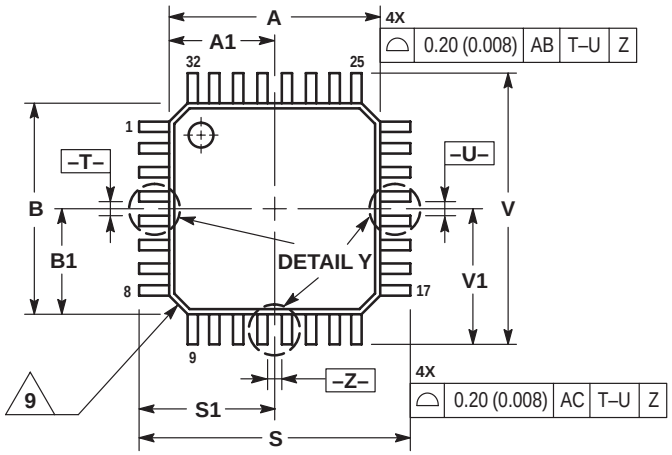


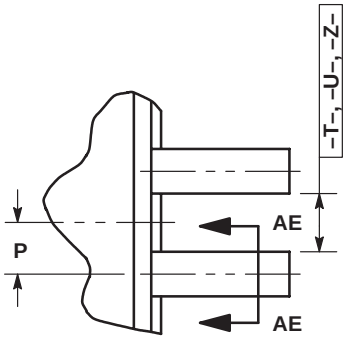
Figure 3.MC100ES6210 AC test reference

NOTES

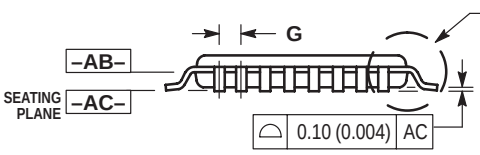
OUTLINE DIMENSIONS

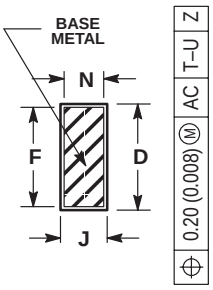
FA SUFFIX
LQFP PACKAGE
CASE 873A-02
ISSUE A



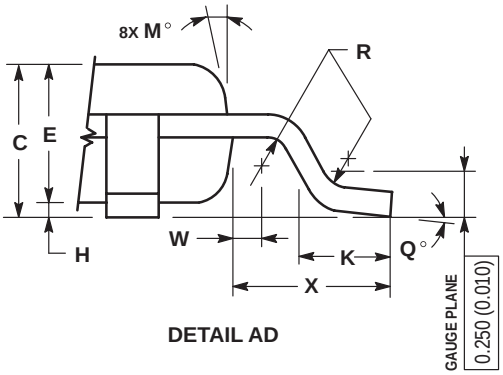


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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