MRF19030
MRF19030S

The RF MOSFET Line

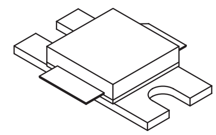
RF Power Field Effect Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

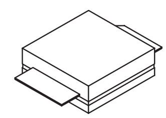
Designed for class AB PCN and PCS base station applications from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

- CDMA Performance @ 1990 MHz, 26 Volts
  IS–97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Thru 13
  885 kHz — –47 dBc @ 30 kHz BW
  1.25 MHz — –55 dBc @ 12.5 kHz BW
  2.25 MHz — –55 dBc @ 1 MHz BW
  Output Power — 4.5 Watts (Avg.)
  Power Gain — 13.5 dB
  Efficiency — 17%
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Ease of Design for Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 1.93 GHz, 30 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters

2.0 GHz, 30 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465E–02, STYLE 1
(MRF19030)



CASE 465F–01, STYLE 1
(MRF19030S)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	+15, –0.5	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	83.3 0.48	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Typical)
Machine Model	M3 (Typical)

THERMAL CHARACTERISTICS

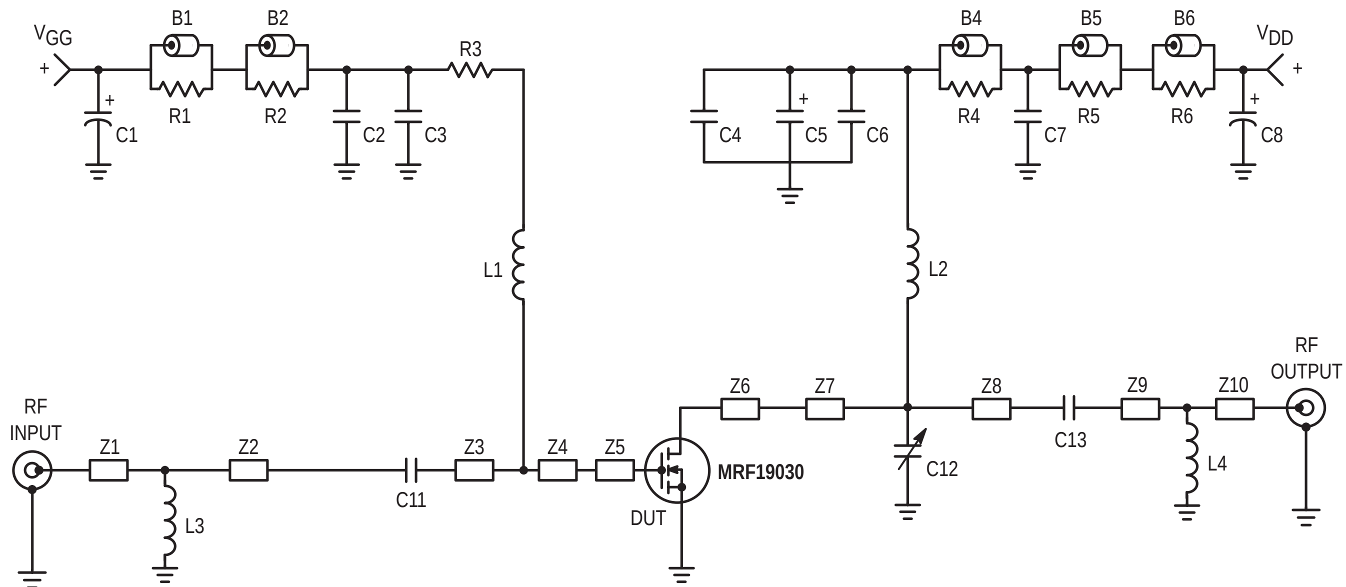
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.1	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 300 mA)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	2	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance (Including Input Matching Capacitor in Package) (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	98.5	—	pF
Output Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.3	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture)					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	G_{ps}	—	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	η	—	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IMD	—	–31	—	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1960.0 MHz, f2 = 1960.1 MHz)	IRL	—	–13	—	dB
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	G_{ps}	12	13	—	dB
Two–Tone Drain Efficiency (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	η	33	36	—	%
3rd Order Intermodulation Distortion (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	IMD	—	–31	–28	dBc
Input Return Loss (V_{DD} = 26 Vdc, P_{out} = 30 W PEP, I_{DQ} = 300 mA, f1 = 1930.0 MHz, f2 = 1930.1 MHz and f1 = 1990.0 MHz, f2 = 1990.1 MHz)	IRL	—	–13	–9	dB
Output Mismatch Stress (V_{DD} = 26 Vdc, P_{out} = 30 W CW, I_{DQ} = 300 mA, f = 1930 MHz, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.



B1 – B6	Ferrite Bead, Fair Rite #2743019447	Z1	0.595″ x 0.080″ Microstrip
C1, C8	470 µF, 63 V, Electrolytic Capacitor, Panasonic #ECEV1HV100R	Z2	0.600″ x 0.080″ Microstrip
C2, C7	0.10 µF, RF Chip Capacitor, B Case, Kemet	Z3	0.480″ x 0.080″ Microstrip
C3	5.1 pF, RF Chip Capacitor, B Case, ATC	Z4	0.280″ x 0.325″ Microstrip
C4	5.1 pF, RF Chip Capacitor, B Case, ATC	Z5	0.200″ x 0.510″ Microstrip
C5	22 µF, 35 V, Tantalum Surface Mount Chip Capacitor, Sprague	Z6	0.200″ x 0.510″ Microstrip
C6	91 pF, RF Chip Capacitor, B Case, ATC	Z7	0.280″ x 0.325″ Microstrip
C11, C13	10 pF, RF Chip Capacitor, B Case, ATC	Z8	0.480″ x 0.080″ Microstrip
C12	0.4 – 2.5 pF, Variable Capacitor, Johanson Gigatrim	Z9	0.530″ x 0.080″ Microstrip
L1 – L4	8.0 nH Inductors, 3 Turn, Coilcraft	Z10	0.720″ x 0.080″ Microstrip
R1, R2	12 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″	Board	0.030″ Glass Teflon® Arlon
R3	3.75 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″		GX–0300–55–22, 2 oz. Cu
R4 – R6	10 Ω, Fixed Film Chip Resistor, 0.08″ x 0.13″		

Figure 1. MRF19030 Schematic

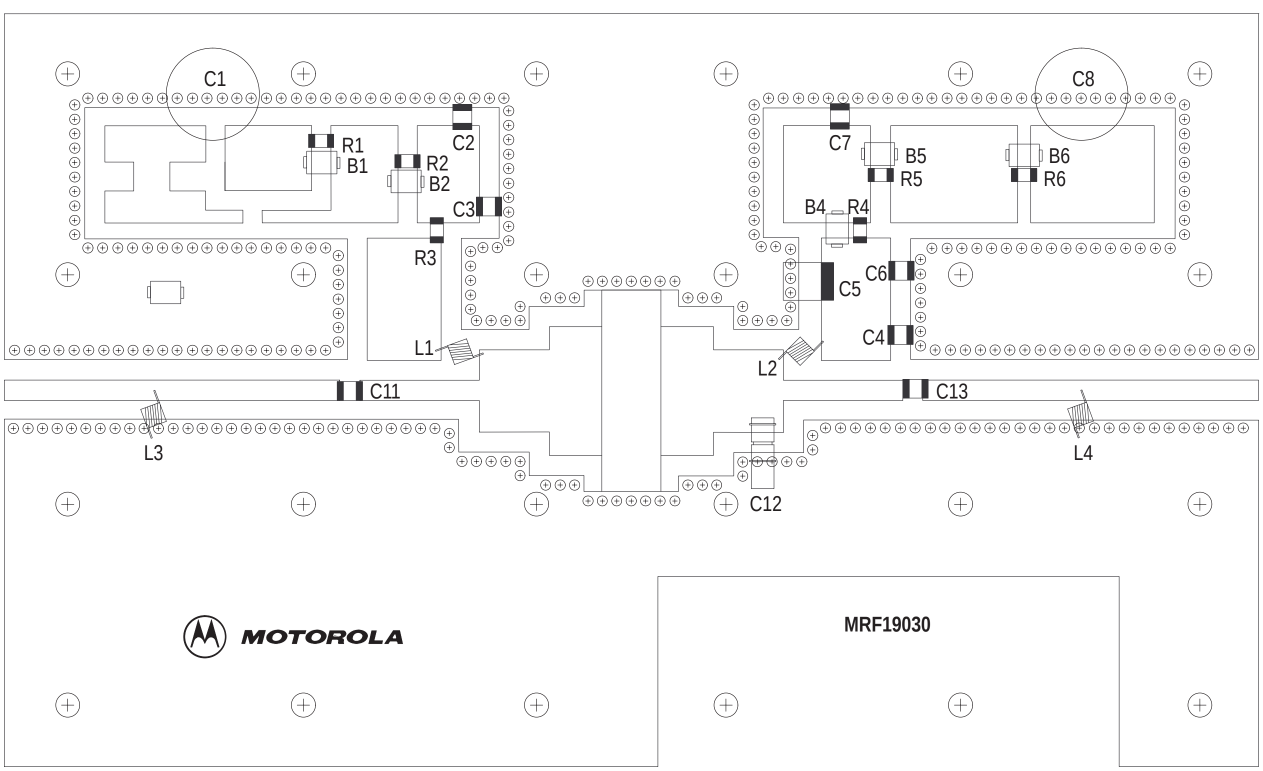


Figure 2. MRF19030 Populated PC Board Layout Diagram

TYPICAL CHARACTERISTICS

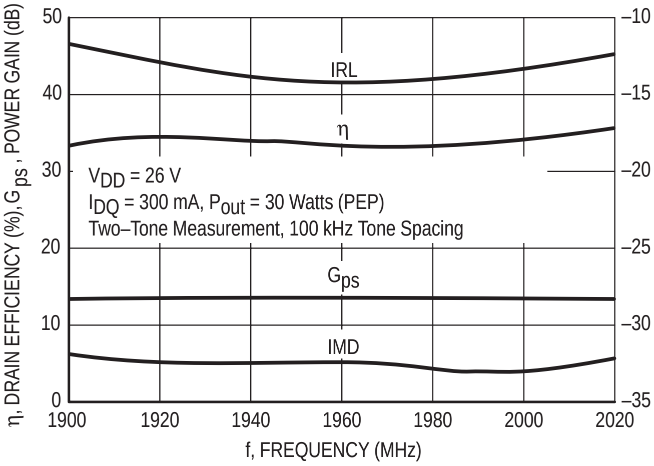


Figure 3. Class AB Broadband Circuit Performance

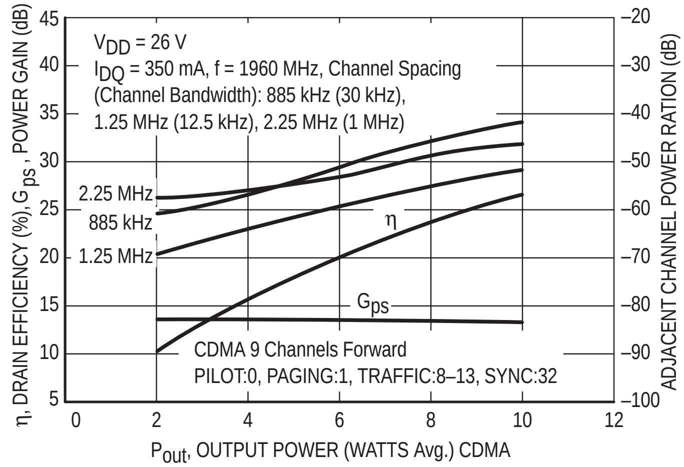


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

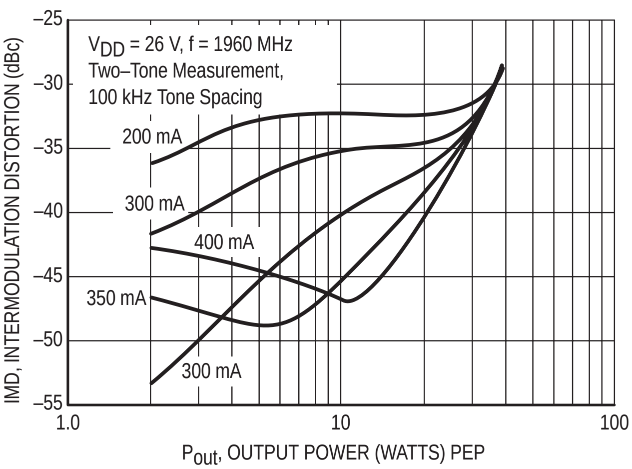


Figure 5. Intermodulation Distortion versus Output Power

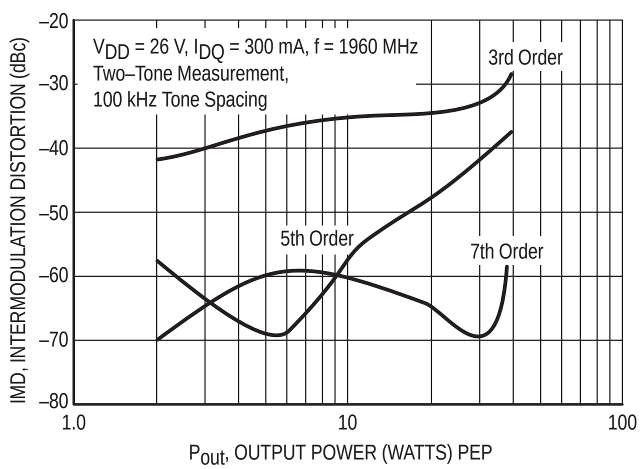


Figure 6. Intermodulation Distortion Products versus Output Power

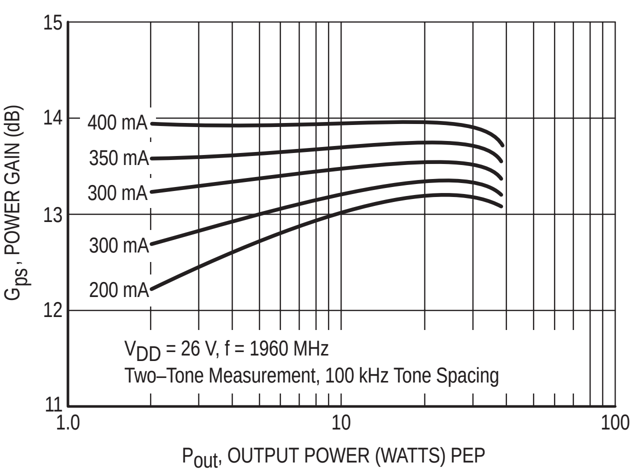


Figure 7. Power Gain versus Output Power

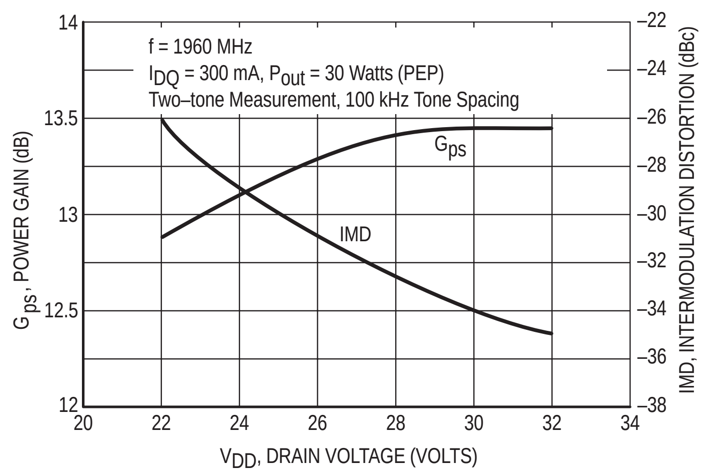
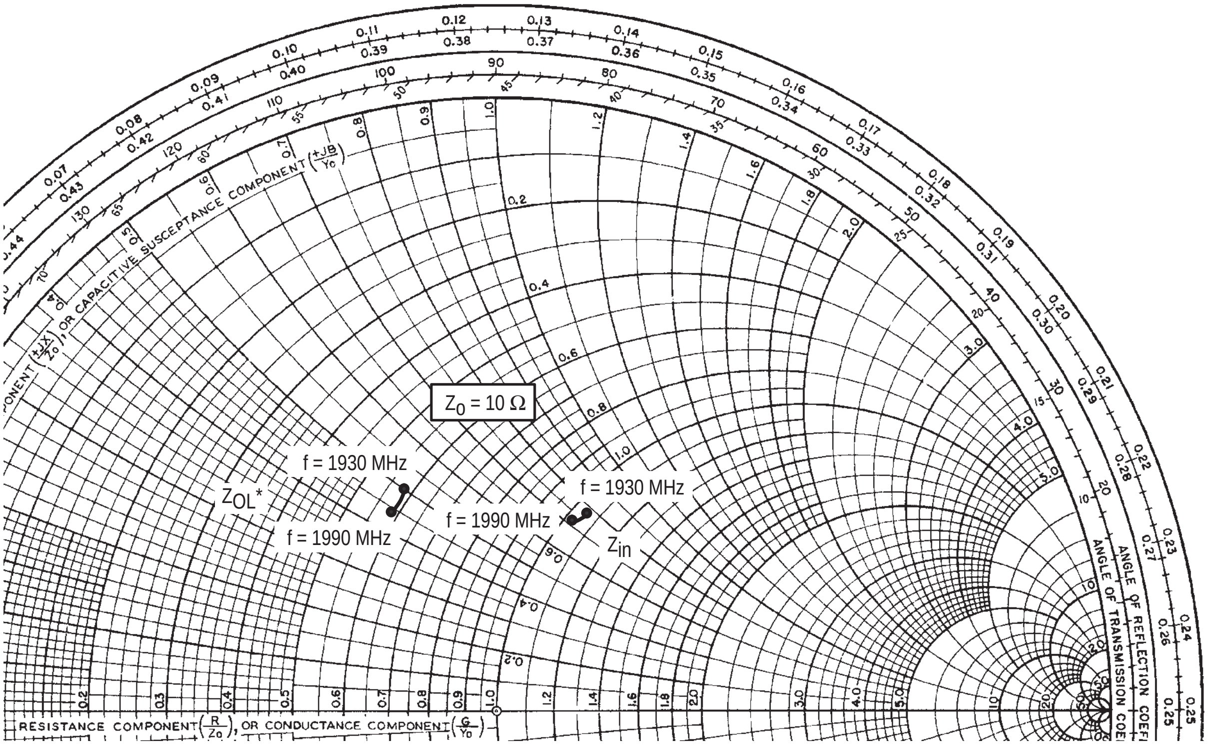


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



V_{DD} = 26 V, I_{DQ} = 300 mA, P_{out} = 30 Watts (PEP)

f MHz	Z_{in} Ω	Z_{OL}* Ω
1930	10.57 + j7.69	5.81 + j5.01
1960	10.54 + j7.43	5.84 + j4.67
1990	10.47 + j7.21	5.84 + j4.35

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

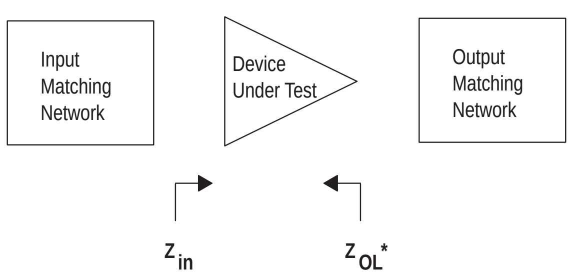
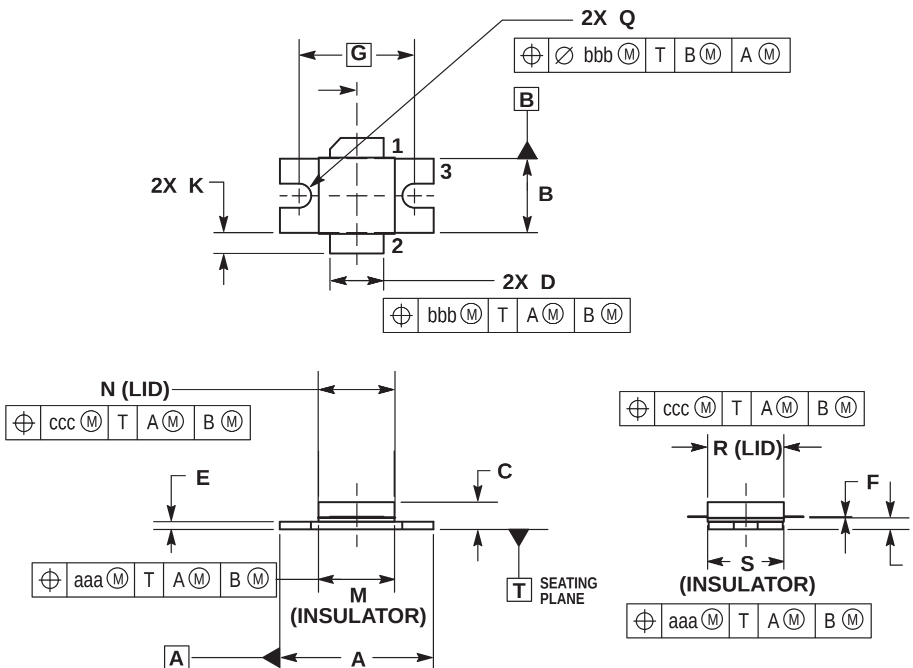


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS

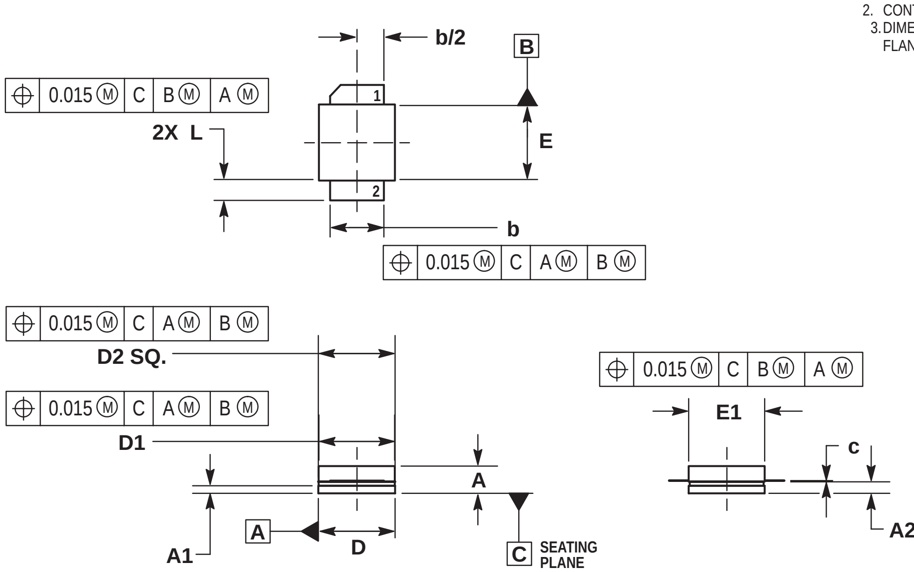


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 INCH AWAY FROM FLANGE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.160	3.17	4.06
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	.110	.130	2.79	3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–02
ISSUE C
(MRF19030)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A2 IS MEASURED 0.030" AWAY FROM FLANGE.

DIM	INCHES	
	MIN	MAX
A	0.125	0.160
A1	0.035	0.045
A2	0.057	0.067
b	0.275	0.285
c	0.003	0.006
D	0.395	0.405
D1	0.392	0.400
D2	0.395	0.405
E	0.395	0.405
E1	0.392	0.400
L	0.092	0.122

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–01
ISSUE O
(MRF19030S)

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