# 3.3 V Dual LVTTL/LVCMOS to Differential LVPECL Translator

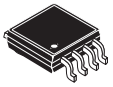
**MC100ES60T22**

The MC100ES60T22 is a low skew dual LVTTL/LVCMOS to differential LVPECL translator. The low voltage PECL levels, small package, and dual gate design are ideal for clock translation applications.

### Features

- 280 ps typical propagation delay
- 100 ps max output-to-output skew
- LVPECL operating range: $V_{CC}$ = 3.135 V to 3.8 V
- 8-lead SOIC and 8-lead TSSOP packages
- Ambient temperature range –40°C to +85°C

**D SUFFIX**
**8-LEAD SOIC PACKAGE**
**CASE 751-06**



**DT SUFFIX**
**8-LEAD TSSOP PACKAGE**
**CASE 1640-01**

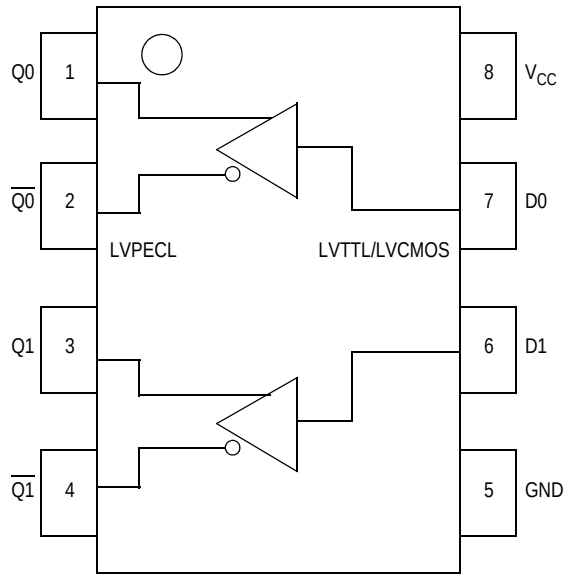



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

| ORDERING INFORMATION | |
|---|---|
| **Device** | **Package** |
| MC100ES60T22D | SOIC-8 |
| MC100ES60T22DR2 | SOIC-8 |
| MC100ES60T22DT | TSSOP-8 |
| MC100ES60T22DTR2 | TSSOP-8 |

| PIN DESCRIPTION | |
|---|---|
| **Pin** | **Function** |
| D0, D1 | LVTTL/LVCMOS Inputs |
| Qn, $\overline{Qn}$ | LVPECL Differential Outputs |
| $V_{CC}$ | Positive Supply |
| GND | Negative Supply |

**Table 1. General Specifications**

| Characteristics | | Value |
|---|---|---|
| Internal Input Pulldown Resistor | | 75 kΩ |
| Internal Input Pullup Resistor | | 75 kΩ |
| ESD Protection | Human Body Model<br>Machine Model | > 2000 V<br>> 200 V |
| $\theta_{JA}$ Thermal Resistance (Junction-to-Ambient) | 0 LFPM, 8 SOIC<br>500 LFPM, 8 SOIC<br>0 LFPM, 8 TSSOP<br>500 LFPM, 8 TSSOP | 190°C/W<br>130°C/W<br>185°C/W<br>140°C/W |

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

**Table 2. Absolute Maximum Ratings(1)**

| Symbol | Rating | Conditions | Rating | Units |
|---|---|---|---|---|
| $V_{SUPPLY}$ | Power Supply Voltage | Difference between $V_{CC}$ & $V_{EE}$ | 3.9 | V |
| $V_{IN}$ | Input Voltage | $V_{CC} - V_{EE} \leq 3.6$ V | $V_{CC}$ + 0.3<br>$V_{EE}$ – 0.3 | V<br>V |
| $I_{out}$ | Output Current | Continuous<br>Surge | 50<br>100 | mA<br>mA |
| $T_A$ | Operating Temperature Range | | –40 to +85 | °C |
| $T_{STG}$ | Storage Temperature Range | | –65 to +150 | °C |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 3. DC Characteristics** ($V_{CC}$ = 3.135 V to 3.8 V; $V_{EE}$ = 0 V)

| | | -40°C | | | 0°C to 85°C | | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Min | Typ | Max | Min | Typ | Max | Unit |
| $V_{OH}$(1) | Output HIGH Voltage | $V_{CC}$ – 1150 | $V_{CC}$ – 1020 | $V_{CC}$ – 800 | $V_{CC}$ – 1200 | $V_{CC}$ – 970 | $V_{CC}$ – 750 | mV |
| $V_{OL}$(1) | Output LOW Voltage | $V_{CC}$ – 1950 | $V_{CC}$ – 1620 | $V_{CC}$ – 1250 | $V_{CC}$ – 2000 | $V_{CC}$ – 1680 | $V_{CC}$ – 1300 | mV |

1. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ – 2 volts.

**Table 4. LVTTL / LVCMOS Input DC Characteristics** ($V_{CC}$ = 3.135 V to 3.8 V)

| | | | -40°C | | | 0°C to 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristic | Condition | Min | Typ | Max | Min | Typ | Max | Unit |
| $I_{IN}$ | Input Current | $V_{IN} = V_{CC}$ | | | ±150 | | | ±150 | μA |
| $V_{IK}$ | Input Clamp Voltage | $I_{IN}$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$+0.3 | 2.0 | | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | | | 0.8 | V |

**Table 5. AC Characteristics** ($V_{CC}$ = 3.134 V to 3.8 V; $V_{EE}$ = 0 V)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
| $f_{max}$ | Maximum Toggle Frequency | | | 1 | | | 1 | | | 1 | GHz |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | 100 | 260 | 400 | 100 | 280 | 400 | 100 | 280 | 450 | ps |
| $t_{SKEW}$ | Skew part-to-part | | | 300 | | | 300 | | | 350 | ps |
| $t_{JITTER}$ | Cycle-to-Cycle Jitter RMS (1σ) | | | 1 | | | 1 | | | 1 | ps |
| $V_{outPP}$ | Output Peak-to-Peak Voltage | 350 | 750 | | 350 | 750 | | 350 | 750 | | mV |
| $t_r$ / $t_f$ | Output Rise/Fall Times (20% – 80%) | 50 | | 400 | 50 | | 400 | 50 | | 400 | ps |

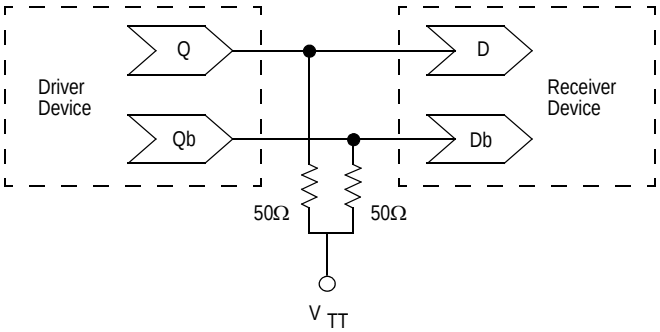
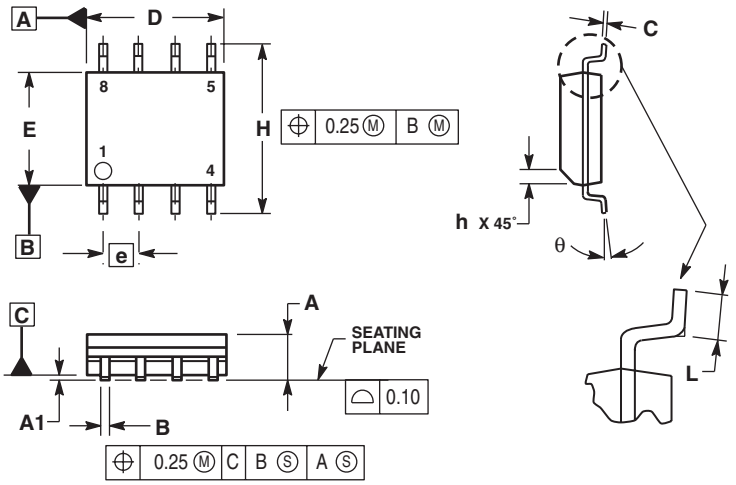



**Figure 2. Typical Termination for Output Driver and Device Evaluation**

## PACKAGE DIMENSIONS

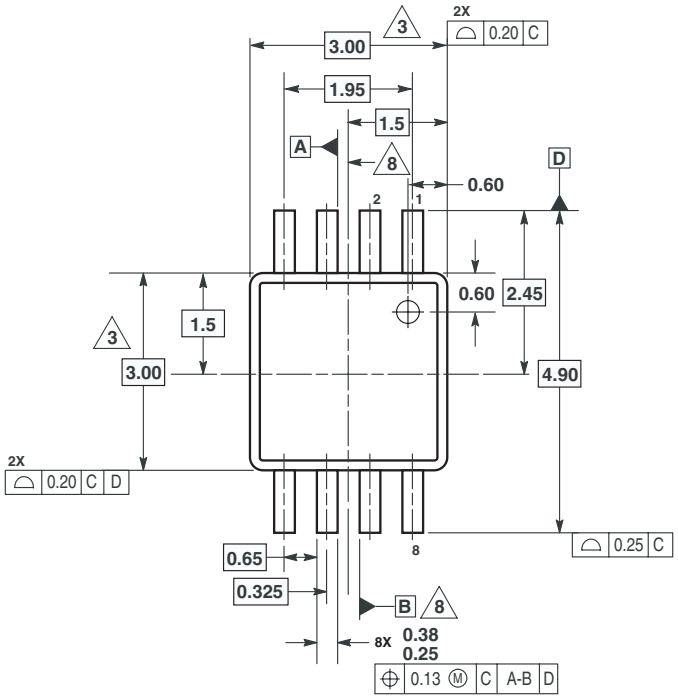



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

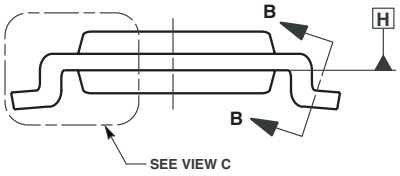
| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

**SOIC-8**
**D SUFFIX**
**8-LEAD SOIC PACKAGE**
**CASE 751-06**
**ISSUE T**

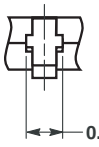
## PACKAGE DIMENSIONS



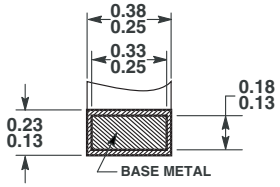

TOP VIEW



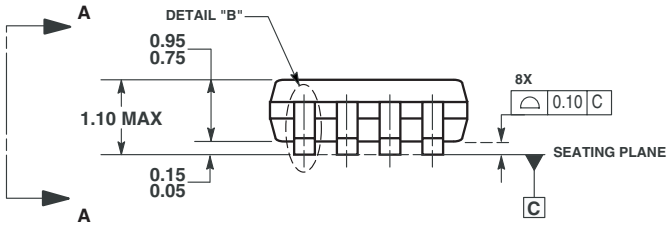

VIEW A-A



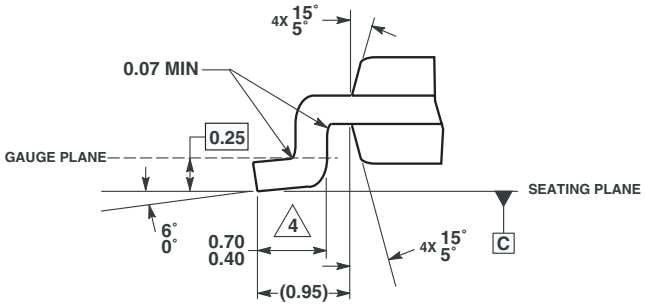

DETAIL "B"
DAMBAR PROTRUSION




SECTION B-B
SEE NOTE 6




SIDE VIEW




VIEW C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT DATUM H, MOLD FLASH OR PROTRUSIONS, SHALL NOT EXCEED 0.15mm PER SIDE.
4. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.14mm SEE DETAIL "B" AND SECTION B-B.
6. SECTION B-B TO BE DETERMINED AT 0.10 TO 0.25mm FROM THE LEAD TIP.
7. THIS PART IS COMPLIANT WITH JEDEC REGISTRATION MO-187 AA.
8. DATUMS A AND B TO BE DETERMINED DATUM PLANE H.

**TSSOP-8**
**DT SUFFIX**
**8-LEAD TSSOP PACKAGE**
**CASE 1640-01**
**ISSUE O**

# NOTES

# NOTES

# NOTES


### *How to Reach Us:*

**Home Page:**
www.freescale.com

**E-mail:**
support@freescale.com

**USA/Europe or Locations Not Listed:**
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

**Europe, Middle East, and Africa:**
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

**Japan:**
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

**Asia/Pacific:**
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only:***
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com






MC100ES60T22
Rev. 2
2/2005