HA12167FB/HA12169FB

Audio Signal Processor for Cassette Deck (Deck 1 Chip)

HITACHI

ADE-207-110B (Z)

3rd. Edition
June 1997

Description

HA12167FB/HA12169FB is silicon monolithic bipolar IC providing REC volume system, Level meter system and Dolby noise reduction system in one chip.

Functions

- REC equalizer × 2 channel
- Equalizer volume × 2 channel
- Dolby B/C NR × 2 channel
- REC/PB input electronic volume × 2 channel
- Level Meter × 2 channel
- DAC for adjusting bias × 2 channel

Features

- Available to create characteristics of REC equalizer by changing external resistor, no coil
- Equalizer volume is available to calibrate recording automatically with micro-controller
- Electronic volume built-in is available to set the level of recording and play back automatically with micro-controller
- 4 types of input (3 out of 4 are by way of electronic volume)
- Input electronic control switching is irrelevant to REC/PB electronic control switching
- Dolby noise reduction system is available with double cassette decks (Unprocessed signal output available from recording out terminals during PB mode)
- Log-compressed level meter output is range from 0 V to 5 V (Usable as music search switchable gain of 0 dB and 20 dB respectively)
- Normal-speed/high-speed, normal/metal/chrome fully electronic control switching built-in
- NR-ON/OFF, Dolby B/C, MPX ON/OFF fully electronic control switching built-in
- Reduction of the number of pins by transfered serial data to electronic volume control switching and another control switching (Controllable from micro-controller directly)
- Small the number of external parts

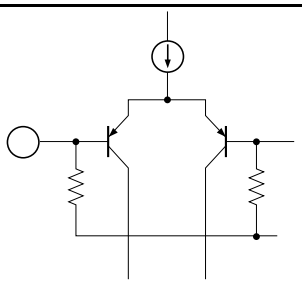
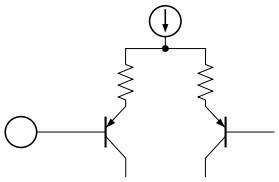
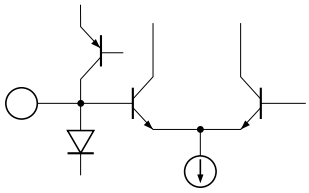
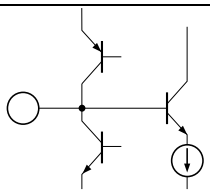
Hitachi semiconductor

Ordering Information

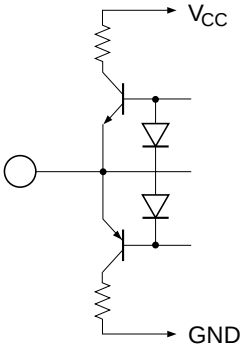
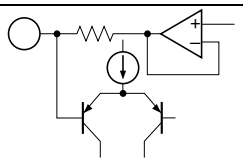
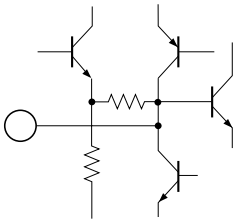
Type	Package	PB-OUT Level	REC-OUT Level	Dolby Level	Operating Voltage	
					Min	Max
HA12167FB	QFP-80	775 mVrms	300 mVrms	300 mVrms	12.0 V	15.0 V
HA12169FB	(14 × 14)	580 mVrms			11.0 V	15.0 V

* Dolby is a trademark of Dolby Laboratories Licensing Corporation.
A license from Dolby Laboratories Licensing Corporation is required for the use of this IC.

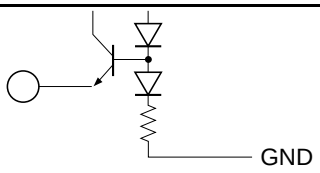
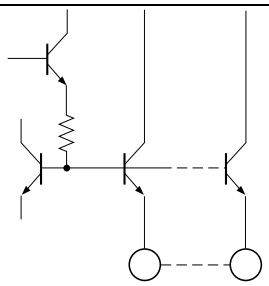
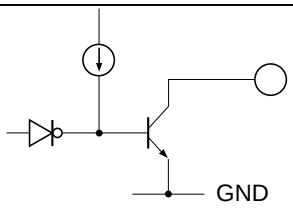
Pin Description (V_{CC} = 14 V, Ta = 25°C, No signal, The value in the show typical value.)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
65	RPI	100 kΩ	V_{cc}/2		Recording input
76					
9	LM IN	100 kΩ			Level meter input
52					
12	EQ IN	100 kΩ			Equalizer input
49					
66, 67, 69	VRI	100 kΩ	V_{cc}/2 + 0.7 V		Volume input
72, 74, 75					
30, 31	VCC	—	V_{cc}	—	Power supply
77	REF	—	V_{cc}/2	—	Ripple filter
62	NR IN	—	V_{cc}/2		NR processor input
79					
3	SS 1	—	V_{cc}/2		Spectral skewing amp input
58					
5	CCR	—	V_{cc}/2		Current controlled resistor output
56					

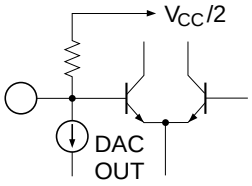
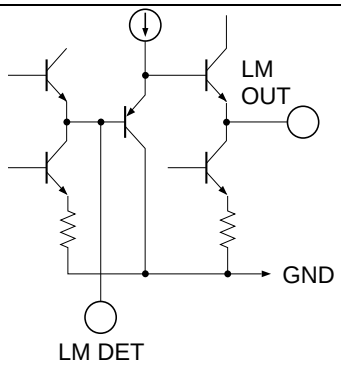
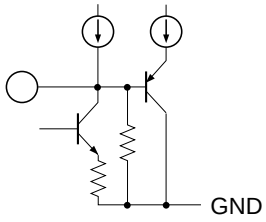
Pin Description (V_{CC} = 14 V, Ta = 25°C, No signal, The value in the show typical value.) (Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
63	IA OUT	—	$V_{cc}/2$		Input amp output
78					
61	VREF				Reference voltage
80					buffer output
2	PB OUT				Play back
59					(Decode) output
4	SS 2				Spectal skewing
57					amp. output
8	REC OUT				Recording
53					(Encode) output
15	EQ OUT				Equalizer output
46					
1	TP	1.5 kΩ	$V_{cc}/2$		Bias trap terminal
60					
6	HLS DET	—	2.3 V		Time constant pin for rectifier
55					
7	LLS DET				
54					

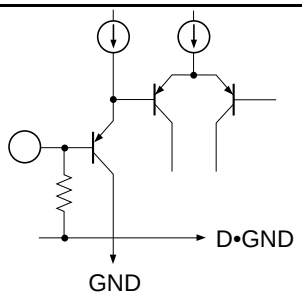
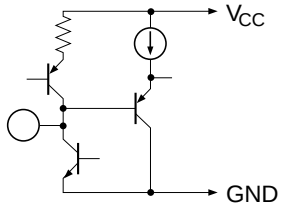
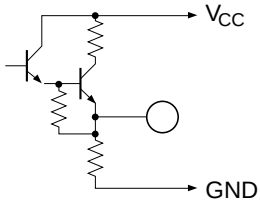
Pin Description (V_{CC} = 14 V, Ta = 25°C, No signal, The value in the show typical value.) (Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
64	BIAS	—	0.28 V		Dolby NR reference current input
14	IREF	—	1.2 V		EQ reference current input
27	MF				EQ parameter
26	fQ				current input
25	f/Q				
24	GH				
23	GL				
22	GP				
35	BIAS ADJ (N)	—	1.2 V		Bias DAC
36	BIAS ADJ (M)				parameter current
37	BIAS ADJ (C)				input
21	HM	—	—		EQ parameter selector
20	HC				
19	HN				
18	NM				
17	NC				
16	NN				

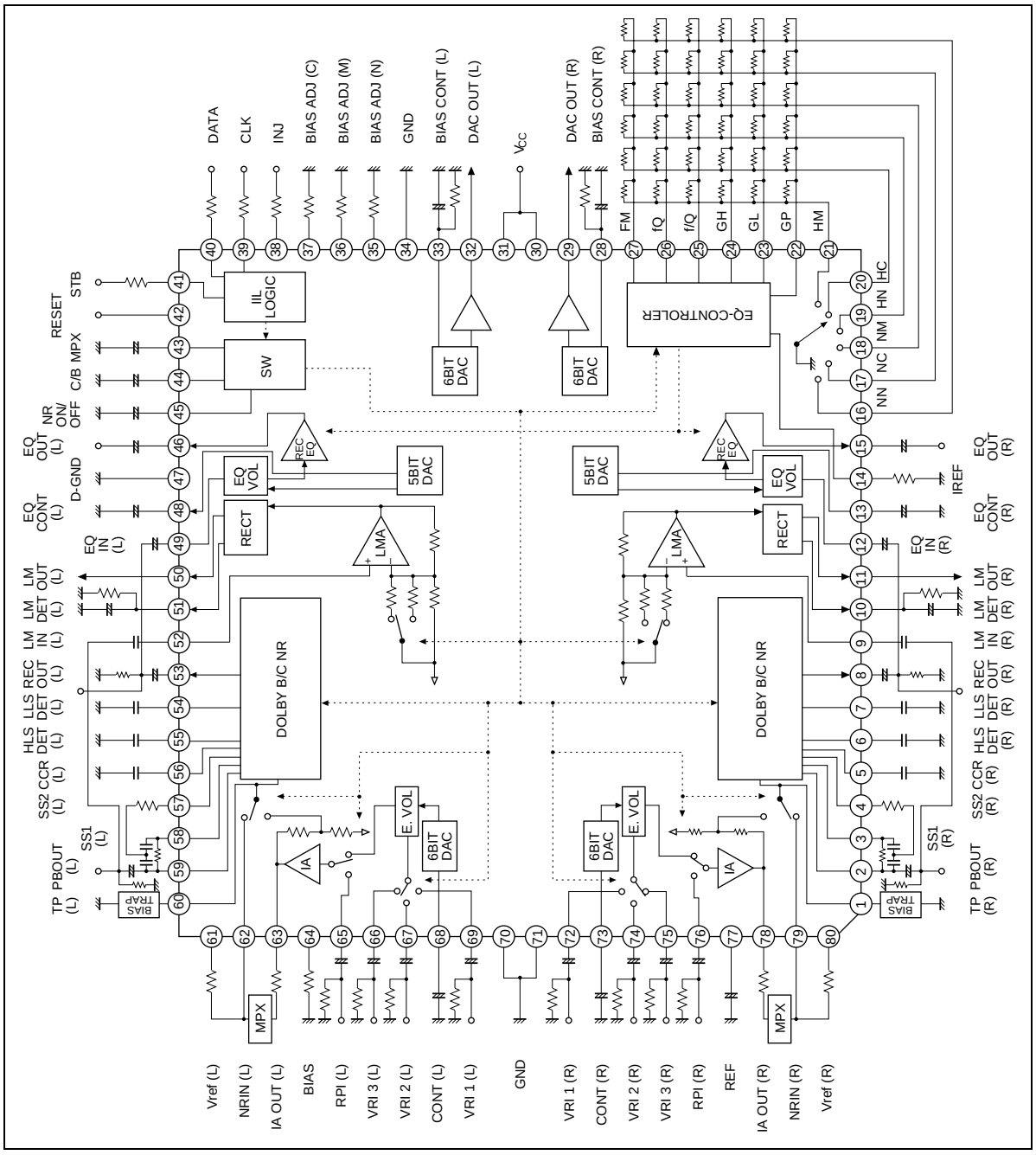
Pin Description (V_{CC} = 14 V, Ta = 25°C, No signal, The value in the show typical value.) (Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
68	CONT	3.3 kΩ	$V_{cc}/2$ – 1.5 V to $V_{cc}/2$		DAC output volume control input
73					
13	EQ CONT	1.65 kΩ			
48					
10	LM DET	—	0.2 V		Time constant pin for level meter
51					
11	LM OUT	—	0.2 V		Level meter output
50					
45	NR ON/OFF	100 kΩ	—		Mode control time constant
44	C/B				
43	MPX				

Pin Description (V_{CC} = 14 V, Ta = 25°C, No signal, The value in the show typical value.) (Cont)

Pin No. (QFP-80)	Terminal Name	Zin	DC Voltage	Equivalent Circuit	Description
42	RESET	100 kΩ	—		Mode control input
41	STB				
40	DATA				
39	CLK				
38	INJ	—	0.7 V	—	Injection current input I^2L
47	D-GND	—	0.0 V	—	Digital (Logic) ground
70	GND	—	0.0 V	—	Ground
71, 34					
28	BIAS CONT	—	—		Bias DAC output
33					
29	DAC OUT	—	—		Bias DAC buffer out
32					

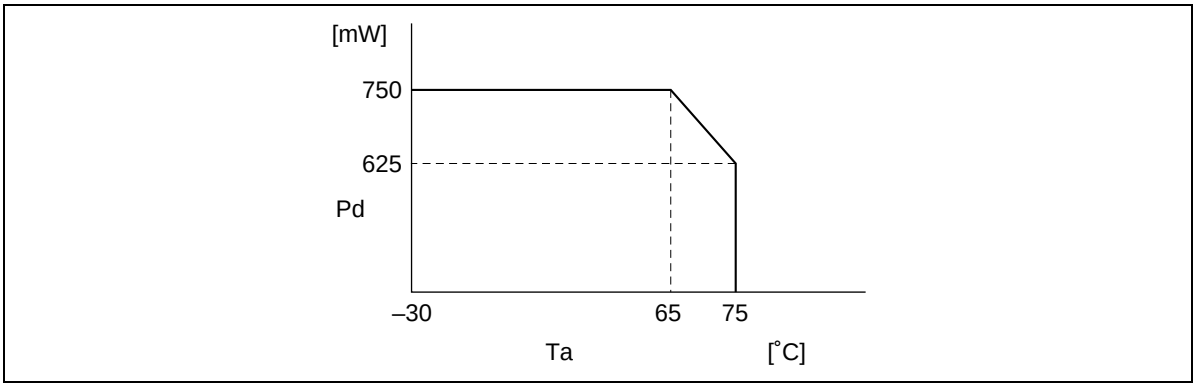
Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note
Supply voltage	V_{CC} max	15	V	
Power dissipation	Pd	750	mW	1
Operating temperature	Topr	–30 to +75	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: For Ta is higher than 65°C, reduce Pd at the rate of 12.5 mW/°C.
Please, see the below graph.



Electrical Characteristics (Ta = 25°C, V_{CC} = 14 V, Dolby Level 300 mVrms at RECOUT)

		Specification				Test Conditions															Application Terminal					
																					Input		Output			
Item	Symbol	Min	Typ	Max	Unit	REC /PB	RV /PV	MPX	NR	B/C	Input Pin	Meter	Tape Speed	Tape	Input DAC	EQ DAC	Bias DAC	fin [Hz]	REC OUT Level		R	L	R	L		Note
Quiescent current	IQ	—	34.5	42.0	mA	PB	PV	OFF	OFF	B	VRI1	NOR	NOR	NOR	32	0	0	—	—	No signal	—	—	—	—	30 31	
Input amp. gain	G_VIA RPI	18.5	20.0	21.5	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	0		76	65	78	63		
B-type encode boost	B-ENC -2 k	2.8	4.3	5.8	dB	REC	RV	ON	OFF → ON	B	RPI	NOR	NOR	NOR	63	0	0	2 k	–20		76	65	8	53		
	B-ENC -5 k	1.7	3.2	4.7		REC	RV	ON	OFF → ON	B	RPI	NOR	NOR	NOR	63	0	0	5 k	–20		76	65	8	53		
C-typ encode boost	C-ENC -1 k (1)	3.9	5.9	7.9	dB	REC	RV	ON	OFF → ON	C	RPI	NOR	NOR	NOR	63	0	0	1 k	–20		76	65	8	53		
	C-ENC -1 k (2)	18.1	19.6	21.6		REC	RV	ON	OFF → ON	C	RPI	NOR	NOR	NOR	63	0	0	1 k	–60		76	65	8	53		
	C-ENC -700	9.8	11.8	13.8		REC	RV	ON	OFF → ON	C	RPI	NOR	NOR	NOR	63	0	0	700	–30		76	65	8	53		
Signal handling	V_OMax	12.0	13.0	—	dB	REC	RV	ON	ON	C	RPI	NOR	NOR	NOR	63	0	0	1 k	—		76	65	8	53		1
Signal to noise ratio	S/N (C)	60.0	63.0	—	dB	REC	RV	ON	ON	C	RPI	NOR	NOR	NOR	63	0	0	—	—	Rg = 5.1 kΩ CCIR/ARM	76	65	8	53		
T.H.D.	THD (C)	—	0.08	0.3	%	REC	RV	ON	ON	C	RPI	NOR	NOR	NOR	63	0	0	1 k	0		76	65	8	53		
Crosstalk	CT (R↔L)	—	–85.0	–79.0	dB	REC	RV	ON	OFF	B	VPI1	NOR	NOR	NOR	0	0	0	1 k	6		72	69	8	53		
	CT (VRI1 ↔VRI2)	—	–80.0	–74.0		REC	RV	ON	OFF	B	VRI1 ↔ VRI2	NOR	NOR	NOR	0	0	0	1 k	6		72/ 74	69/ 67	2	59		
	CT (VRI1 ↔RPI)	—	–80.0	–74.0		REC	RV	ON	OFF	B	VRI1 ↔ RRI	NOR	NOR	NOR	0/63	0	0	1 k	6		72/ 76	69/ 65	2	59		

Electrical Characteristics (Ta = 25°C, V_{CC} = 14 V, Dolby Level 300 mVrms at RECOUT) (Cont)

Item	Symbol	Specification Min	Typ	Max	Unit	Test Conditions REC /PB	RV /PV	MPX	NR	B/C	Input Pin	Meter	Tape Speed	Tape	Input DAC	EQ DAC	Bias DAC	fin [Hz]	REC OUT Level		Application Terminal Input R	Input L	Output R	Output L	Note
Serial digital input level	V_SH	4.0	—	5.3	V	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLK, DATA, STB	—	—	—	—	39, 40
	V_SL	–0.2	—	1.0		—	—	—	—	—	—	—	—	—	—	—	—	—	—		—	—	—	—	41
PB-output level	Vout	500	580	670	mVrms	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k HA12167	0	Low	76	65	2	59	
		665	775	900														HA12169		High					
PB-out of fset	Vofs	–100	0.0	+100	mV	PB	PV	OFF	OFF → ON	C	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—	—	2	59	2
Channel balance	ΔGv	–1.0	0.0	1.0	dB	—	—	—	—	—	—	—	—	—	—	—	—	—	—		76	65	78	63	
REC volume gain	$G_V$rec VR (Max)	17.5	19.1	21.5	dB	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	0	0	0	1 k	—	Vin = 100 mVrms	72	69	78	63	
	$G_V$rec VR (Min)	–56.0	–50.0	–47.0	dB	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	62	0	0	1 k	—	Vin = 2 Vrms	72	69	78	63	
PB volume gain	$G_{V PB}$VR (Max)	27.0	29.0	31.0	dB	PB	PV	ON	OFF	B	VRI1	NOR	NOR	NOR	0	0	0	1 k	—	Vin = 100 mVrms	72	69	78	63	
	$G_{V PB}$VR (Min)	15.0	17.0	19.0	dB	PB	PV	ON	OFF	B	VRI1	NOR	NOR	NOR	62	0	0	1 k	—	Vin = 100 mVrms	72	69	78	63	
REC volume mute level	CTrec VR (MUT)	—	–82	–75	dB	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	63	0	0	1 k	—	Vin = 2 Vrms	72	69	2	59	
REC volume max input level	Vin max (VR)	11.0	12.0	—	dBS	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	42	0	0	1 k	—	THD = 1%	72	69	2	59	
Signal to noise ratio of REC volume	S/N (VR)	78.0	84.0	—	dB	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	—	0	0	(1 k)	0	Vin = 100 mVrms Rg = 5.1 k, A-WTG	72	69	2	59	3
T.H.D. of REC volume	THD (VR)	—	0.04	0.3	%	REC	RV	ON	OFF	B	VRI1	NOR	NOR	NOR	—	0	0	1 k	0	Vin = 100 mVrms	72	69	2	59	3

Electrical Characteristics (Ta = 25°C, V_{CC} = 14 V, Dolby Level 300 mVrms at RECOUT) (Cont)

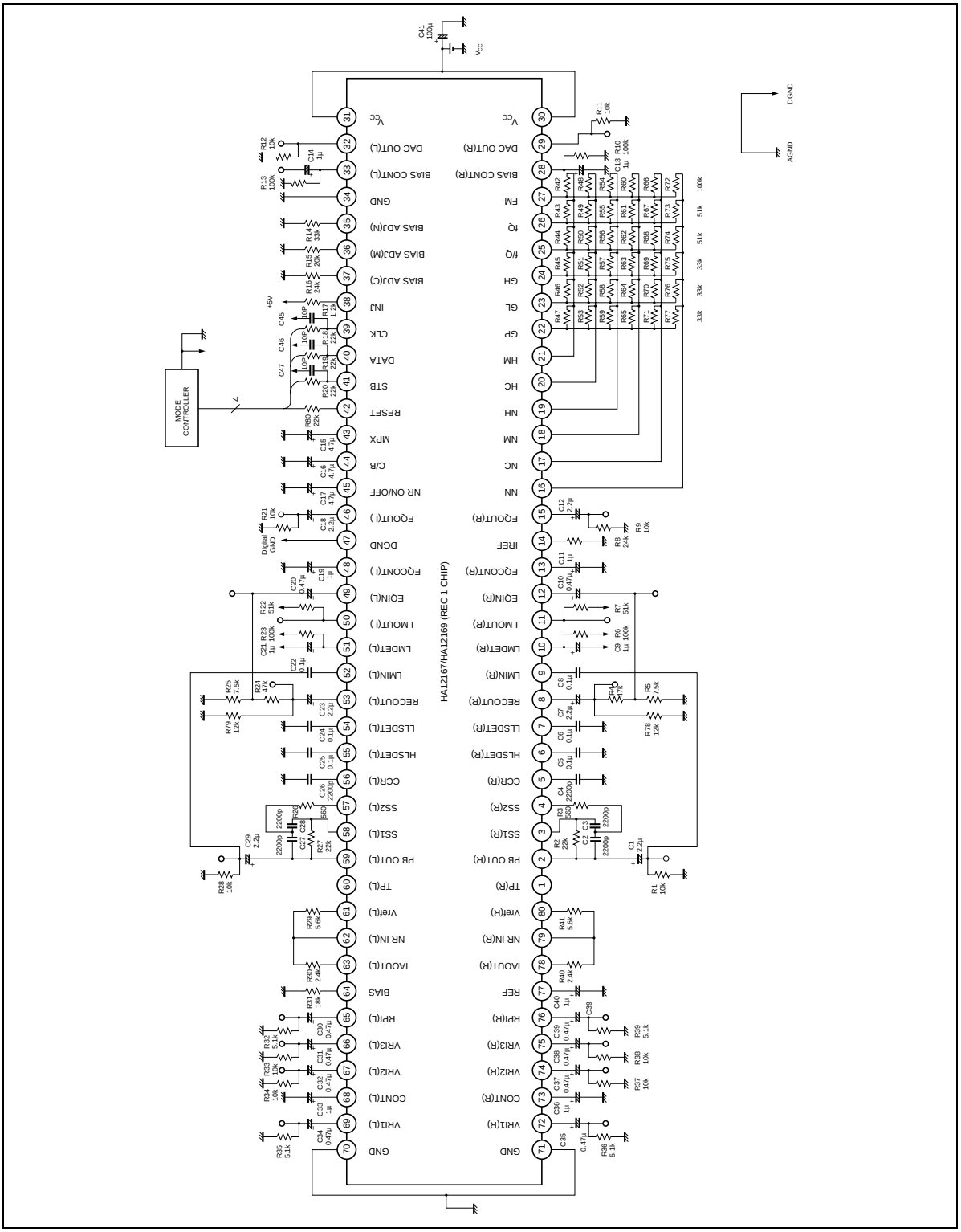
Item	Symbol	Specification Min	Specification Typ	Specification Max	Unit	Test Conditions REC /PB	RV /PV	MPX	NR	B/C	Input Pin	Meter	Tape Speed	Tape	Input DAC	EQ DAC	Bias DAC	fin [Hz]	REC OUT Level		Application Terminal Input R	Input L	Output R	Output L	Note
Equalizer gain	G_VEQ (500)	23.5	25.5	27.5	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	500	—	Vin = –32 dBs	12	49	15	46	
	G_VEQ (1 k)	23.5	25.5	27.5		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	—	Vin = –32 dBs	12	49	15	46	
	G_VEQ (5 k)	25.0	27.0	29.0		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	5 k	—	Vin = –32 dBs	12	49	15	46	
	G_VEQ (12 k)	31.0	33.5	36.0		REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	12 k	—	Vin = –32 dBs	12	49	15	46	
Equalizer volume variable a range	ΔG_VEQ (1 k)	6	8	10	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0/30	0	1 k	—	Vin = –32 dBs	12	49	15	46	
Equalizer max input level	Vin Max (EQ)	–10.0	–9.0	—	dBS	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	16	0	1 k	—	THD = 1%	12	49	15	46	
Equalizer volume mute gain	G_VEQ (MUT)	—	–75	–62	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	31	0	1 k	—	Vin = –9 dBs 1 kHz BPF	12	49	15	46	
Signal to noise radio of equalizer	S/N (EQ)	57.0	62.0	—	dB	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	Rg = 5.1 kΩ, A-WTG	12	49	15	46	
THD of equalizer	THD (EQ)	—	0.2	0.5	%	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	16	0	1 k	—	Vin = –26 dBs	12	49	15	46	
Equalizer of fset	Vofs (EQ)	–400	0.0	+400	mV	REC	RV	OFF	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—	—	15	46	4
Level meter output	LM (0 dB)	2.50	2.75	3.00	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	0		9	52	11	50	
	LM (12 dB)	3.55	3.85	4.15	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	12		9	52	11	50	
	LM (–20 dB) [1]	0.70	1.00	1.30	V	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	1 k	–20		9	52	11	50	
	LM (–20 dB) [2]	2.45	2.75	3.05	V	REC	RV	ON	OFF	B	RPI	20 dB	NOR	NOR	63	0	0	1 k	–20		9	52	11	50	

Electrical Characteristics (Ta = 25°C, V_{CC} = 14 V, Dolby Level 300 mVrms at RECOUT) (Cont)

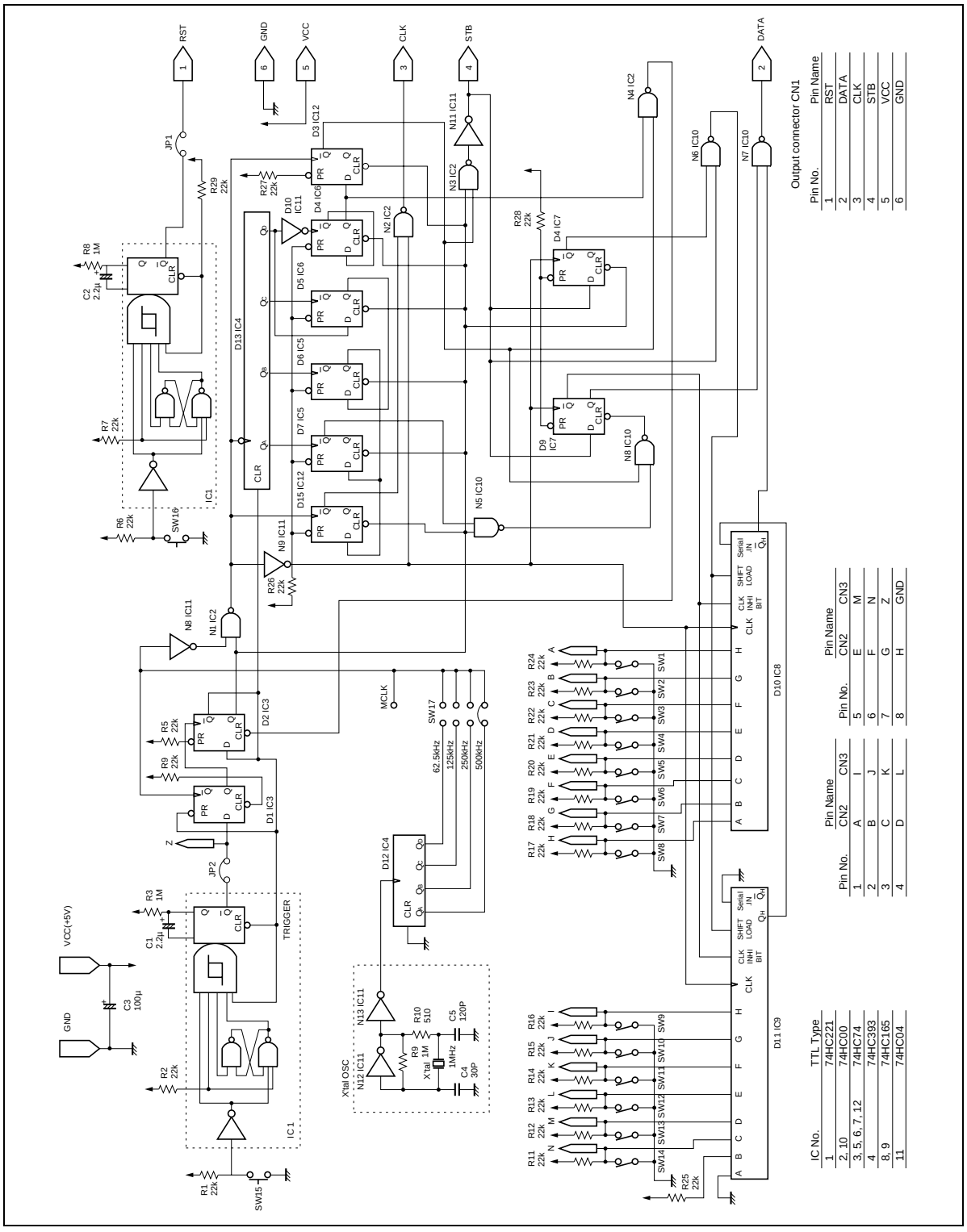
		Specification				Test Conditions															Application Terminal				
																					Input		Output		
Item	Symbol	Min	Typ	Max	Unit	REC /PB	RV /PV	MPX	NR	B/C	Input Pin	Meter	Tape Speed	Tape	Input DAC	EQ DAC	Bias DAC	fin [Hz]	REC OUT Level		R	L	R	L	Note
Level meter of fset	LMofs 1	—	150	300	mV	REC	RV	ON	OFF	B	RPI	NOR	NOR	NOR	63	0	0	—	—	No signal	—	—	11	50	
	LMofs 2	—	200	350		REC	RV	ON	OFF	B	RPI	20 dB	NOR	NOR	63	0	0	—	—	No signal	—	—	11	50	
DAC output Max	V_B Max	11.0	12.0	13.0	V	REC	RV	OFF	OFF	B	VRI1	NOR	NOR	MET	63	0	63	—	—		—	—	29	32	
DAC output Min	V_B Min	—	0.5	1.0	V	REC	RV	OFF	OFF	B	VRI1	NOR	NOR	MET	63	0	0	—	—		—	—	29	32	

Note: 1. HA12167: V_{CC} = 12 V
HA12169: V_{CC} = 11 V
2. V_{CC} = 15 V
3. Adjust the input volume to Dolby level.
4. V_{CC} = 15 V

Test Circuit

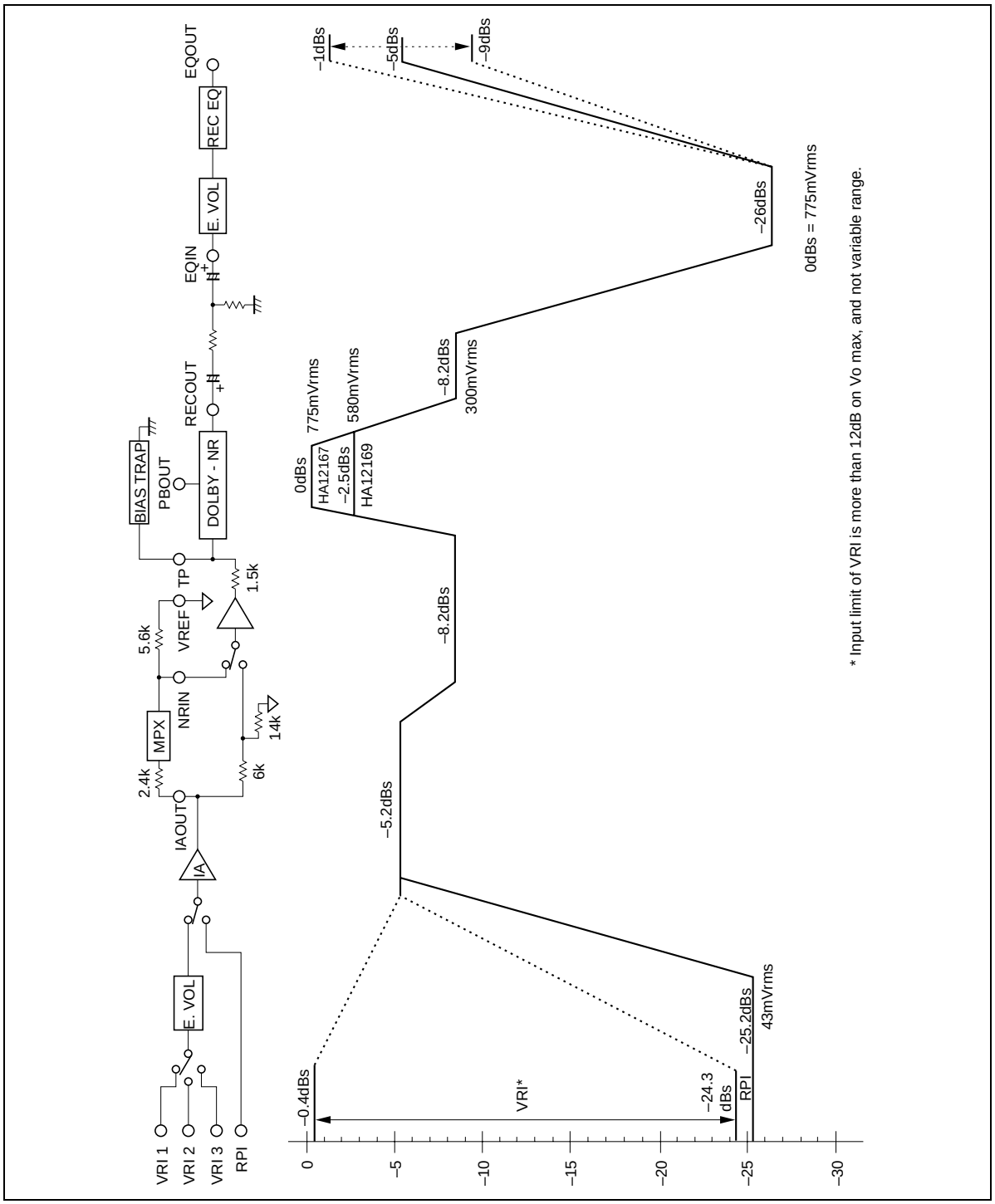


Mode Controller

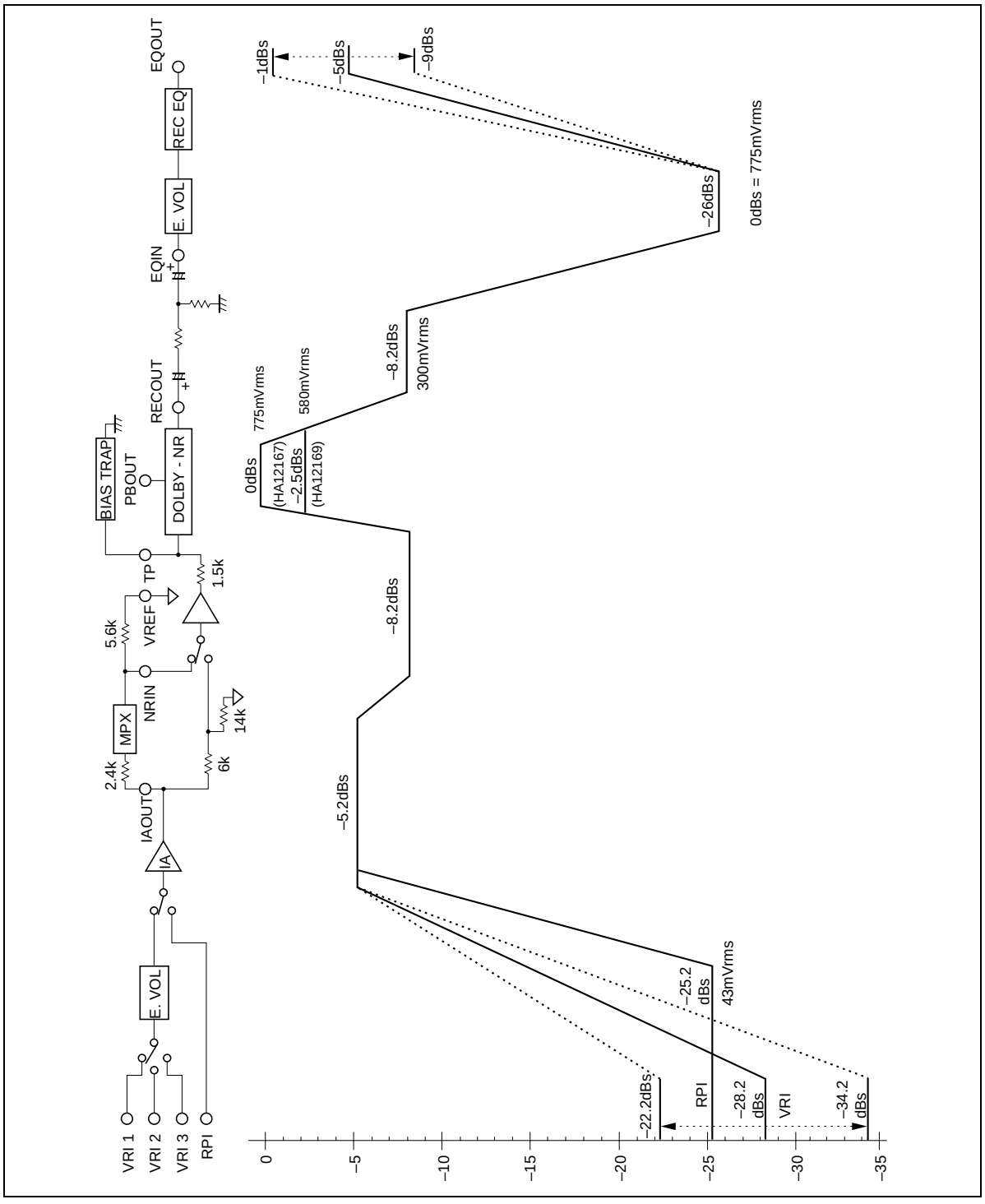


Level Diagram

REC Mode (1 kHz NR-OFF)



PB Mode (1 kHz NR-OFF)



Application Note

Power Supply Range

HA12167FB/HA12169FB are designed to operate on either single supply or split supply.

The operating range of the supply voltage is shown in table 1.

Table 1 Supply Voltage

Type No.	Single Supply	Split Supply
HA12167FB	12 V to 15 V	±6.0 V to 7.5 V
HA12169FB	11 V to 15 V	±6.0 V to 7.5 V

The lower limit of supply voltage depends on the line output reference level.

The minimum value of the overload margin is specified as 12 dB by Dolby Laboratories. HA12167 series are provided with two line output level, which will permit an optimum overload margin for power supply conditions.

Reference Voltage

For the single supply operation these devices provide the reference voltage of half the supply voltage that is the signal grounds. As the peculiarity of these devices, the capacitor for the ripple filter is very small about 1/100 compared with their usual value. The Reference voltage are provided for the left channel and the right channel separately. The block diagram is shown as figure 1.

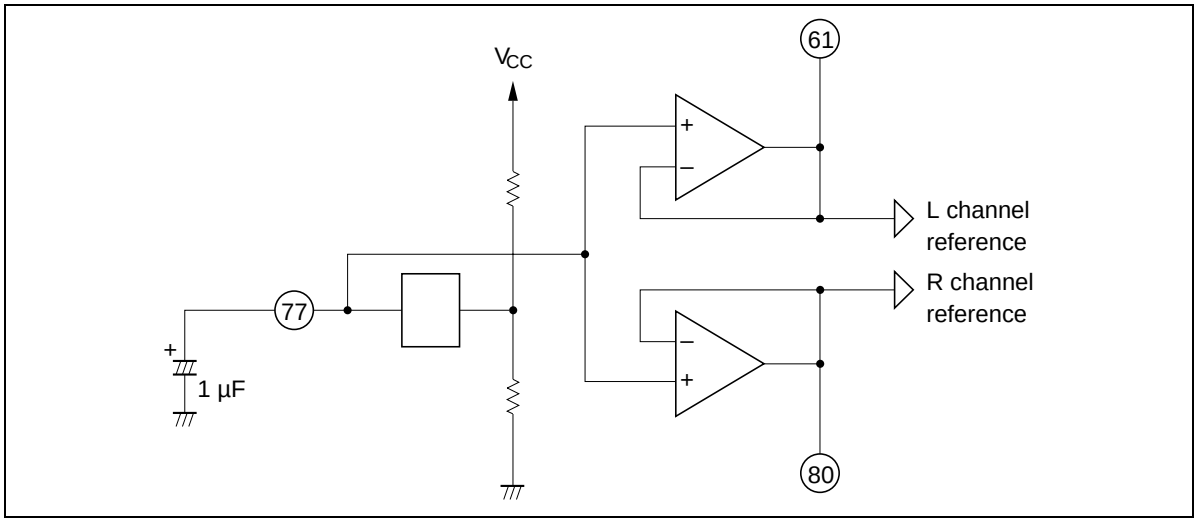


Figure 1 The Block Diagram of Reference Voltage Supply

Operating Mode Control

HA12167FB/HA12169FB provides fully electronic switching circuits. All switches are controlled by serial data.

Table 2 Threshold Voltage (VTH)

Pin No.	Lo	Hi	Unit
42	–0.2 to 1.5	3.5 to 5.3	V
39, 40, 41	–0.2 to 1.0	4.0 to 5.3	V

Notes: 1. Voltages shown above are determined by internal circuits of LSI when take pin 47 (DGND pin) as reference pin. On split supply use, same VTH can be offered by connecting DGND pin to GND pin.
This means that it can be controlled directly by micro processor.
2. Each pins are on pulled down with 100 kΩ internal resistor.
Therefore, it will be low-level when each pins are open.
3. Note on serial data inputting
(a) The clock frequency on CLK must be less than 500 kHz.
(b) Over shoot level and under shoot level of input signal must be the value shown below.

When connecting microcomputer or Logic-IC with HA12167FB/HA12169FB directly, there is apprehension of rash-current under some transition timming of raising voltage or falling voltage at V_{CC} ON/OFF.

For this countermeasure, connect 10 kΩ to 20 kΩ resistor with each pins. It is shown in test circuit on this data sheet.

In case of changing NR-ON/OFF at the C-mode, for the countermeasure of the noise of pop, perform the following processes.

In case of changing NR-OFF to NR-ON at C-mode. C-mode, NR-OFF → B-mode, NR-OFF → B-mode, NR-ON → C-mode, NR-ON.

In case of changing NR-ON to NR-OFF at C-mode. C-mode, NR-ON → B-mode, NR-ON → B-mode, NR-OFF → C-mode, NR-OFF.

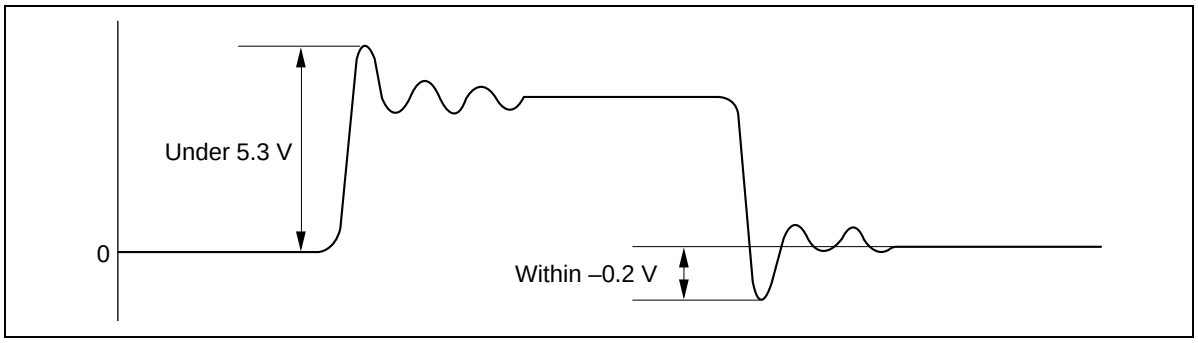


Figure 2 Input Level

Serial Data Formatting

14 bit shift register is employed.

CLK and data are stored during STB being high and data is latched when STB goes high to low.

Reset goes reset a state when reset low and high releasles reset. (High fixed at use time)

Attention Point of Serial Interface

- Reset goes low condition when a power supply is ON or OFF.
- Characteristics select of Bias DAC is connected with equalizer tape selector.
- Bias DAC register is all low when a time of tape select.
- Bias DAC register is all low and Bias DAC out is dropped low level at compulsion by force.
- Input pin select, REC/PB select and Input volume gain select does not select at the same time.
- Input volume must go mute condition when selected of RPI is input pin select.

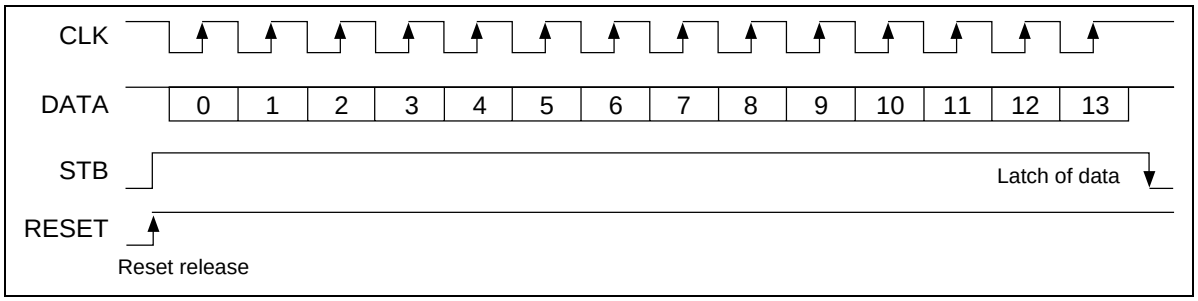


Figure 3 Serial Data Timming Chart Figure

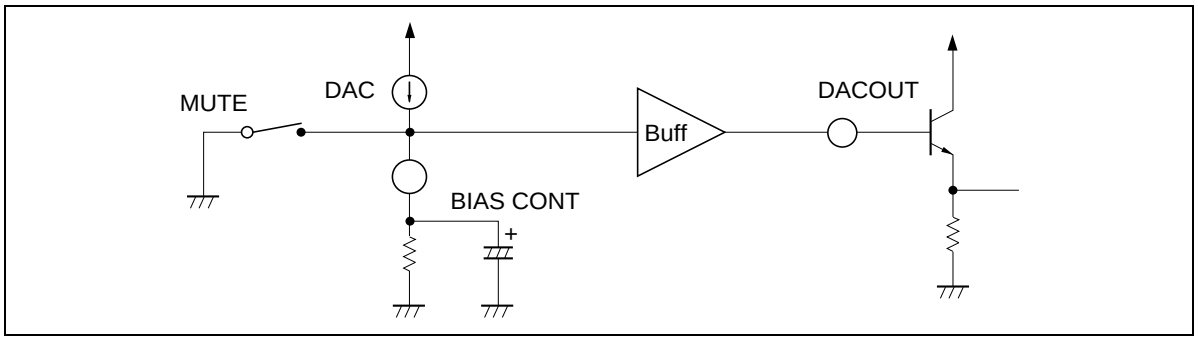


Figure 4 Bias DAC Output Circuit

Serial Data Formatting

Bit No.	Mode Control			Reset	Input Voltage		Reset	Eaqualizer Voltage		Reset	Basic DAC		Reset
0	Tape selector 1	bit 0 / bit 1	H / L	L	L channel	I-bit 0	L	L channel	E-bit 0	L	L channel	B-bit o	L
		H	Metal / Normal										
		L	Crom / Normal										
1	Tape selector 2			L		I-bit 1	L		E-bit 1	L		B-bit 1	L
2	Tape speed	H	Hi speed selection	L		I-bit 2	L		E-bit 2	L		B-bit 2	L
		L	Normal speed selection										
3	Meter sensitivity	H	Meter sensitivity 20 dB up	L		I-bit 3	L		E-bit 3	L		B-bit 3	L
		L	Meter sensitinity normal										
4	Input selector 1	bit 4 / bit 5	H / L	L		I=bit 4	L		E-bit 4	L		B-bit 4	L
		H	VRI3 / RPI										
		L	VRI2 / VRI1										
5	Input selector 2			L		I-bit 5	H		—	—		B-bit 5	L
6	REC/PB	H	PB mode selection	H	R channel	I-bit 0	L	R channel	E-bit 0	L	R channel	B-bit 0	
		L	REC mode selection										
7	Input voltage gain	H	PB mode volume gain	H		I-bit 1	L		E-bit 1	L		B-bit 1	L
		L	Rec mode volume gain										
8	MPX	H	ON	L		I-bit 2	L		E-bit 2	L		B-bit 2	L
		L	OFF										
9	NR	H	ON	L		I-bit 3	L		E-bit 3	L		B-bit 3	L
		L	OFF										
10	B/C	H	C	L		I-bit 4	L		E-bit 4	L		B-bit 4	L
		L	B										
11	—	—		—		I-bit 5	H		—	—		B-bit 5	L
12	Registor selector 1	bit 12 / bit 13	H / L										
		H	Bias DAC / Input volume										
		L	Equalizer volume / Mode control										
13	Registor selector 2												

Input Volume Register

I-bit 5	I-bit 4	I-bit 3	I-bit 2	I-bit 1	I-bit 0	Gain
L	L	L	L	L	L	Increase
L	L	L	L	L	H	↑
L	L	L	L	H	L	:
L	L	L	L	H	H	:
:	:	:	:	:	:	:
:	:	:	:	:	:	↓
H	H	H	H	H	L	Decrease
H	H	H	H	H	H	Mute

Equalizer Volume Register

E-bit 4	E-bit 3	E-bit 2	E-bit 1	E-bit 0	Gain
L	L	L	L	L	Increase
L	L	L	L	H	↑
L	L	L	H	L	:
L	L	L	H	H	:
:	:	:	:	:	:
:	:	:	:	:	↓
H	H	H	H	L	Decrease
H	H	H	H	H	Mute

Bias DAC Register

B-bit 5	B-bit 4	B-bit 3	B-bit 2	B-bit 1	B-bit 0	Bias
L	L	L	L	L	L	Mute
L	L	L	L	L	H	Decrease
L	L	L	L	H	L	↑
L	L	L	L	H	H	:
:	:	:	:	:	:	:
:	:	:	:	:	:	:
H	H	H	H	H	L	↓
H	H	H	H	H	H	Increase

MPX ON/OFF Switch

MPX-OFF mode means that signal from input amp doesn't go through the MPX filter, but signal goes through the NR circuit after being attenuated 3 dB by internal resistor. Refer to figure 5. For not cause any level difference between MPX-ON mode and MPX-OFF mode, it is requested to use MPX-filter which has definitely 3 dB attenuated. And when applying other usage except figure 5,

take consideration to give bias voltage to NR-IN terminal by resistor or so on because internal of NR-IN terminal has no bias resistor.

Application as for the Dubbing Cassette Deck

HA12167FB/HA12169FB series has unprocessor signal from recording out terminals during playback mode. So, it is simply applied for dubbing cassette decks.

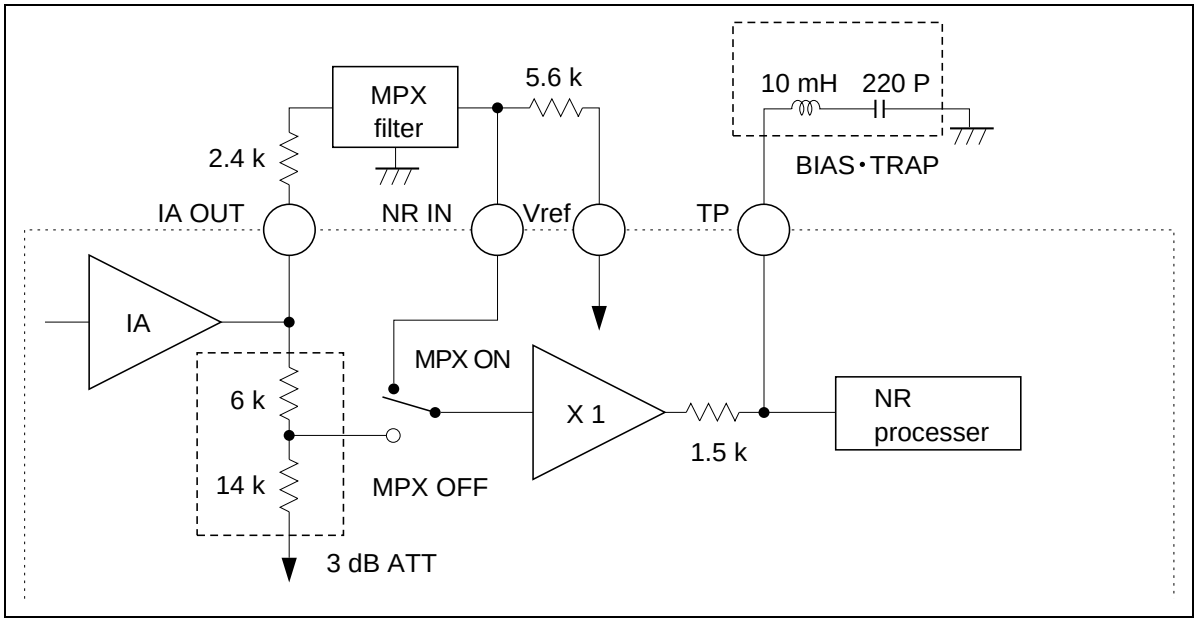


Figure 5 MPX ON/OFF Switch Block Diagram

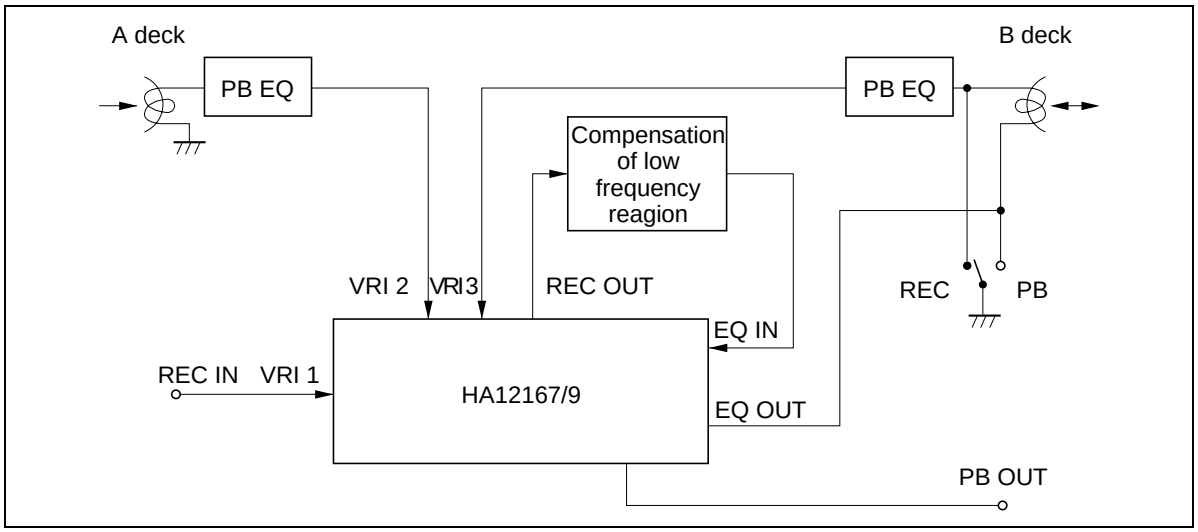


Figure 6 Application for Dubbing Deck

Injector Current

HA12167FB/HA12169FB has logic circuit which is fabricated by I^2L into IC. To operate this circuit, it is required enough injector current. Injector current goes into from the INJ pin (pin 38) and external resistor is required to connect to this pin for adequate current. The value of external resistor is obtained by using following equations. And put them with ±10% tolerance value which is calculated. V_{INJ} can allow to connect to V_{CC} shown below. Large injector current fear to cause mis-operation of Logic under the condition of high temperature. Also, small injector current fear to cause mis-operation (stop operation). Under the condition of low temperature. Therefore, pay attention to have good stability of V_{INJ}.

$$R_{INJ} = \frac{V_{INJ} - 0.7}{3.6} \quad [k\Omega]$$ Single supply

$$R_{INJ} = \frac{V_{INJ} + V_{EE} - 0.7}{3.6} \quad [k\Omega]$$ Split supply

Gain Control of Electronic Volume

HA12167FB/HA12169FB is designed in order to change the gain by DAC fabricated into IC. To reduce the click noise when changing volume gain instantaneously, required to connect the capacitor and resistor (CR time constant) to CONT pin (pin 13, 48, 68, 73). These terminals are also be used as output pin of DAC. Therefore, by forcing voltage and current to these terminals, it is applicable to control volume gain directly. But, voltage forced to these terminals must be from $V_{CC}/2$ –2 V to $V_{CC}/2$ (for split supply use, –2 V to 0 V) in this case. And, this case, change of a gain depending on a temperature gets large.

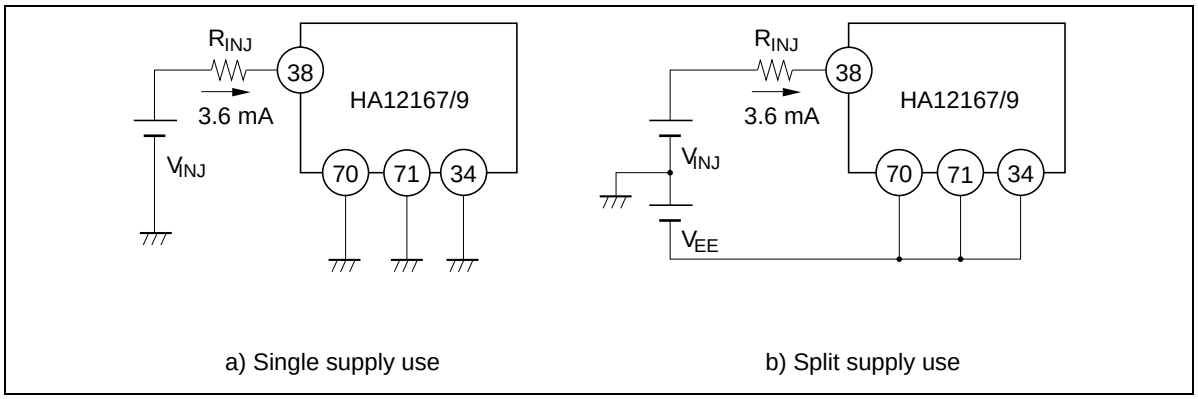


Figure 7 Injector Current Application

The Tolerances of External Components for Dolby NR-Block

For adequate Dolby NR tracking response, take external components shown below.

For C5, C6, C24, and C25, please employ a few object of the leak, though you can be useful for an electrolytic-capacitor.

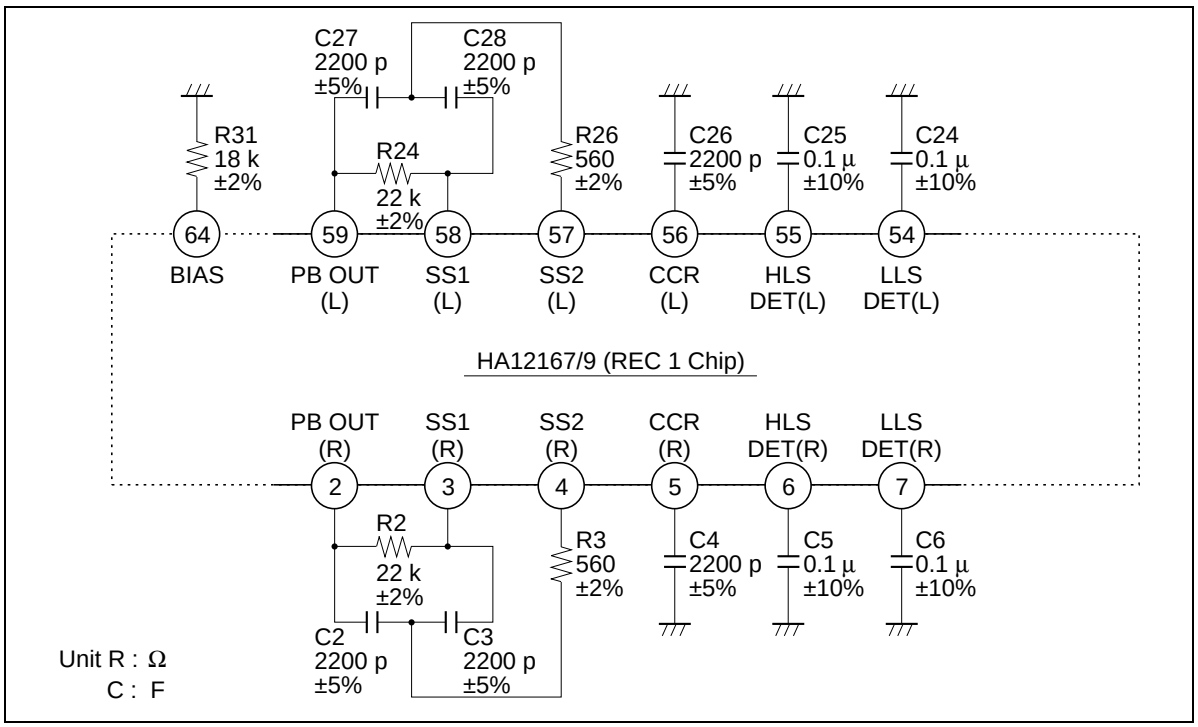


Figure 8 Tolerances of External Components

BIAS DAC

The full-scale of DAC is computed by the formula mentioned below.

$$V_{29} = \frac{2.4}{R_{14\ to\ 16}} \times R_{10} \quad [V]$$

$$V_{32} = \frac{2.4}{R_{14\ to\ 16}} \times R_{13} \quad [V]$$

R_{14}: Normal Tape (pin 35)

R_{15}: Metal Tape (pin 36)

R_{16}: Chrome Tape (pin 37)

The maximum source current of DAC output (pin 29, 32) is 2 mA. Therefor the Bias-osc is drived through external transisitor of emitter-follower.

Level Meter

The coupling capacitor of LMIN pin (9 pin and 52 pin).

For these capacitors, please employ a small object of the leak.

The Application of Equalizer Frequency Response

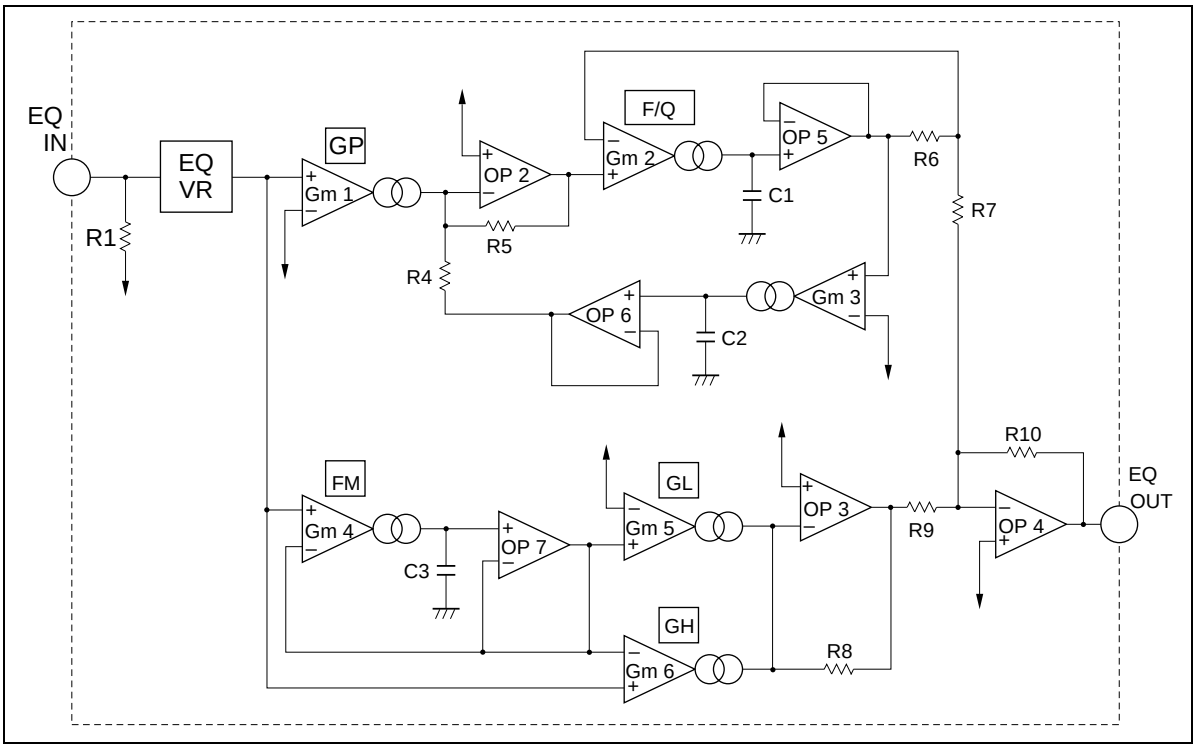


Figure 9 REC Equalizer Block Diagram

Transfer Function:

$$\frac{Vout}{Vin} = G_V \left(Gm5 \cdot \frac{R_8 \cdot R_{10}}{R_9} \cdot \frac{1+\frac{C3}{Gm4}\cdot\frac{Gm6}{Gm5}\cdot S}{1+\frac{C3}{Gm4}\cdot S} + Gm1 \cdot \frac{R_4 \cdot R_{10}}{R_6+R_7} \cdot \frac{\frac{C3}{Gm4}\cdot S}{1+\frac{R_4}{R_5}\cdot\frac{R_7}{R_6+R_7}\cdot\frac{C2}{Gm3}\cdot S+\frac{R_4}{R_5}\cdot\frac{C1}{Gm2}\cdot\frac{C2}{Gm3}\cdot S^2} \right)$$

$$= \frac{9}{R_{REF}} \left(R_{GL} \cdot \frac{1+6.67\times10^{-10}\frac{R_{FM}\cdot R_{GH}}{R_{GL}}\cdot S}{1+6.67\times10^{-10} R_{FM}\cdot S} + R_{GP} \cdot \frac{3.0\times10^{-10}\cdot R_{FQ}\cdot S}{1+4.5\times10^{-11}\cdot R_{FQ}\cdot S+2.5\times10^{-20}\cdot R_{FQ}\cdot R_{F/Q}\, S^2} \right)$$

Note: R_{REF}.... 14 pin bias resistance
G_V..... Gain of EQ-VR

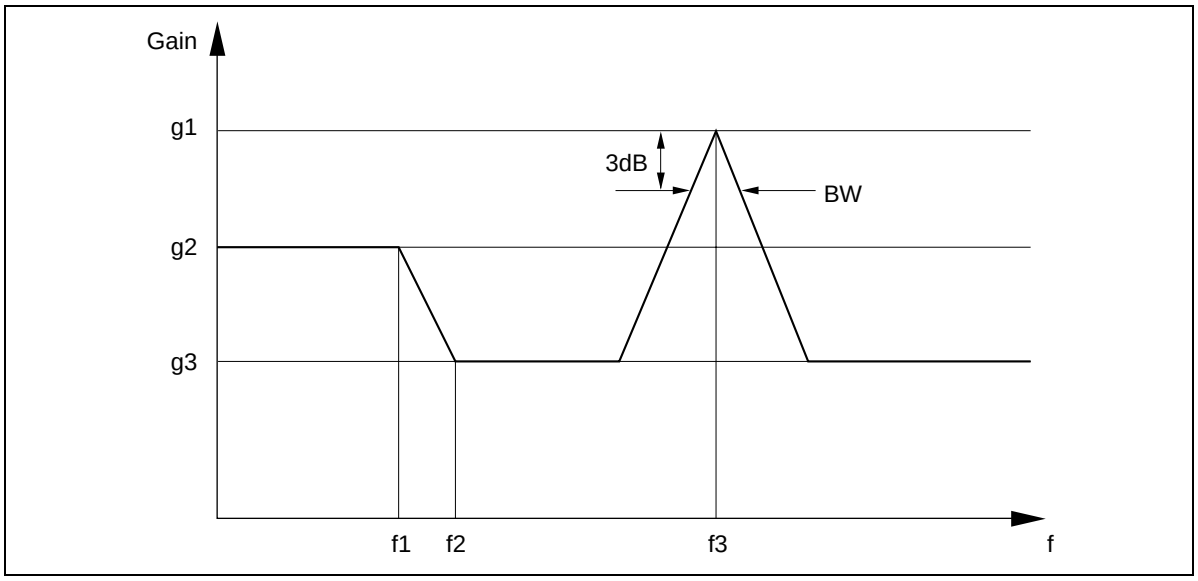


Figure 10 REC Equalizer Frequency Response

$$g1 = \frac{9}{R_{REF}}(6.67 \times R_{GP} + R_{GH})$$
$$g2 = \frac{9 \times R_{GL}}{R_{REF}}$$
$$g3 = \frac{9 \times R_{GH}}{R_{REF}}$$

} when Gain of EQ - VR is center

$$f1 = \frac{1}{2\pi \times 6.67 \times 10^{-10} \times R_{FM}}$$

$$f2 = \frac{R_{GL}}{2\pi \times 6.67 \times 10^{-10} \times R_{FM} \times R_{GH}}$$

$$f3 = \frac{1}{2\pi} \cdot \frac{0.3}{\sqrt{2.25 \times 10^{-21} \times R_{FQ} \times R_{F/Q}}}$$

$$BW = \frac{1}{4\pi \times 2.78 \times 10^{-10} \times R_{F/Q}}$$

$$Q = \frac{f3}{BW} = 3.51 \times \sqrt{\frac{R_{F/Q}}{R_{FQ}}}$$

Equalizer Characteristics Control Using a Bias DAC

When only one of the bias DAC channels is used, any one of the six parameters (FM, fQ, f/Q, GH, GL, and GP) that set the equalizer's chara cteristics can controlled by the unused bias DAC.

The figure below gives one example.

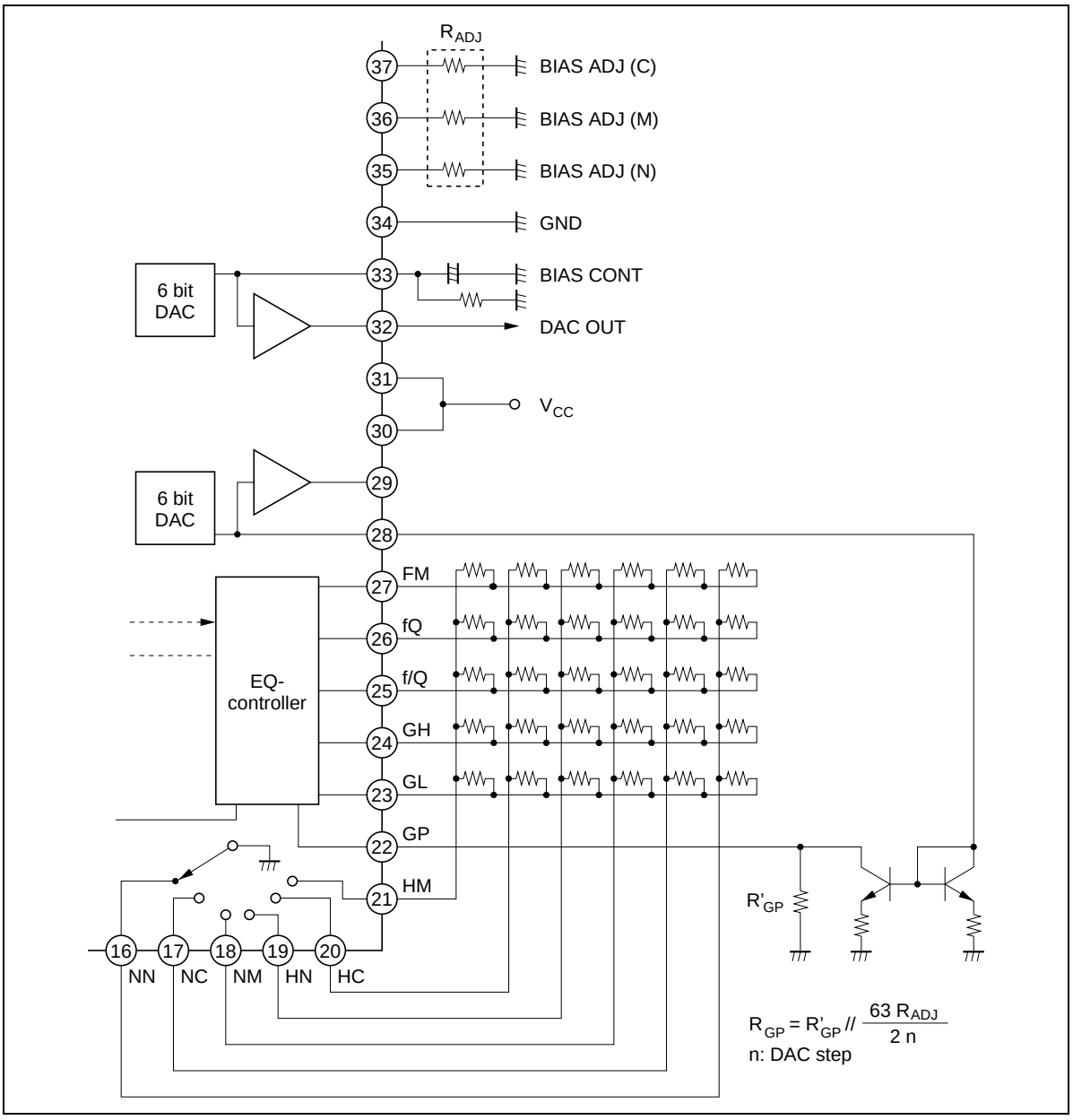


Figure 11 Bias DAC Control of the GP Parameter

Figures 12, 13, and 14 show the characteristics when GP is controlled by a bias DAC.

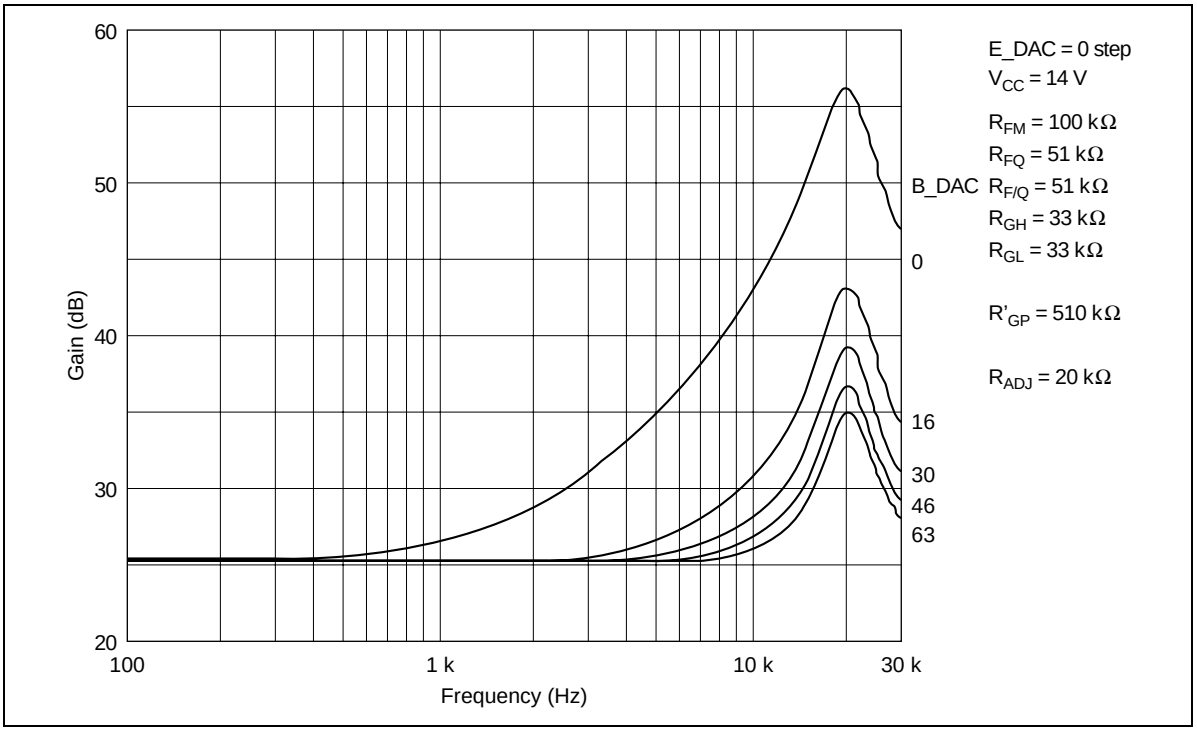


Figure 12 Equalizer Gain vs. Frequency

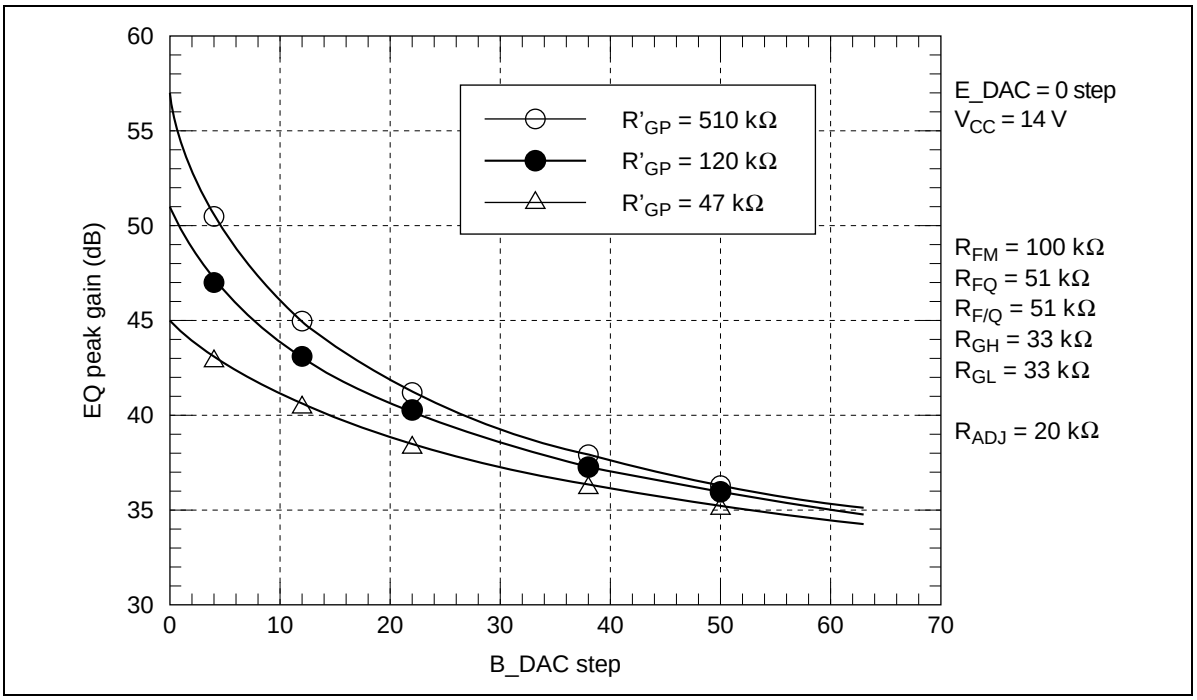


Figure 13 Equalizer Peak Gain vs. DAC Step Characteristics (1)

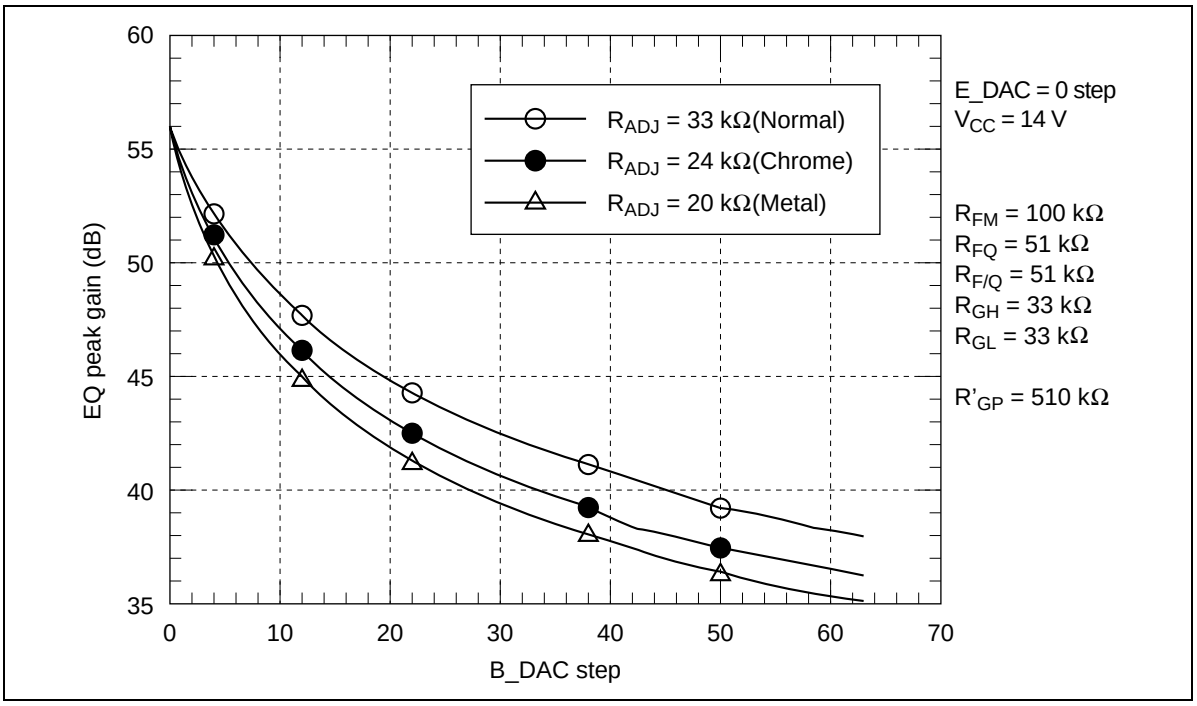


Figure 14 Equalizer Peak Gain vs. DAC Step Characteristics (2)

When the (variable) width of the DAC step is to be changed, the gain at step 0 or at step 63 must be changed. The step 0 gain can be changed using R'_{GP} as shown in figure 13. Also, R'_{GP} can be switched using the tape selector, as shown in figure 15. However, it is necessary to take into account that the value of R_{ADJ}, which sets the step 63 gain, is also used for the output bias. When the load resistance on pin 33 is R_L, the following formula gives the output bias, V_{BMAX}.

$$V_{BMAX} = 2.4 \times R_L / R_{ADJ}$$

Therefore, it is possible to compensate the output bias, V_{BMAX} for the R_{ADJ} setting by changing R_L.

Note: R_{ADJ} should be in the range 16 kΩ to 75 kΩ.

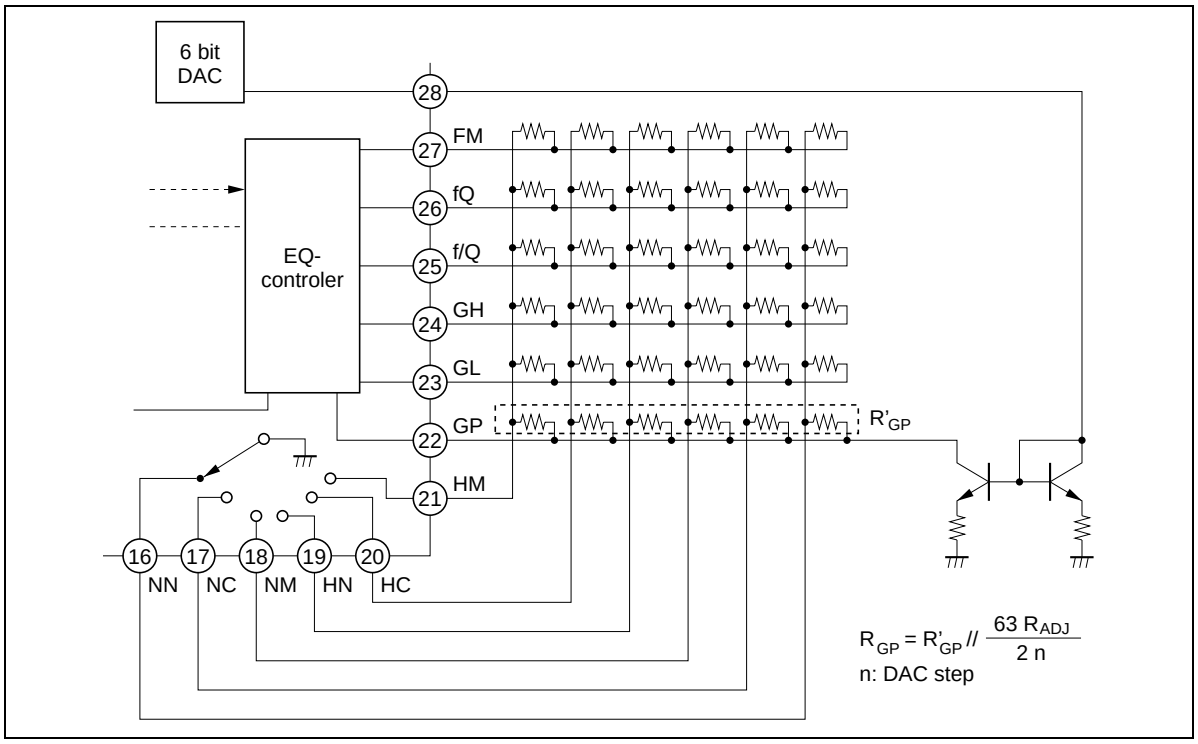
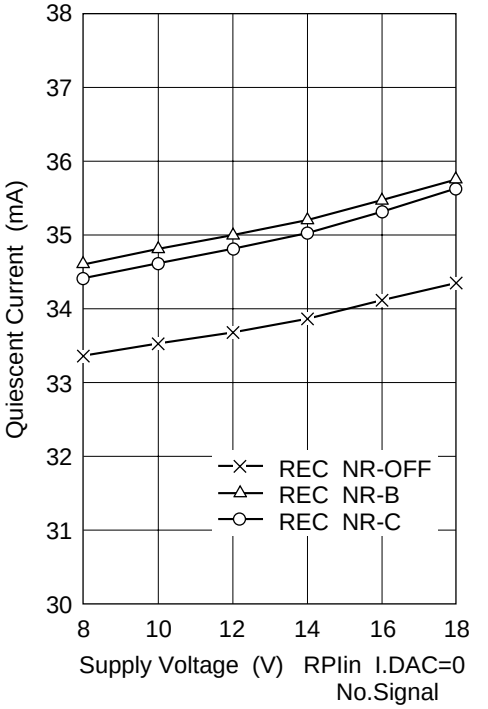
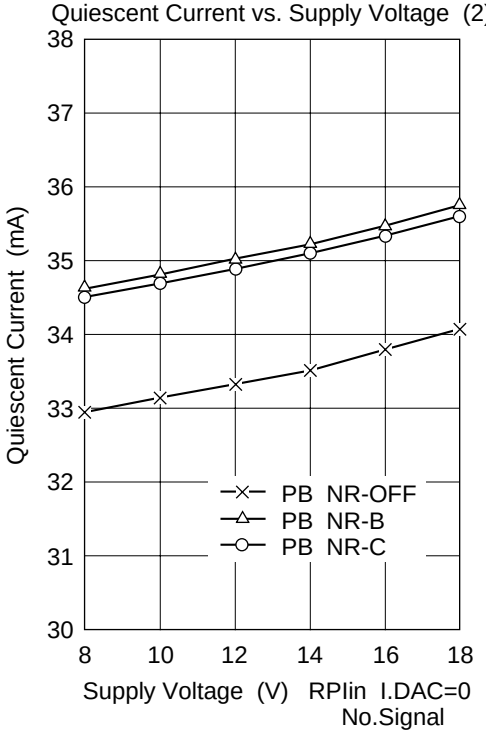


Figure 15 Switch by Tape Select

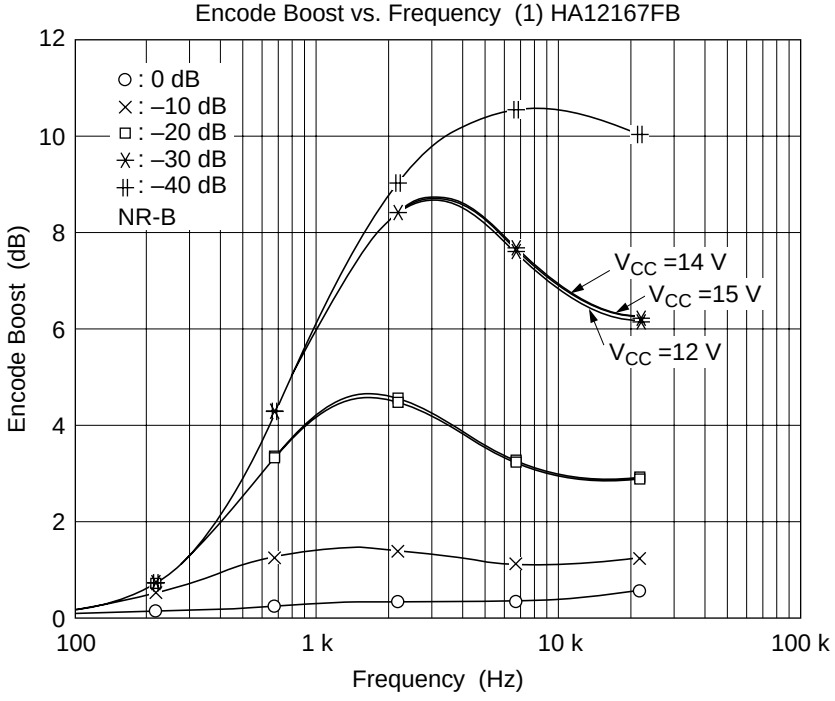
Quiescent Current vs. Supply Voltage (1)



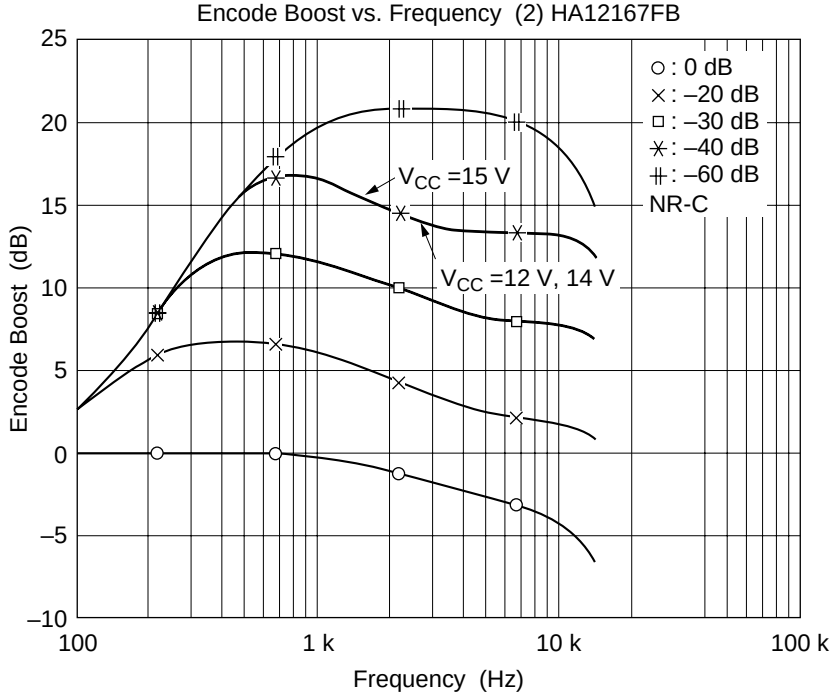
Quiescent Current vs. Supply Voltage (2)



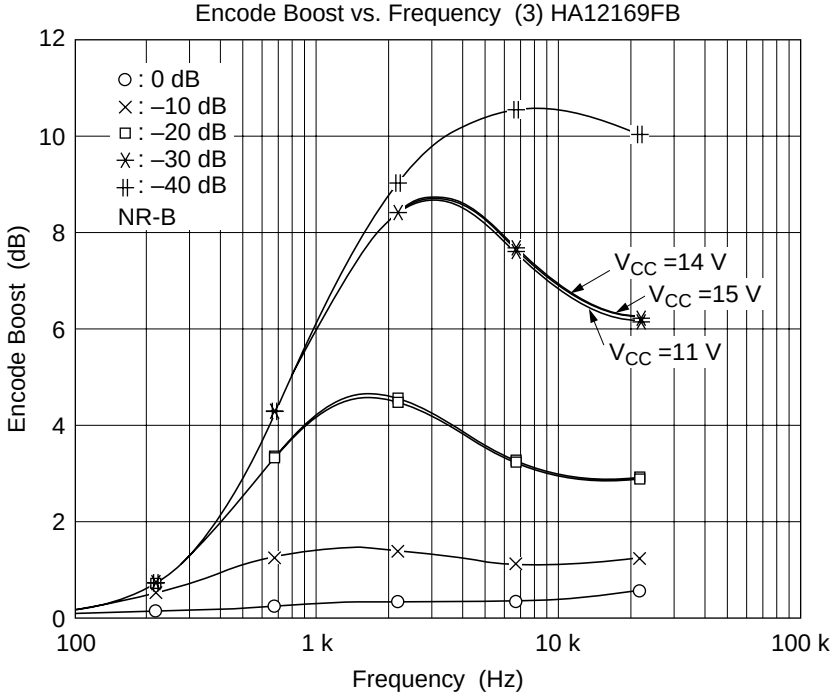
Encode Boost vs. Frequency (1) HA12167FB



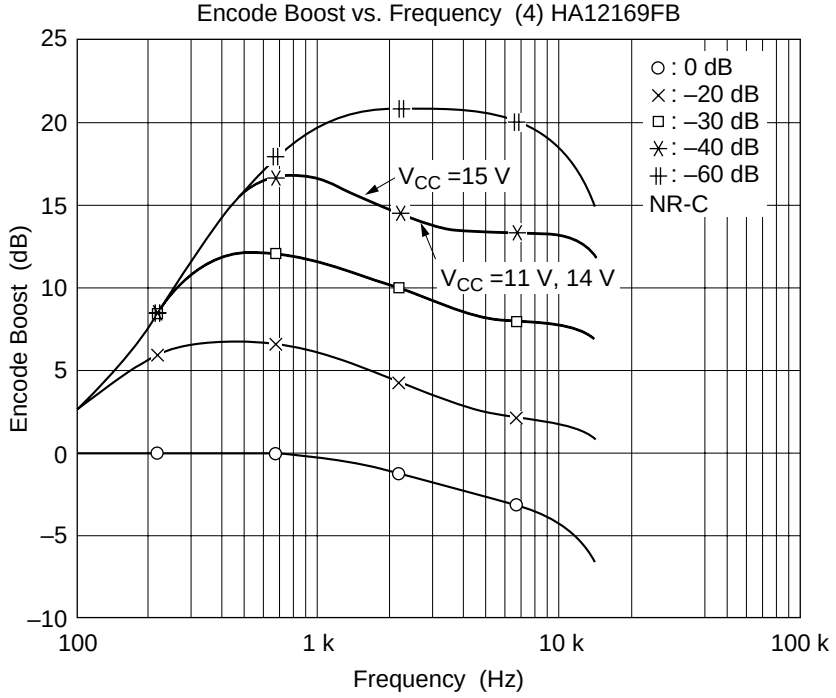
Encode Boost vs. Frequency (2) HA12167FB



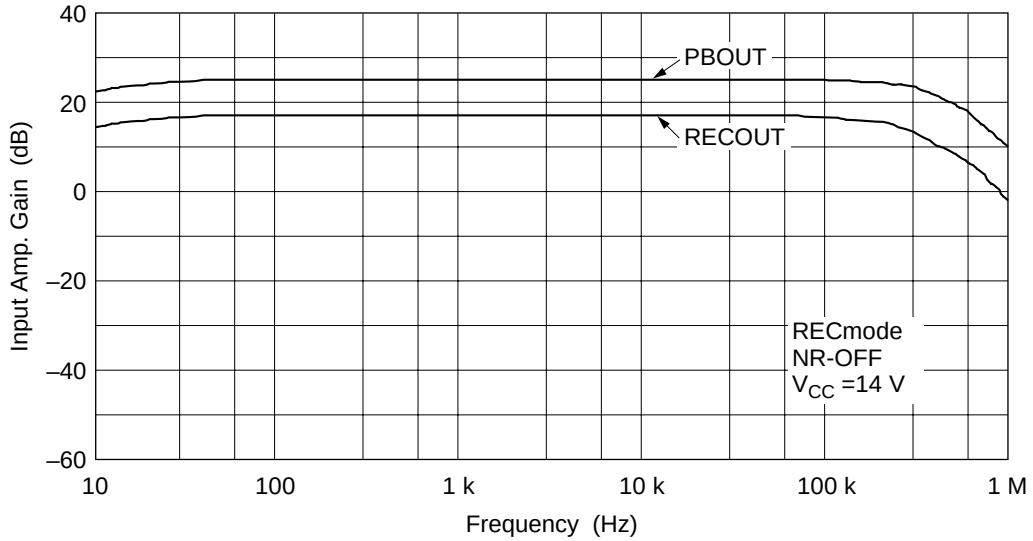
Encode Boost vs. Frequency (3) HA12169FB



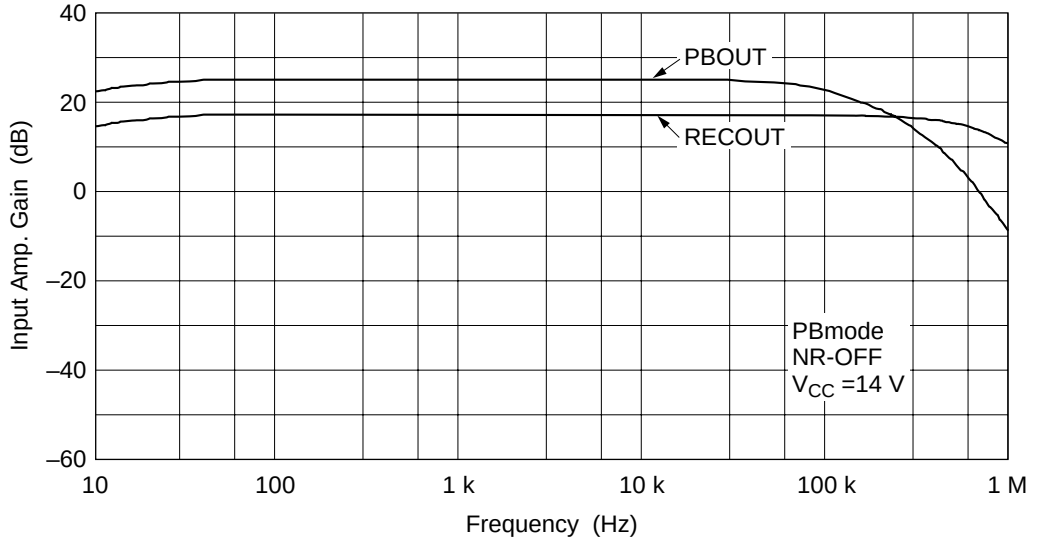
Encode Boost vs. Frequency (4) HA12169FB



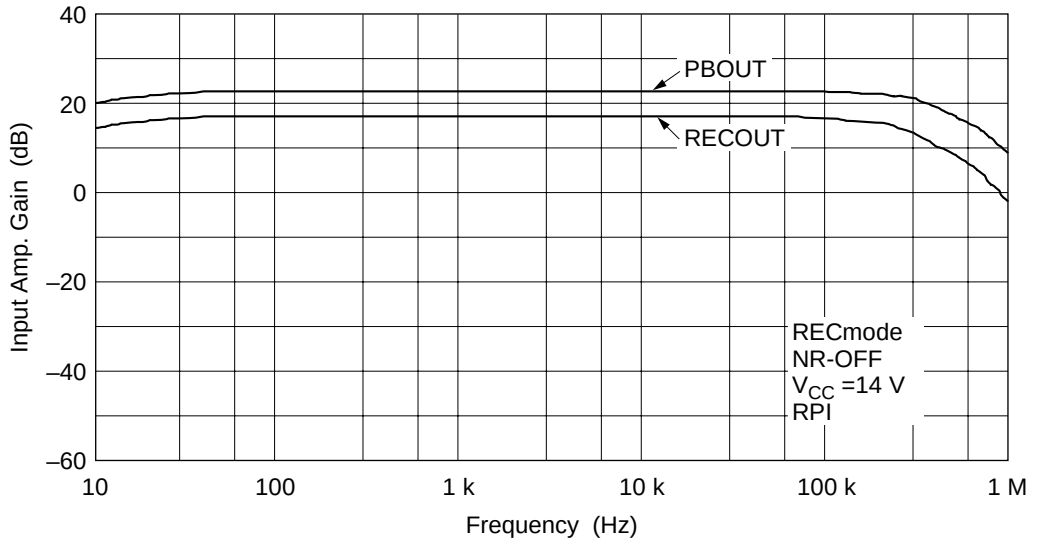
Input Amp. Gain vs. Frequency (1) HA12167FB

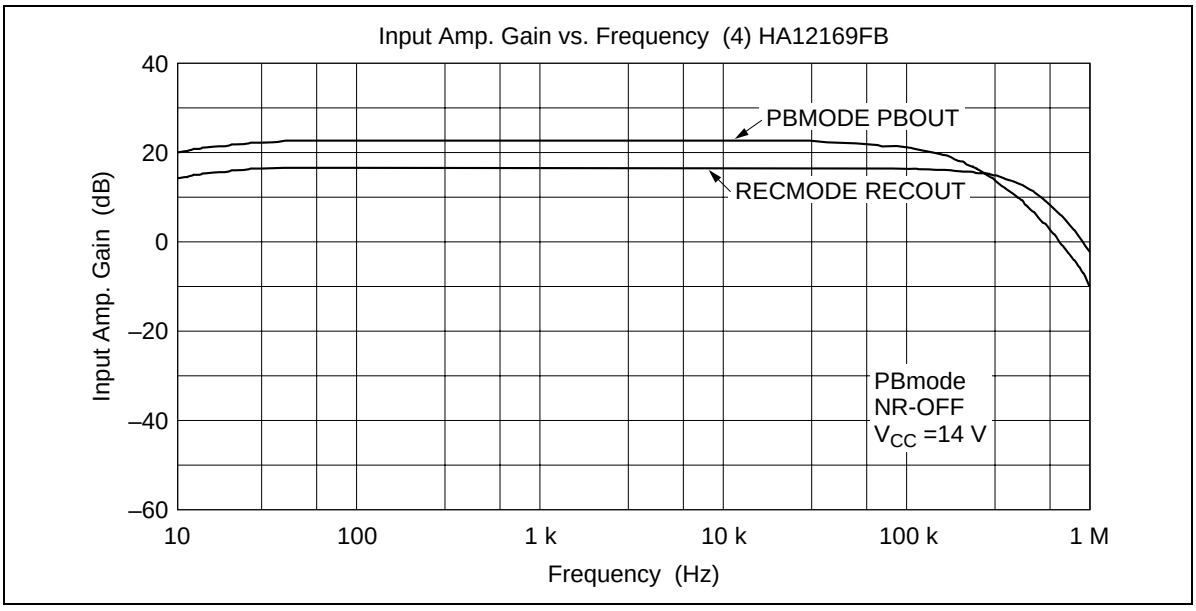


Input Amp. Gain vs. Frequency (2) HA12167FB

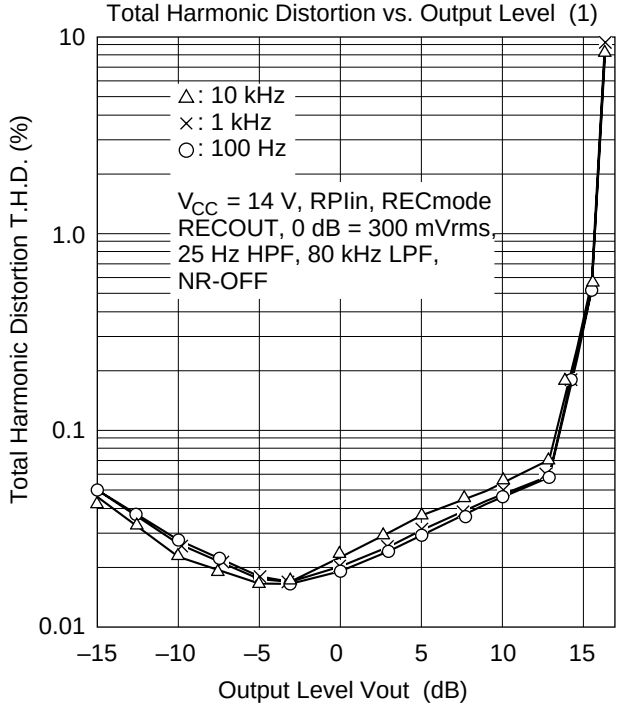


Input Amp. Gain vs. Frequency (3) HA12169FB

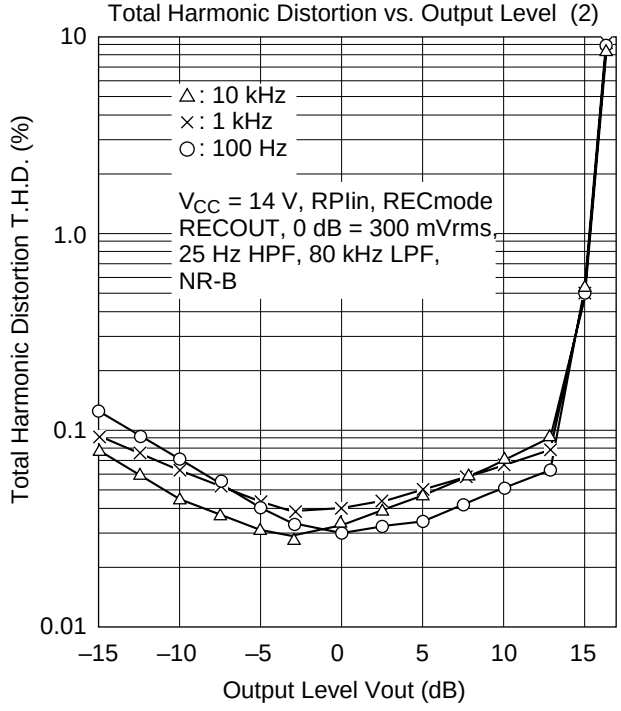



Input Amp. Gain vs. Frequency (4) HA12169FB
40
20
0
–20
–40
–60
Input Amp. Gain (dB)
10
100
1 k
10 k
100 k
1 M
Frequency (Hz)
PBMODE PBOUT
RECMODE RECOUT
PBmode
NR-OFF
V_{CC} =14 V

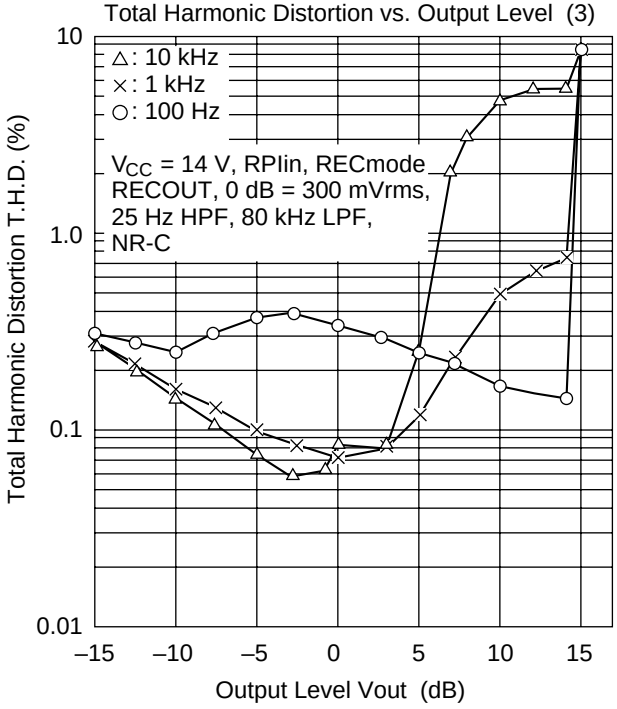
Total Harmonic Distortion vs. Output Level (1)



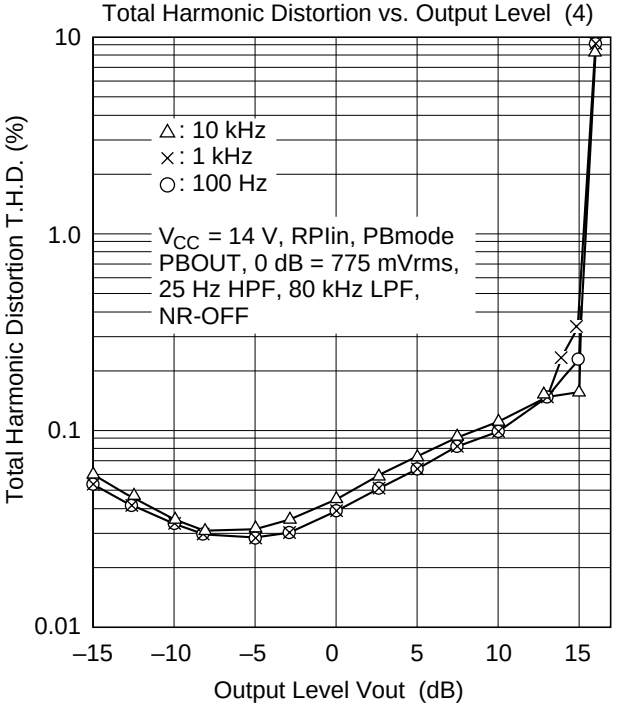
Total Harmonic Distortion vs. Output Level (2)



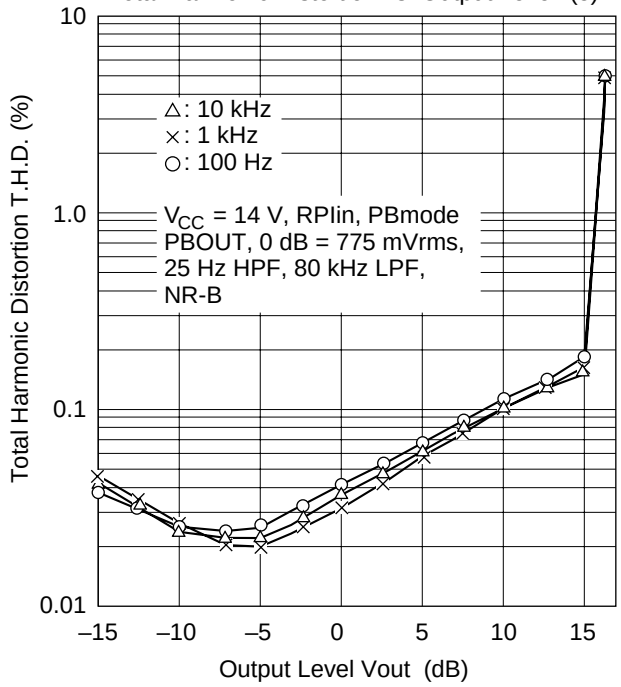
Total Harmonic Distortion vs. Output Level (3)



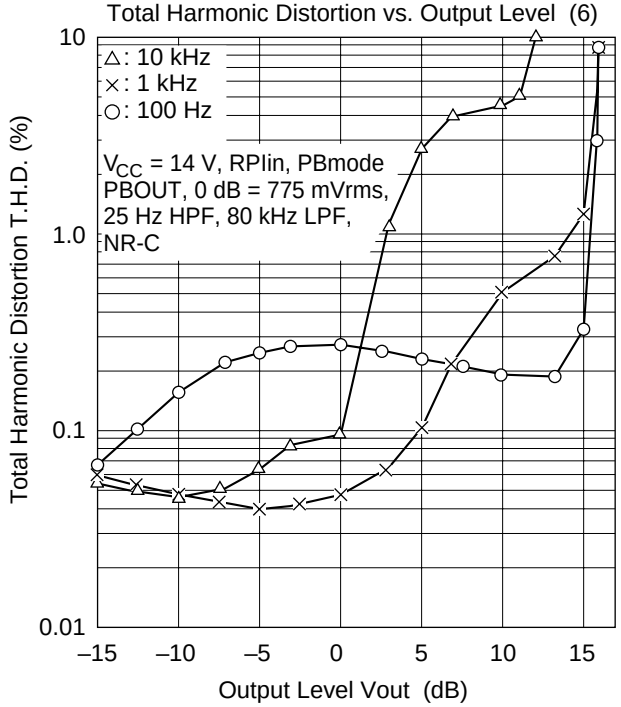
Total Harmonic Distortion vs. Output Level (4)



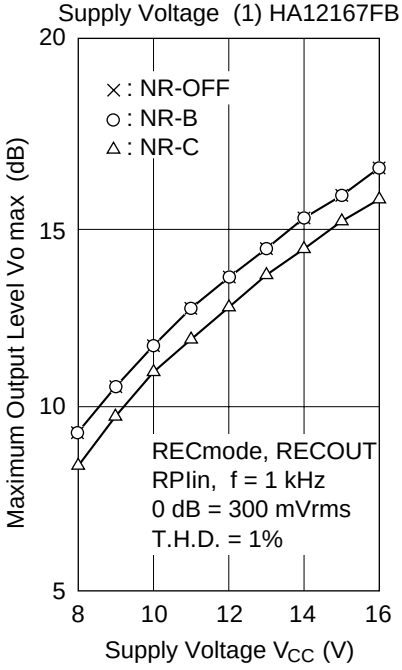
Total Harmonic Distortion vs. Output Level (5)



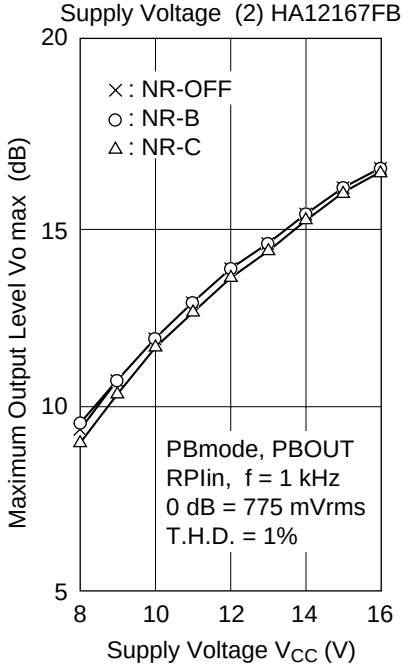
Total Harmonic Distortion vs. Output Level (6)



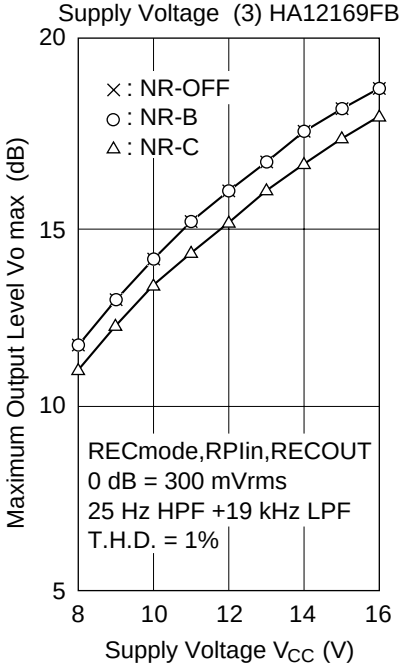
Maximum Output Level vs. Supply Voltage (1) HA12167FB



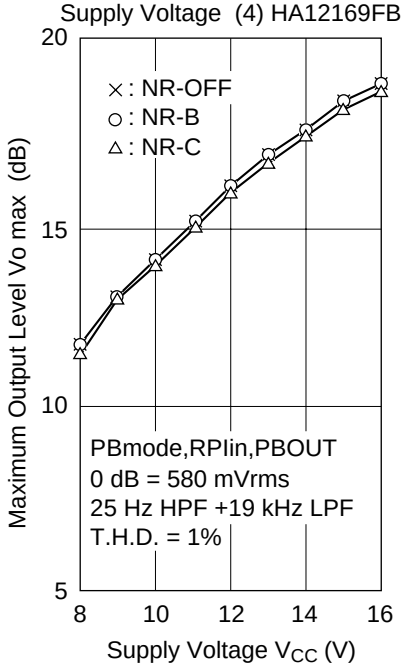
Maximum Output Level vs. Supply Voltage (2) HA12167FB



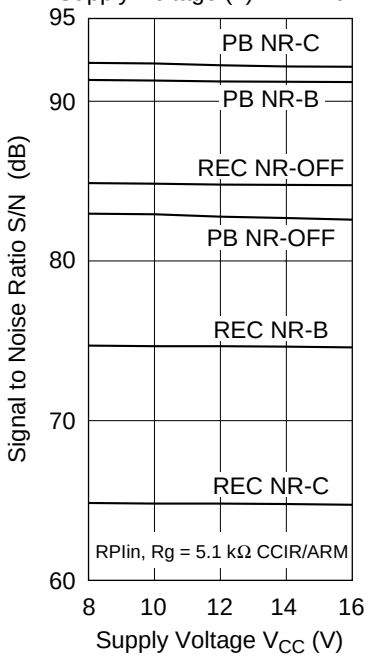
Maximum Output Level vs. Supply Voltage (3) HA12169FB



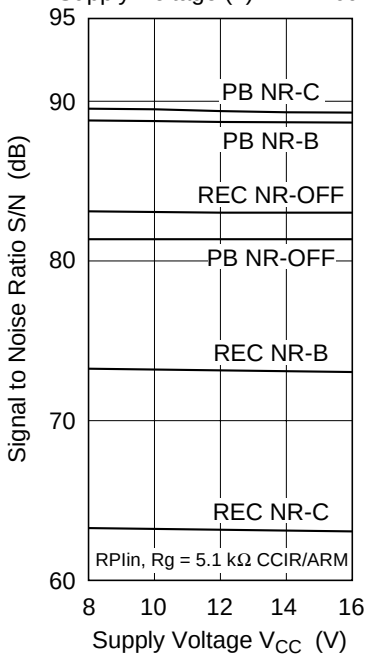
Maximum Output Level vs. Supply Voltage (4) HA12169FB



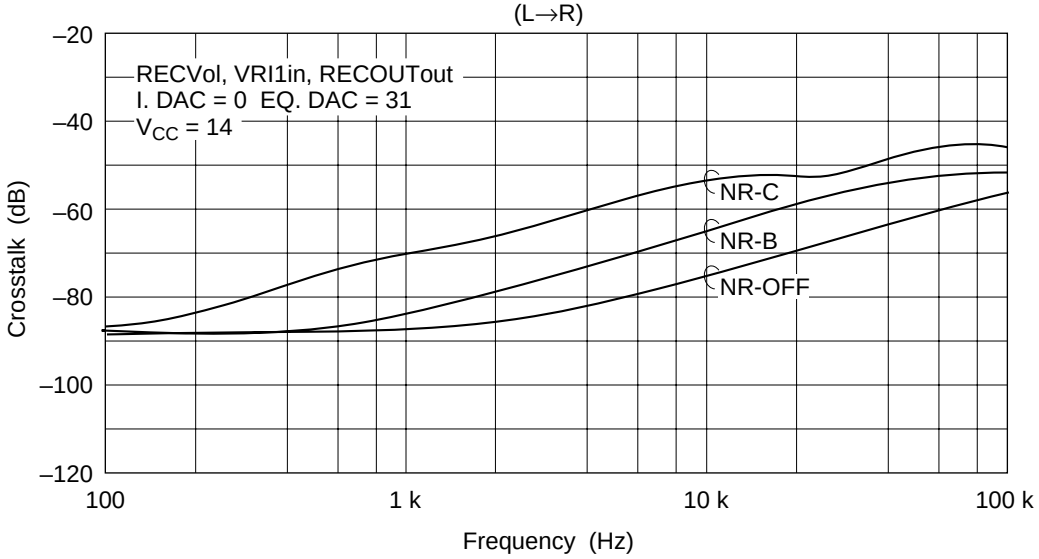
Signal to Noise Ratio vs. Supply Voltage (1) HA12167FB



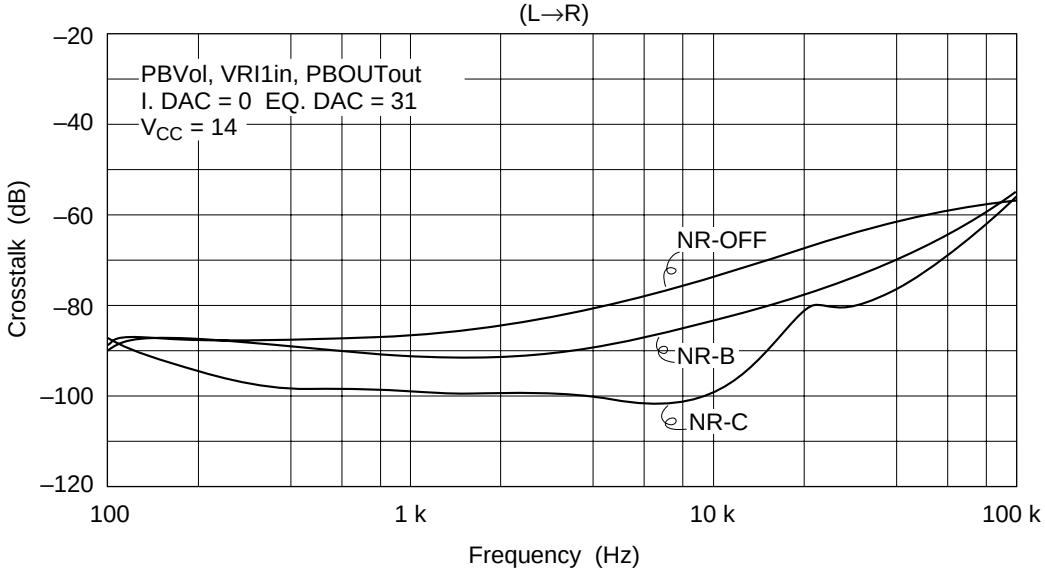
Signal to Noise Ratio vs. Supply Voltage (2) HA12169FB



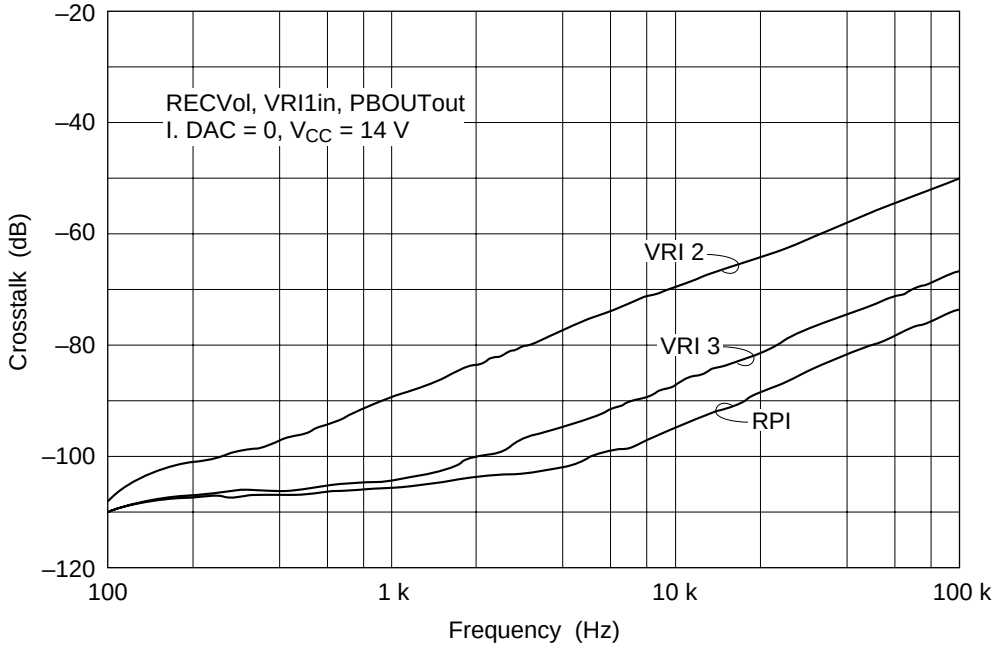
Crosstalk vs. Frequency (1) (L→R)



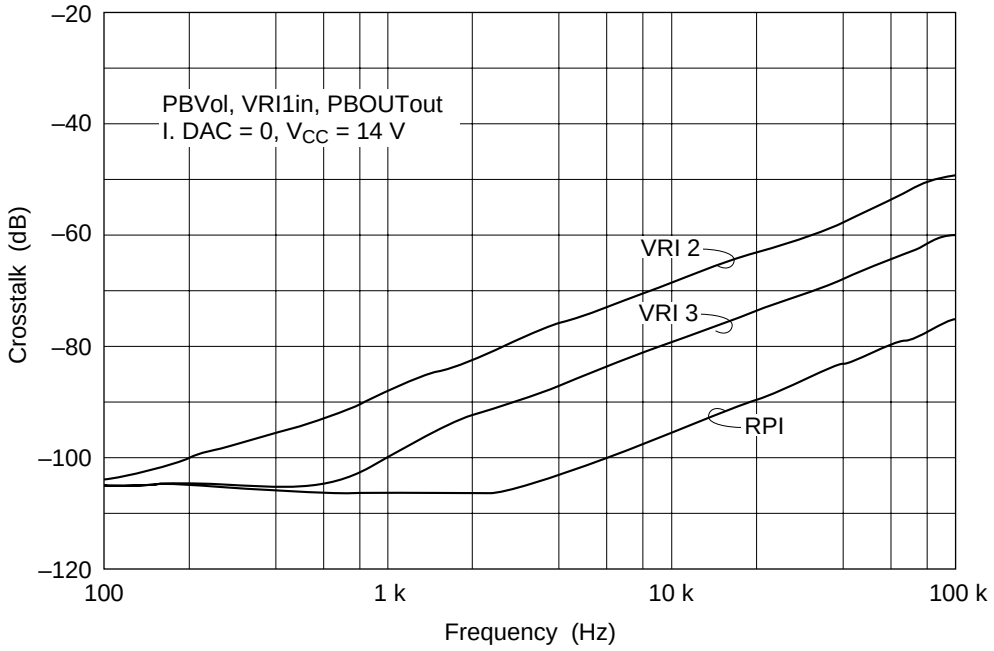
Crosstalk vs. Frequency (2)
(L→R)



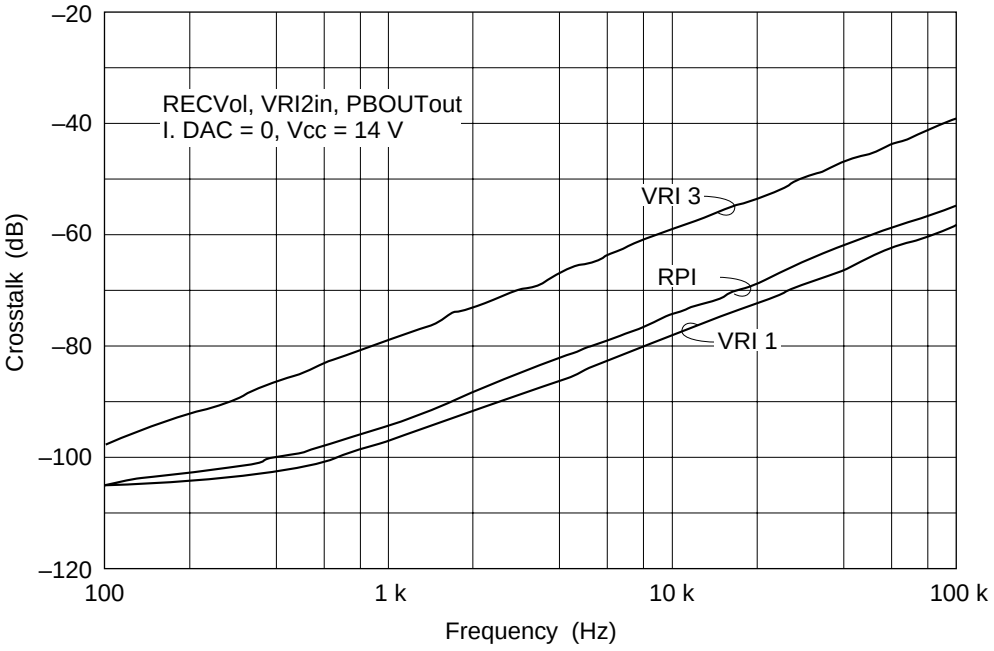
Crosstalk vs. Frequency (3)
(VRI1 ⟶ VRI2, VRI3, RPI)



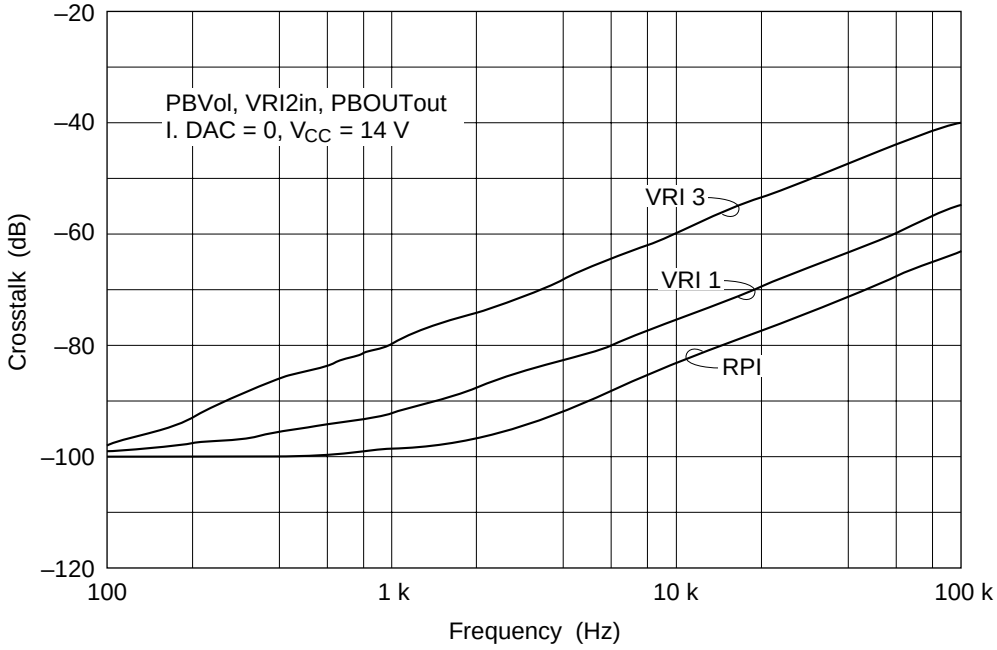
Crosstalk vs. Frequency (4)
(VRI1 → VRI2, VRI3, RPI)



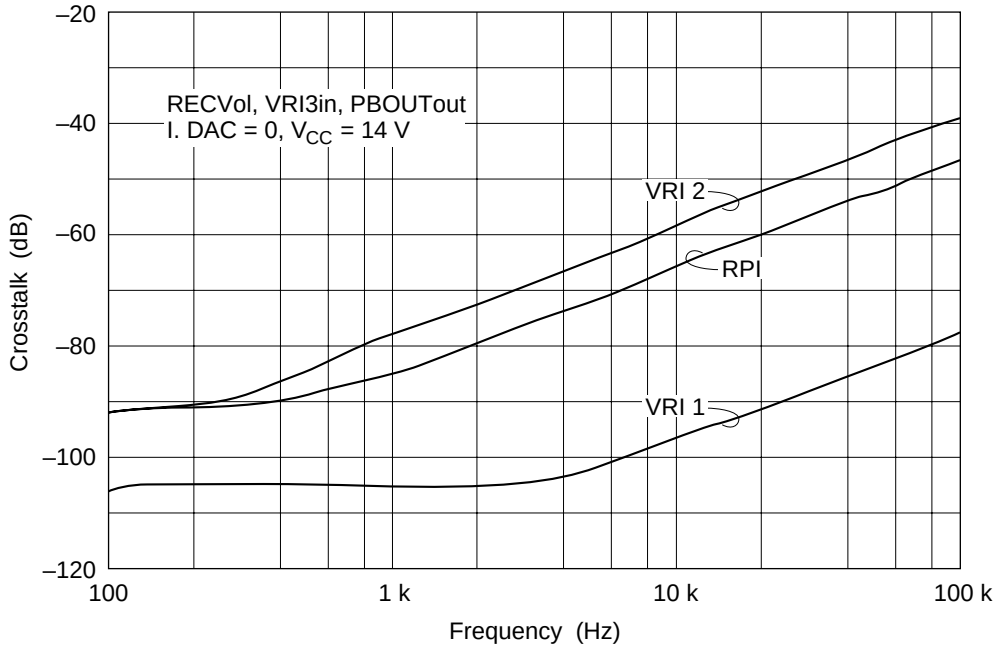
Crosstalk vs. Frequency (5)
(VRI2 → VRI1, VRI3, RPI)



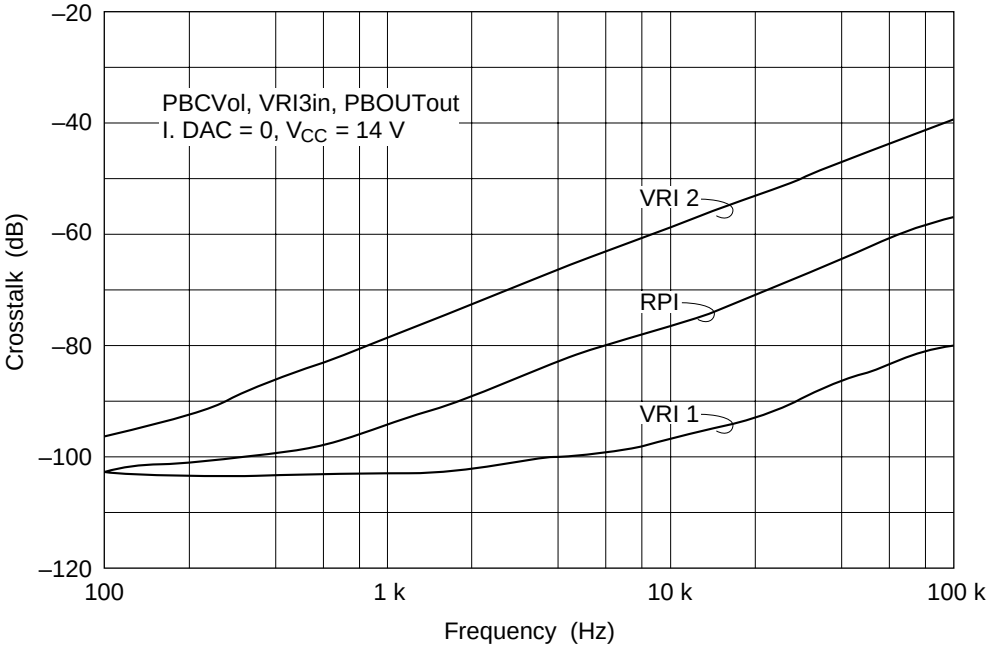
Crosstalk vs. Frequency (6)
(VRI2 → VRI1, VRI3, RPI)



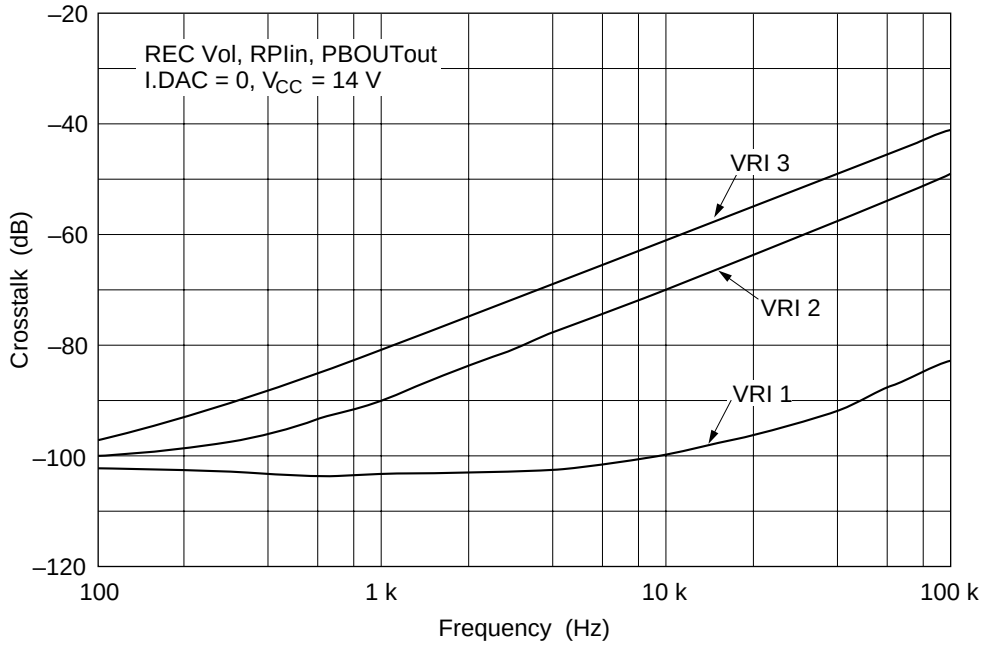
Crosstalk vs. Frequency (7)
(VRI3 → VRI1, VRI2, RPI)



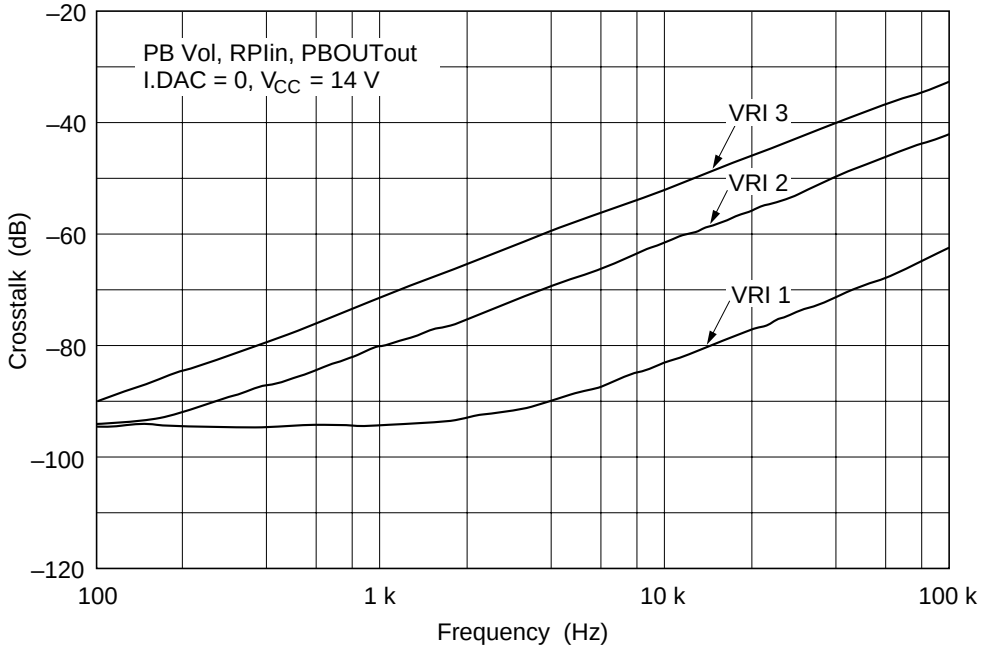
Crosstalk vs. Frequency (8)
(VRI3 → VRI1, VRI2, RPI)



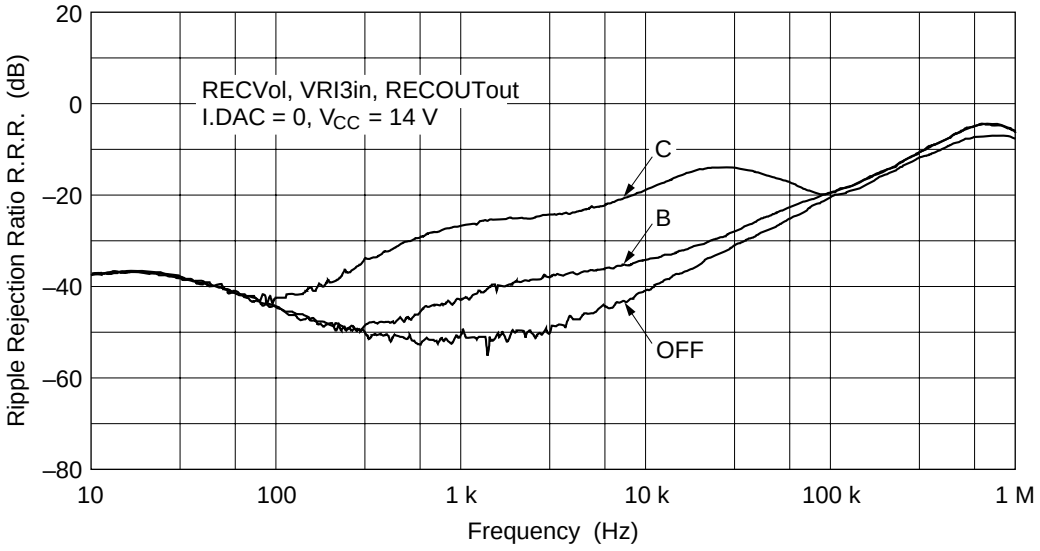
Crosstalk vs. Frequency (9)
(RPI → VRI 1, VRI 2, VRI 3)



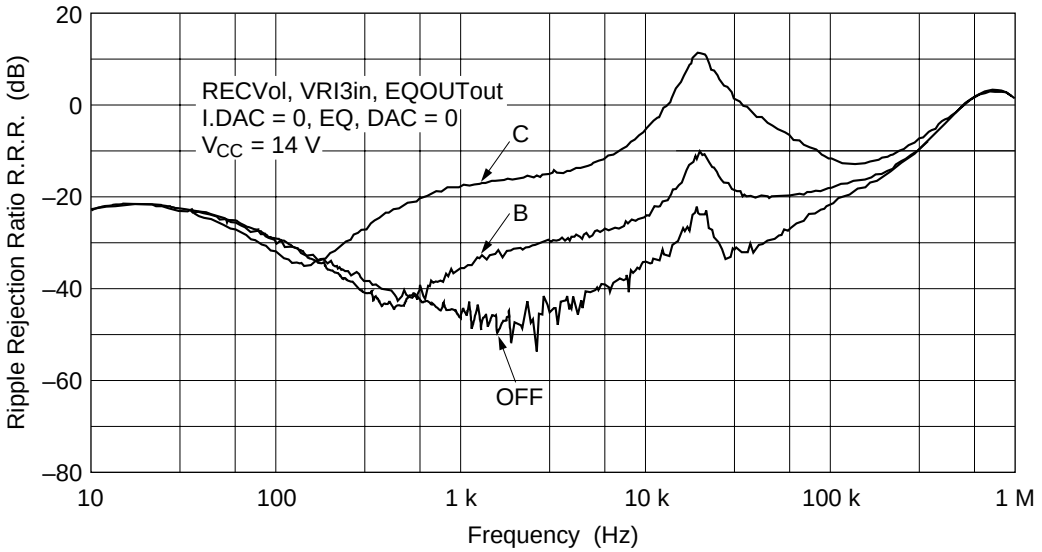
Crosstalk vs. Frequency (10)
(RPI → VRI 1, VRI 2, VRI 3)



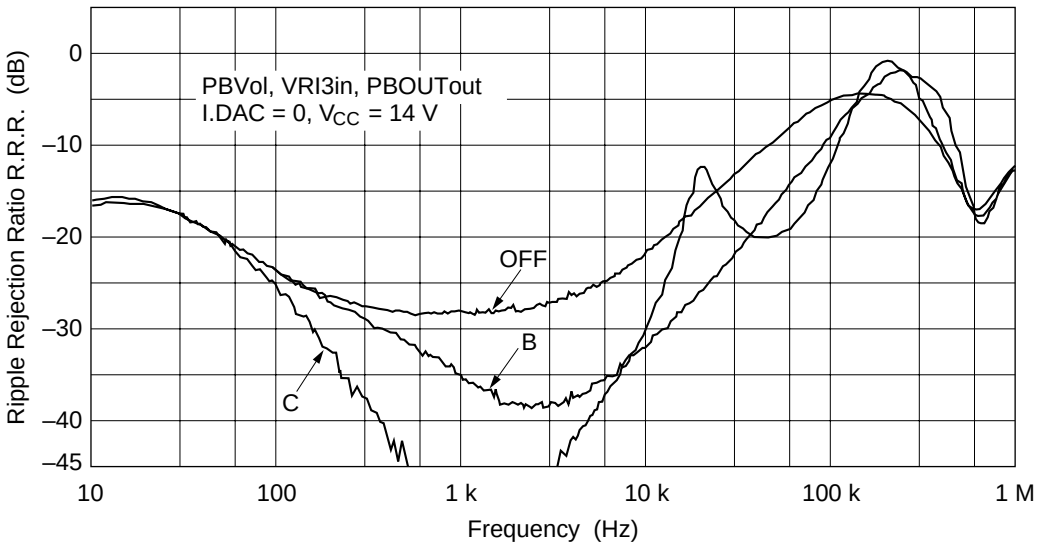
Ripple Rejection Ratio vs. Frequency (1)



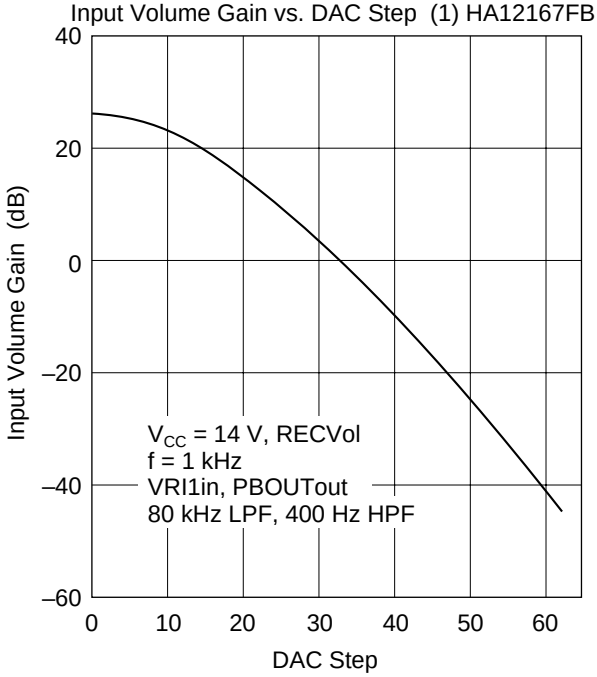
Ripple Rejection Ratio vs. Frequency (2)



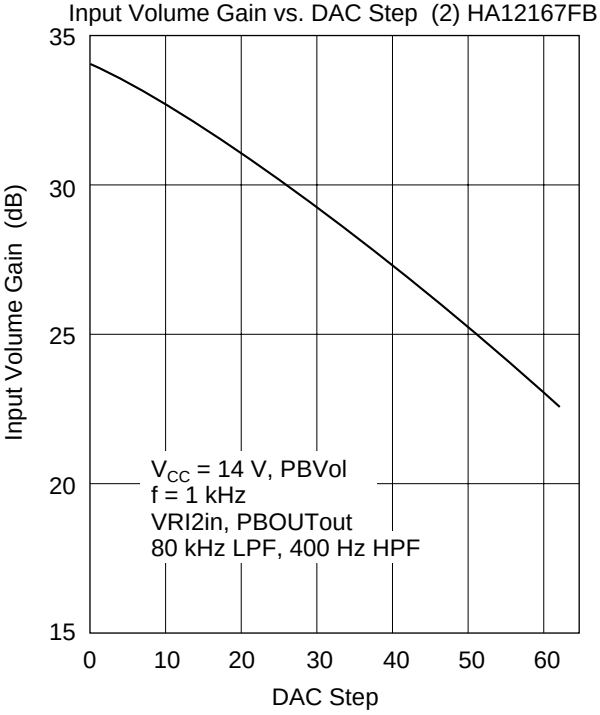
Ripple Rejection Ratio vs. Frequency (3)



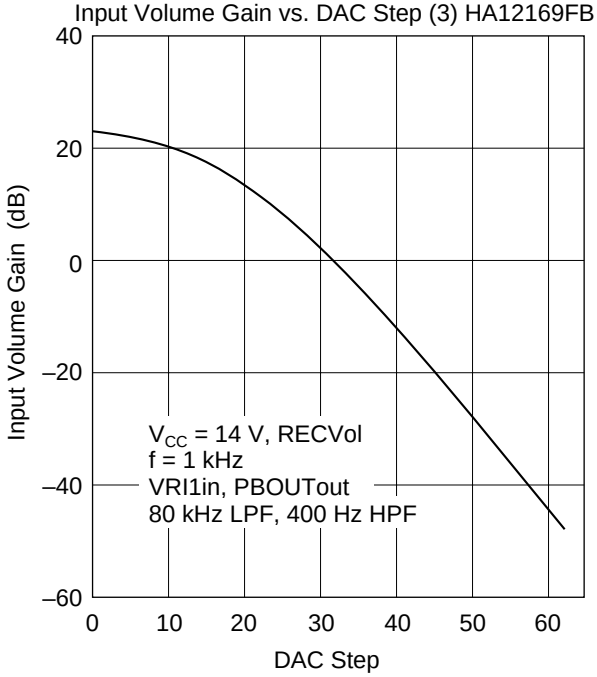
Input Volume Gain vs. DAC Step (1) HA12167FB



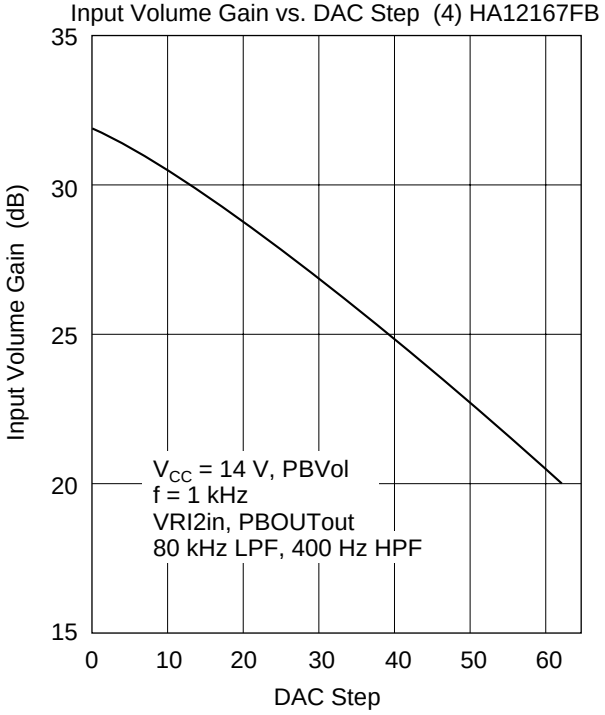
Input Volume Gain vs. DAC Step (2) HA12167FB



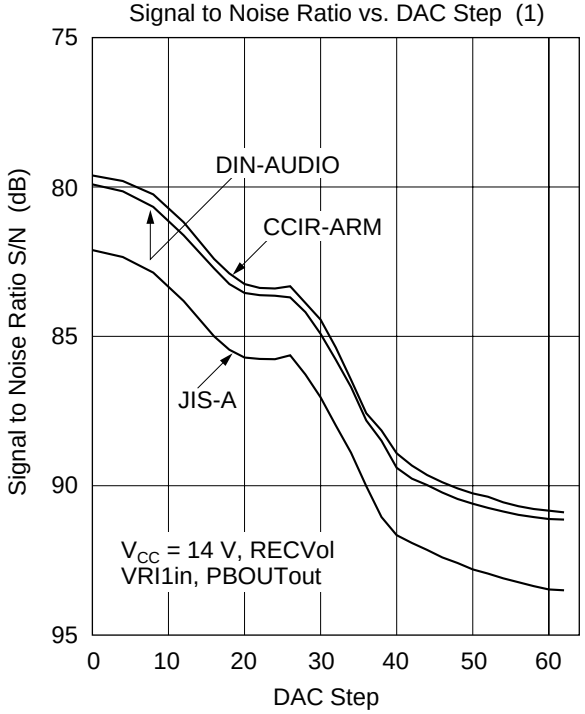
Input Volume Gain vs. DAC Step (3) HA12169FB



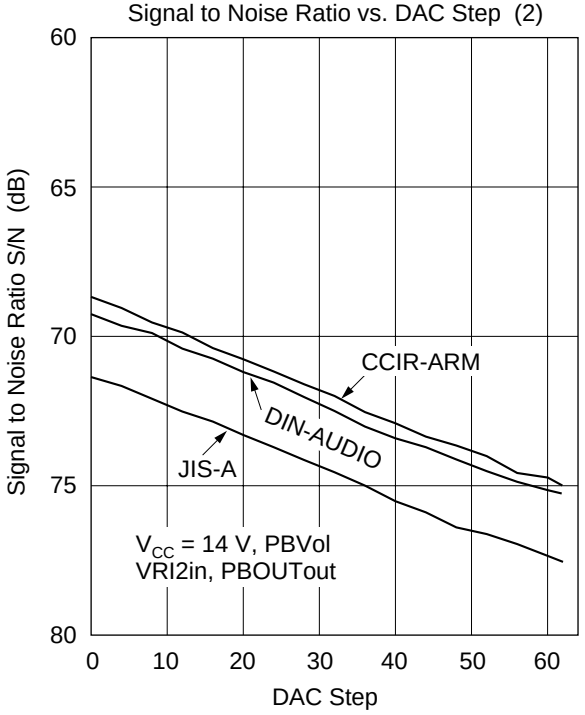
Input Volume Gain vs. DAC Step (4) HA12167FB



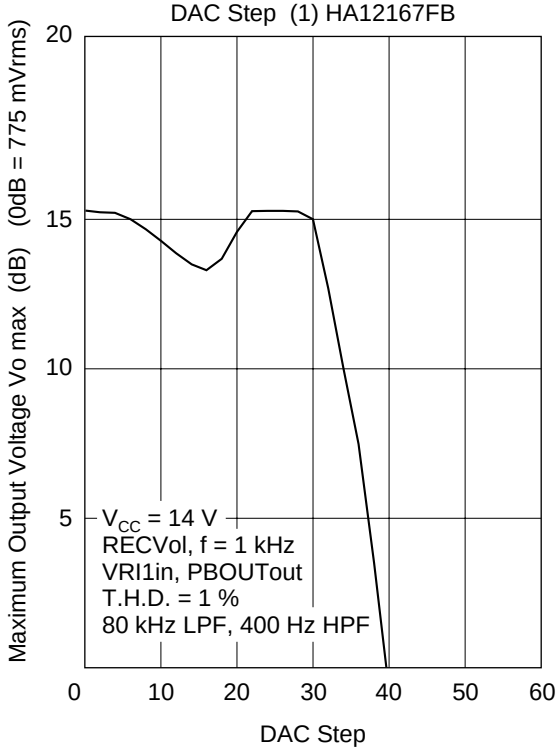
Signal to Noise Ratio vs. DAC Step (1)



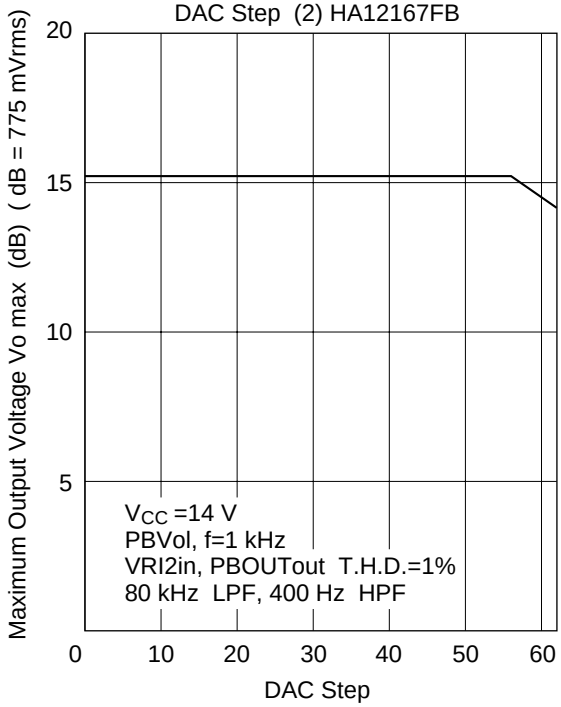
Signal to Noise Ratio vs. DAC Step (2)



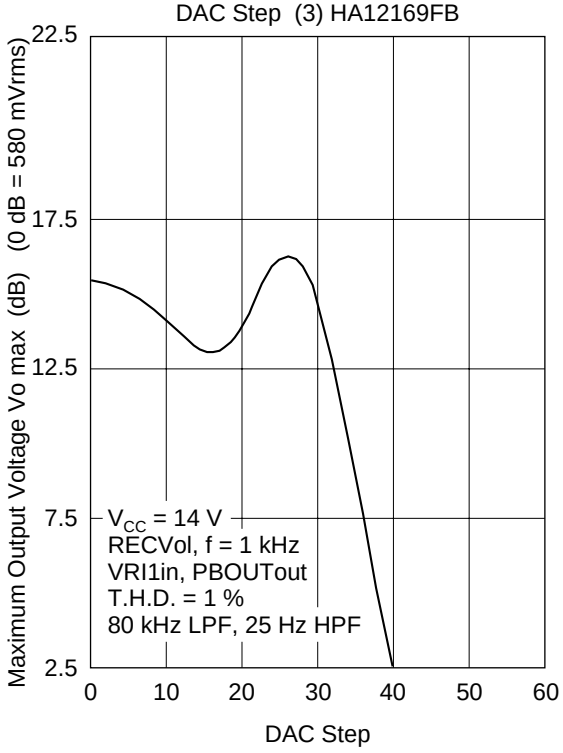
Maximum Output Voltage vs.
DAC Step (1) HA12167FB



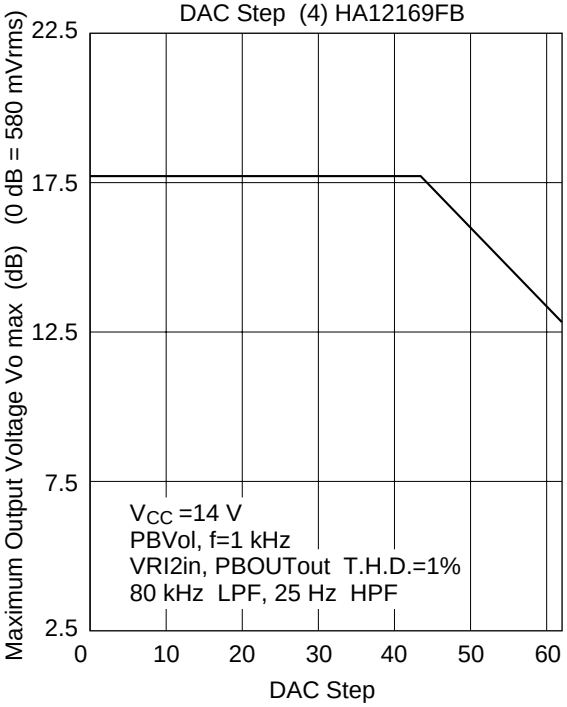
Maximum Output Voltage vs.
DAC Step (2) HA12167FB



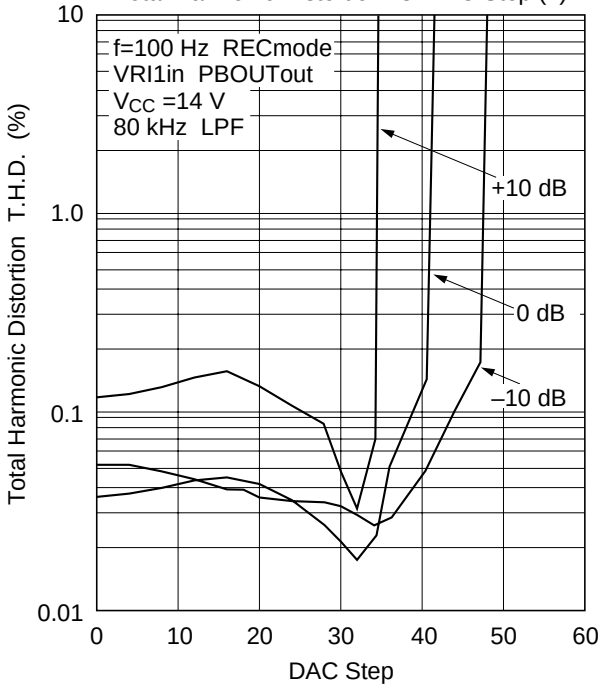
Maximum Output Voltage vs.
DAC Step (3) HA12169FB



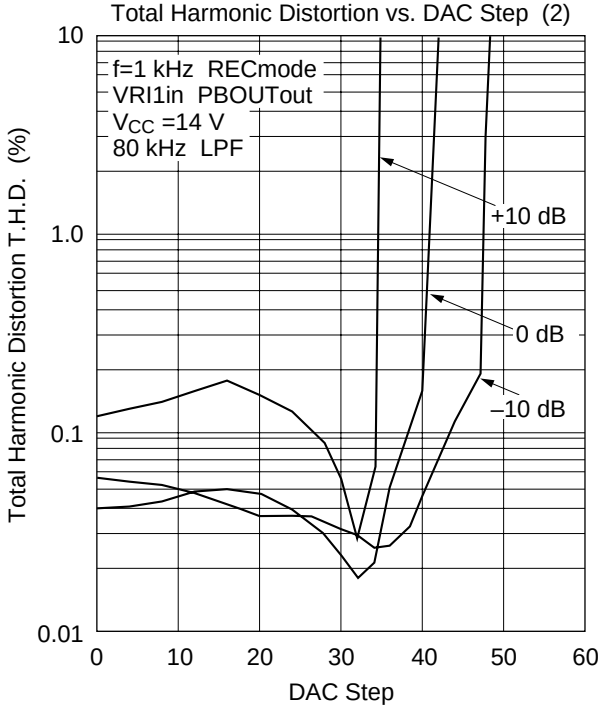
Maximum Output Voltage vs.
DAC Step (4) HA12169FB



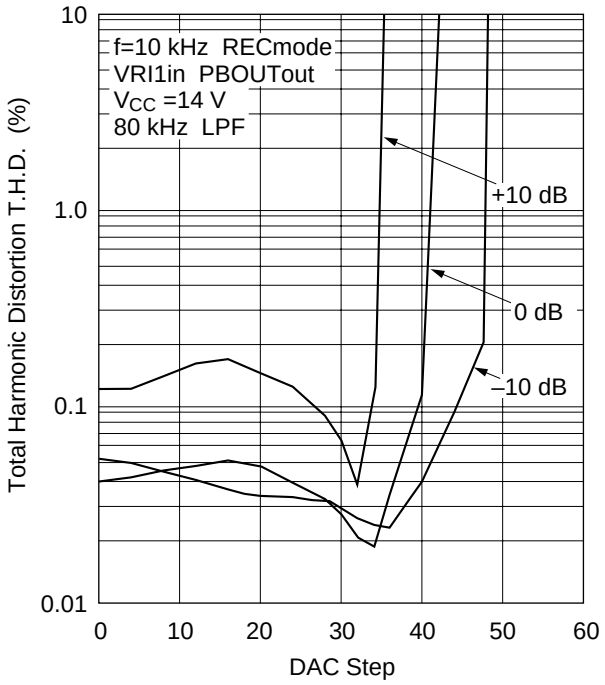
Total Harmonic Distortion vs. DAC Step (1)



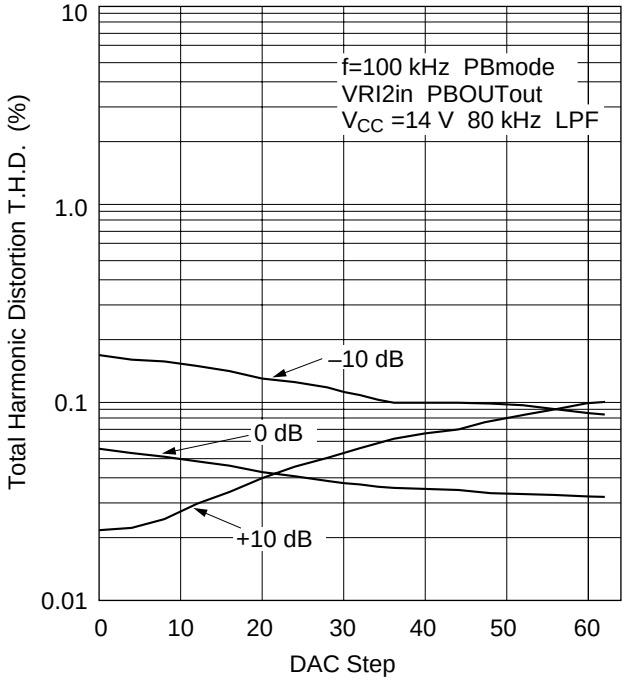
Total Harmonic Distortion vs. DAC Step (2)



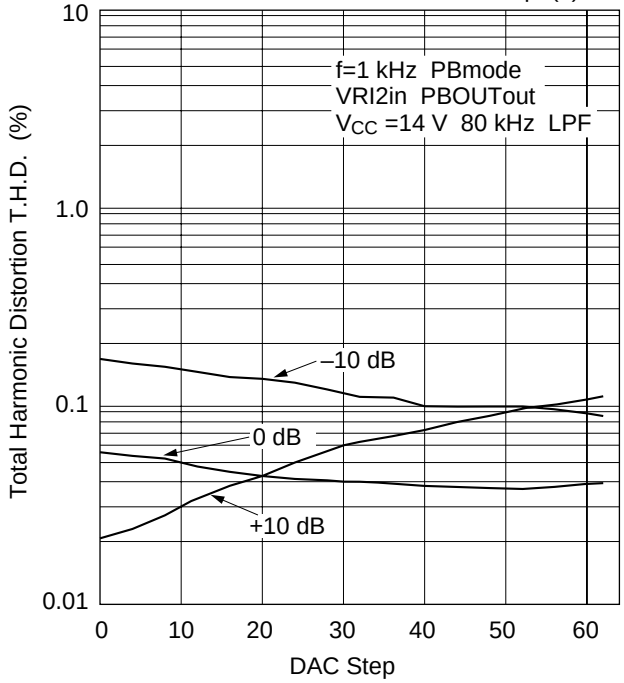
Total Harmonic Distortion vs. DAC Step (3)



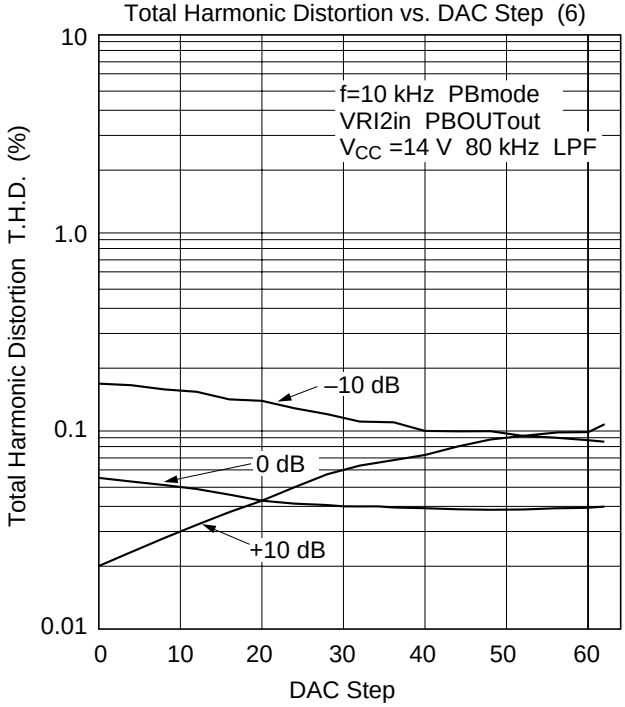
Total Harmonic Distortion vs. DAC Step (4)



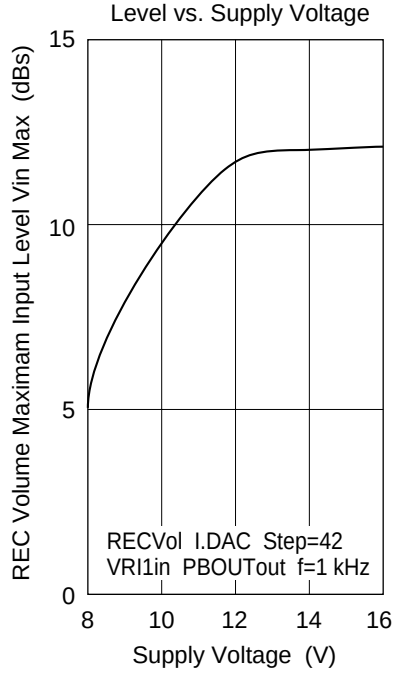
Total Harmonic Distortion vs. DAC Step (5)



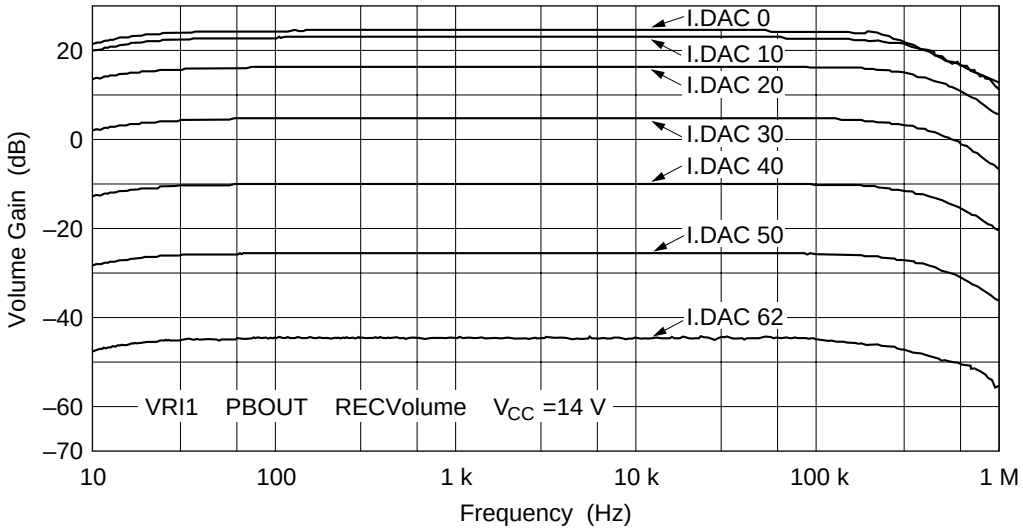
Total Harmonic Distortion vs. DAC Step (6)



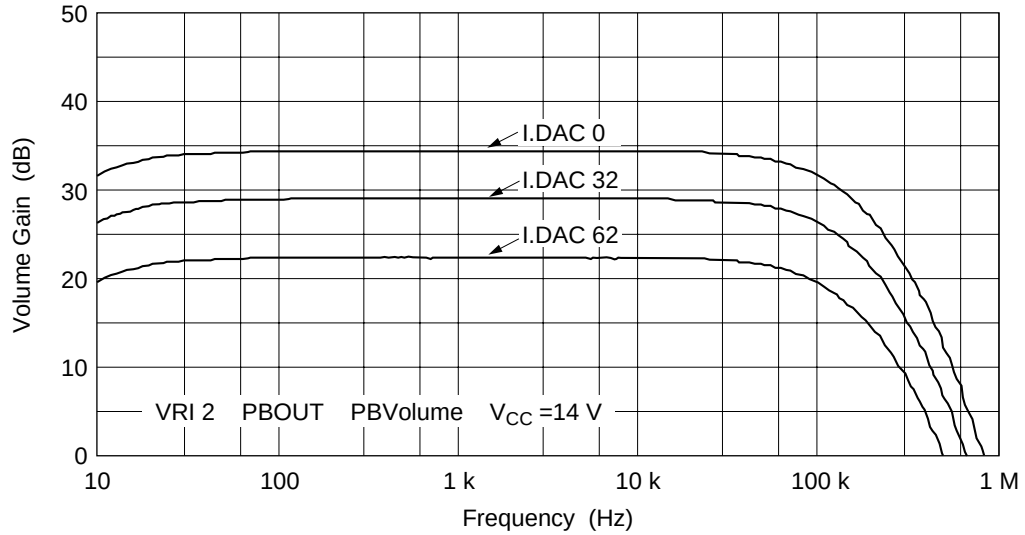
REC Volume Maximam Input Level vs. Supply Voltage



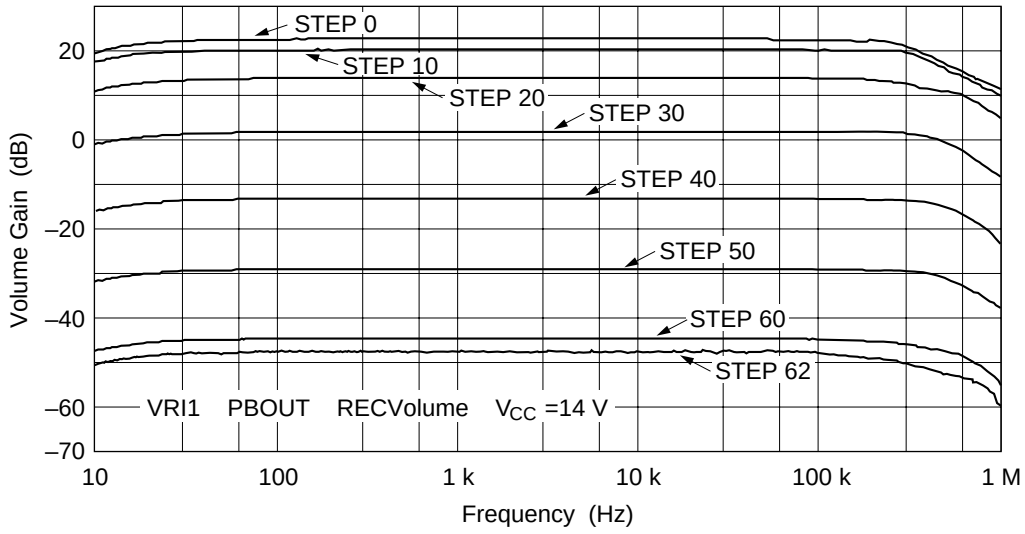
Volume Gain vs. Frequency (1) HA12167FB



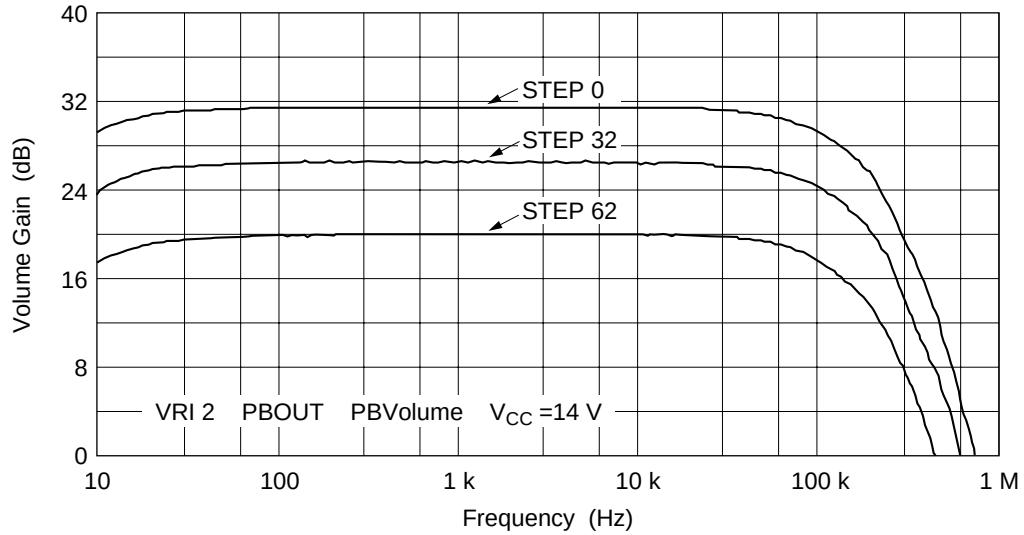
Volume Gain vs. Frequency (2) HA12167FB



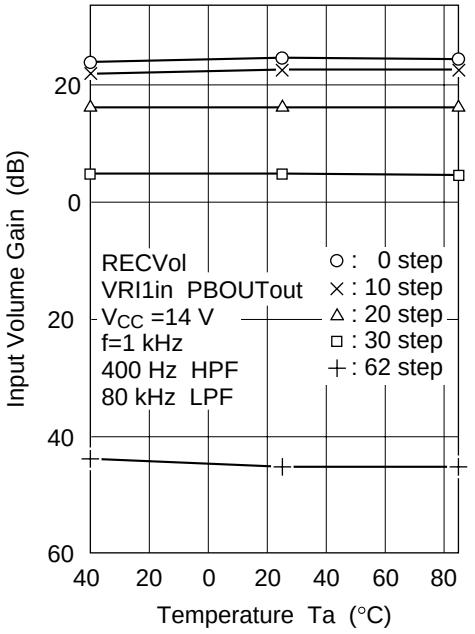
Volume Gain vs. Frequency (3) HA12169FB



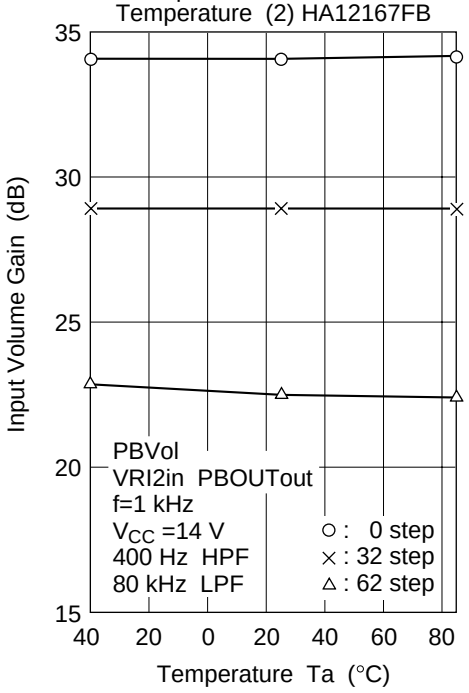
Volume Gain vs. Frequency (4) HA12169FB



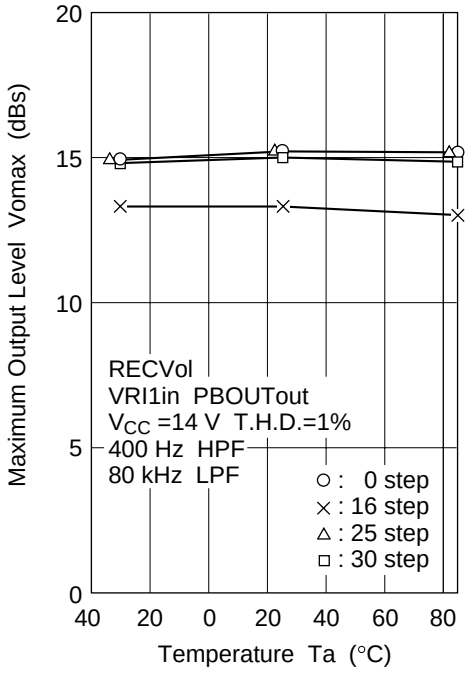
Input Volume Gain vs. Temperature (1) HA12167FB



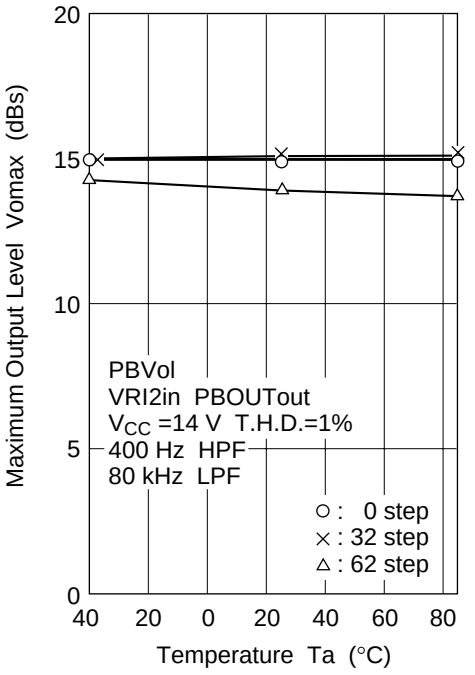
Input Volume Gain vs. Temperature (2) HA12167FB



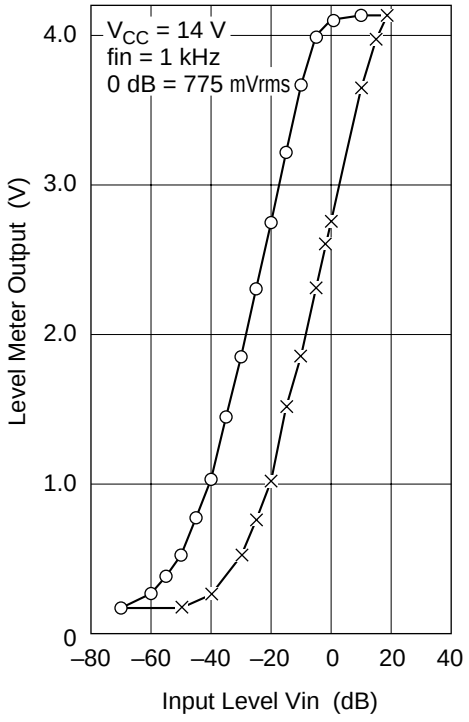
Maximum Output Level vs. Temperature (1)



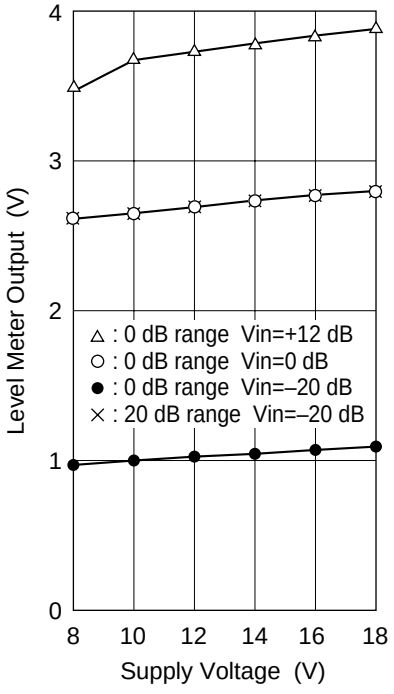
Maximum Output Level vs. Temperature (2)



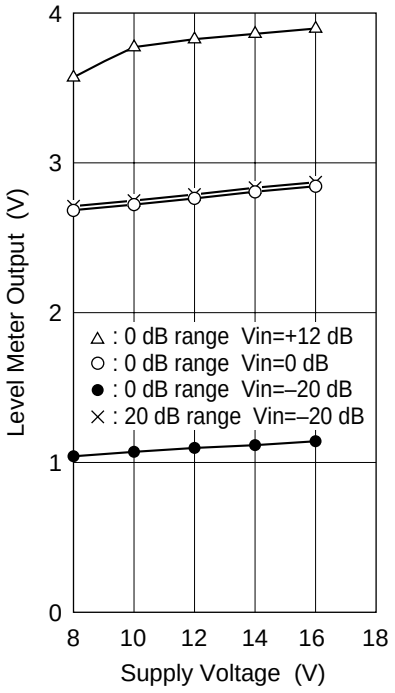
Level Meter Output vs. Input Level



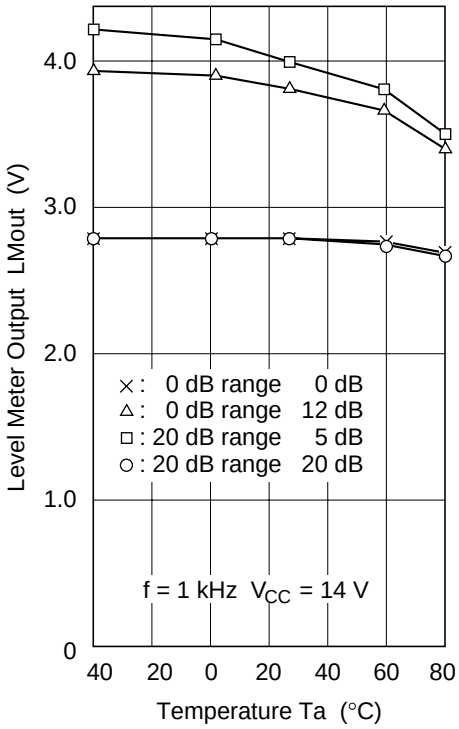
Level Meter Output vs. Supply Voltage (1) HA12167FB



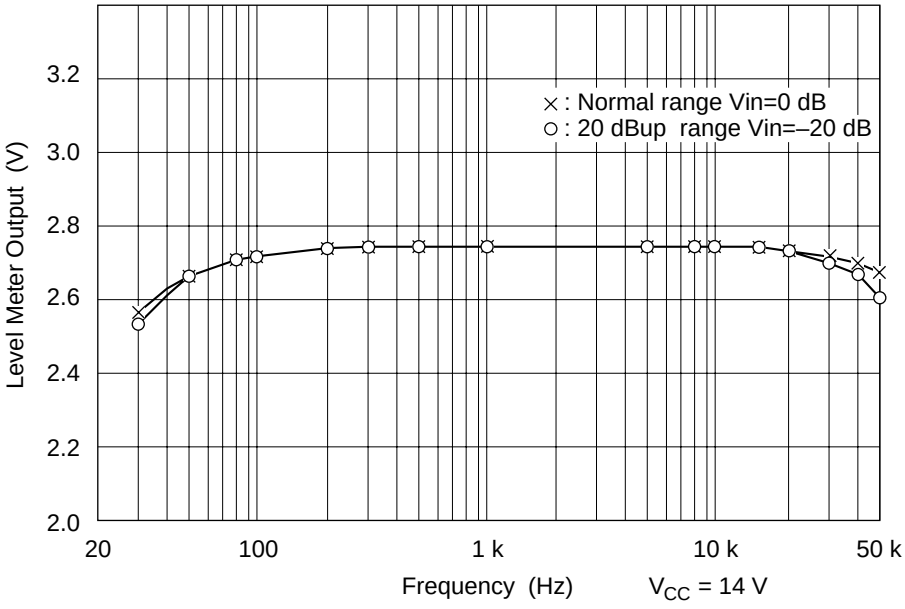
Level Meter Output vs.
Supply Voltage (2) HA12169FB



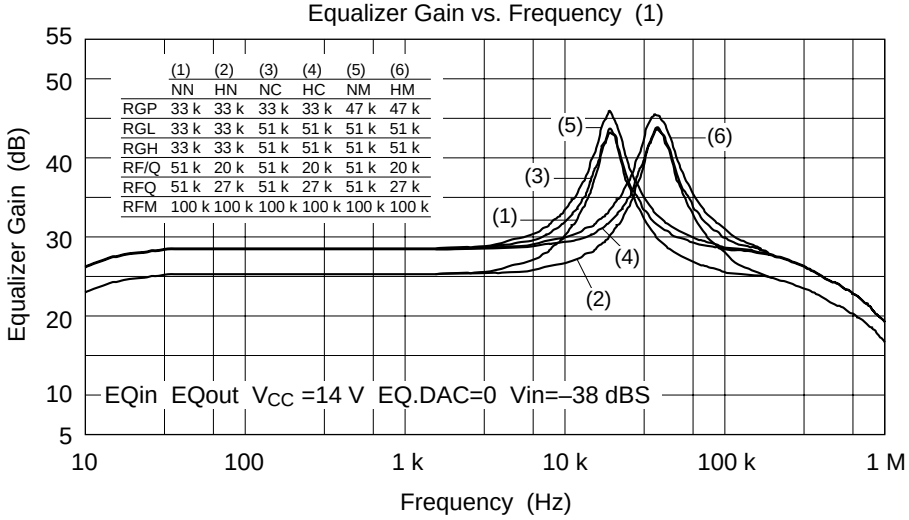
Level Meter Output vs. Temperature



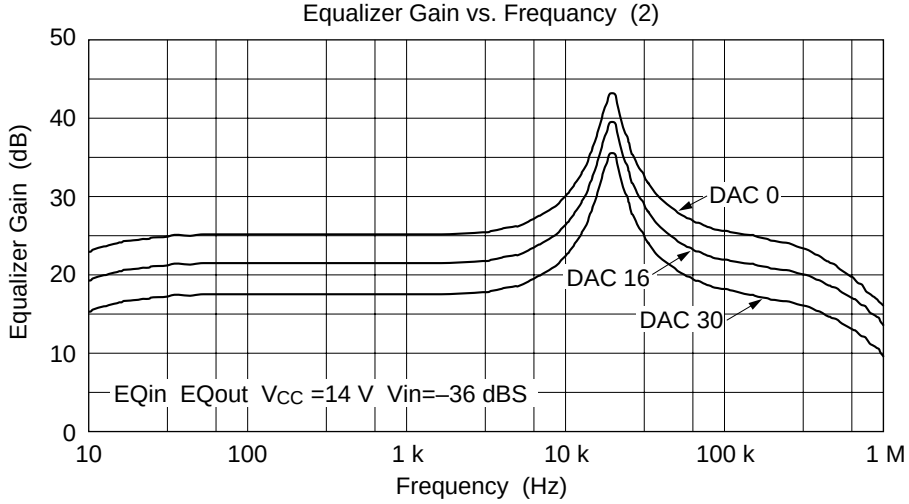
Level Meter Output vs. Frequency



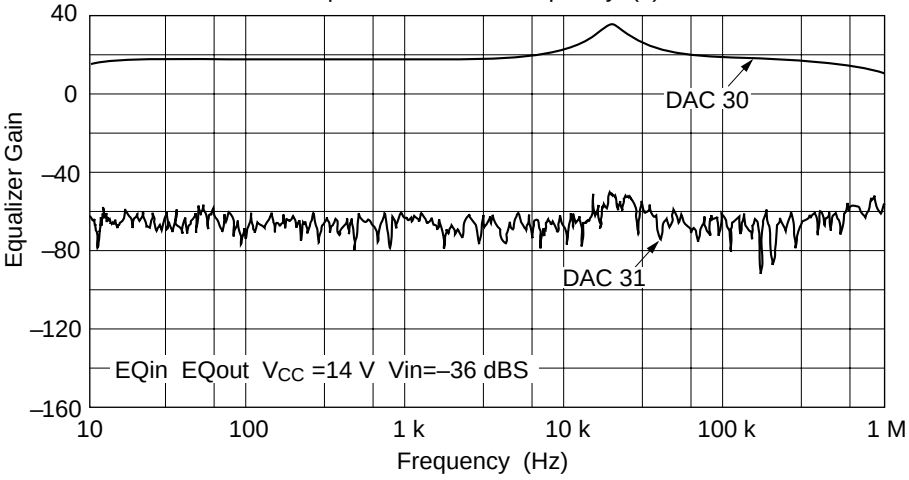
Equalizer Gain vs. Frequency (1)



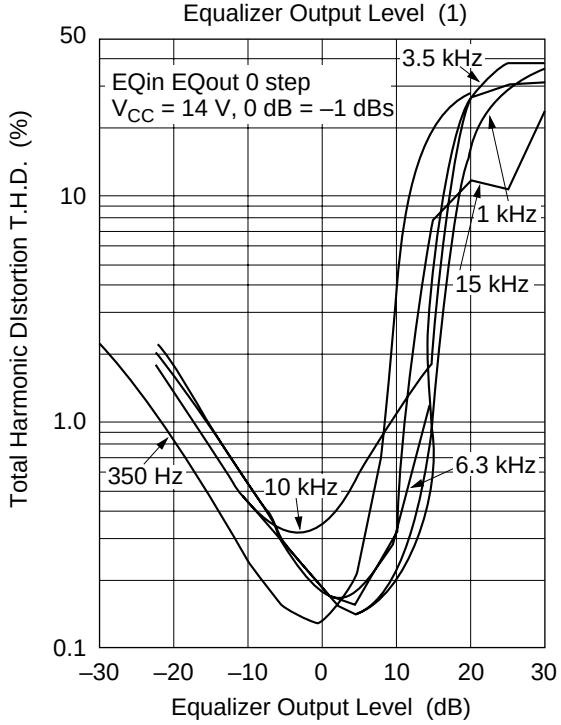
Equalizer Gain vs. Frequancy (2)



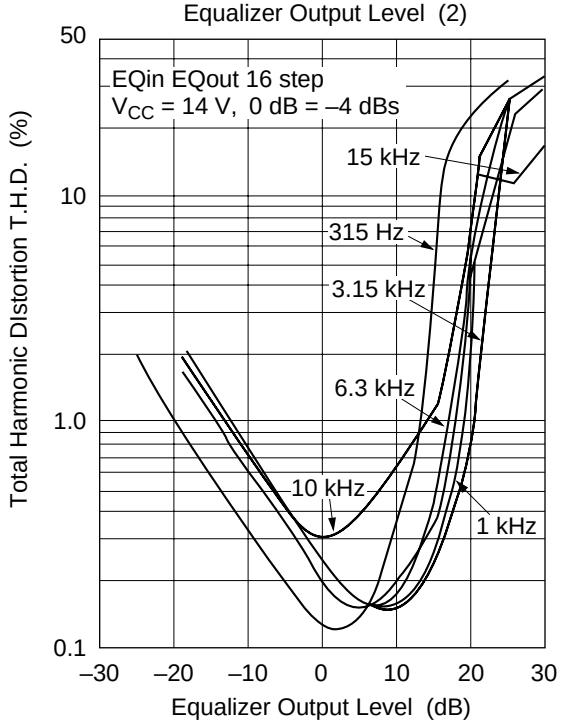
Equalizer Gain vs. Frequancy (3)



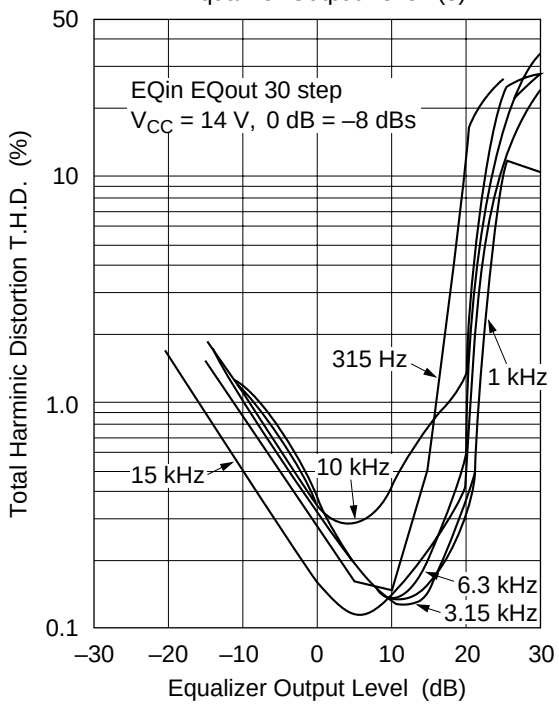
Total Harmonic Distortion vs.
Equalizer Output Level (1)



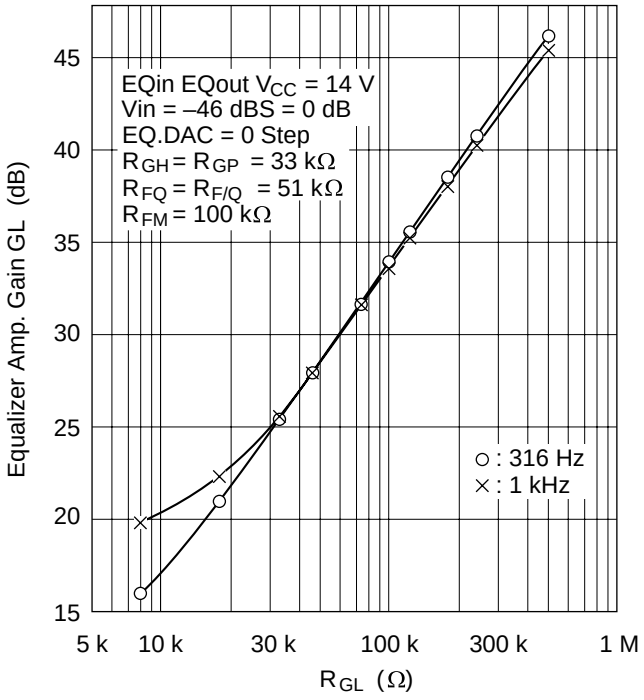
Total Harmonic Distortion vs.
Equalizer Output Level (2)



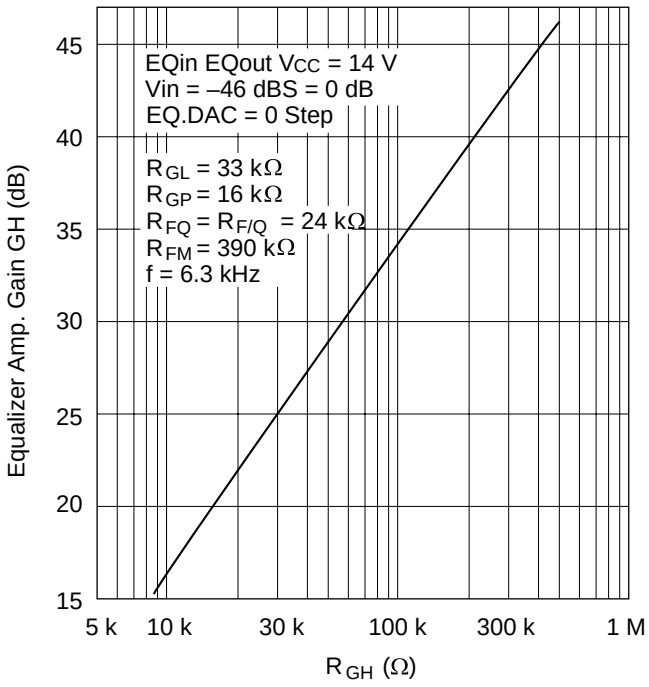
Total Harmonic Distortion vs.
Equalizer Output Level (3)



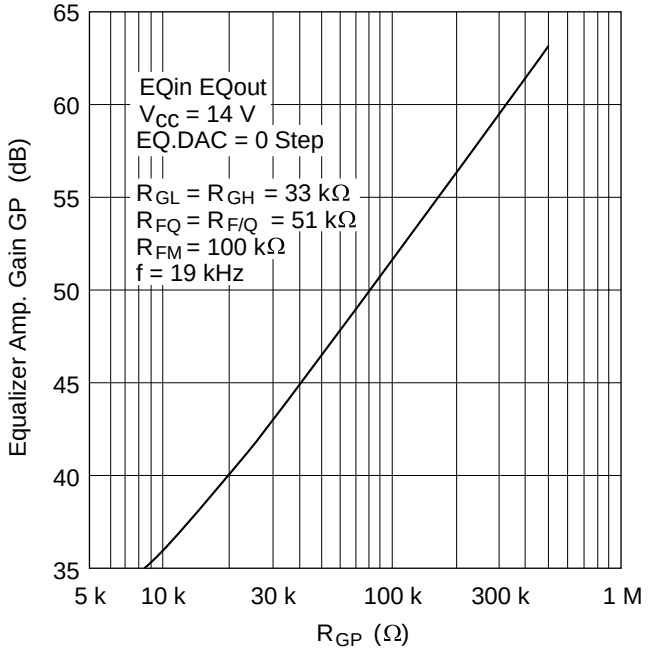
Equalizer Amp. Gain vs. R_{GL}

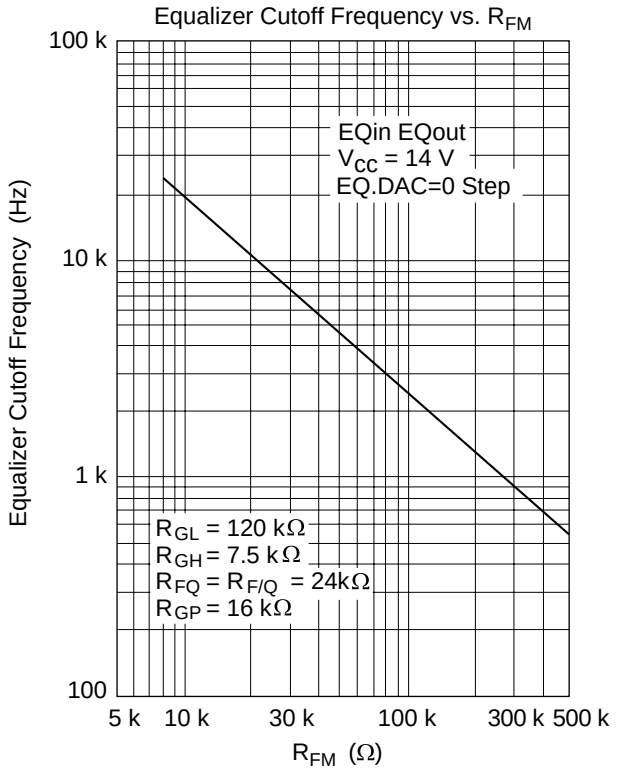


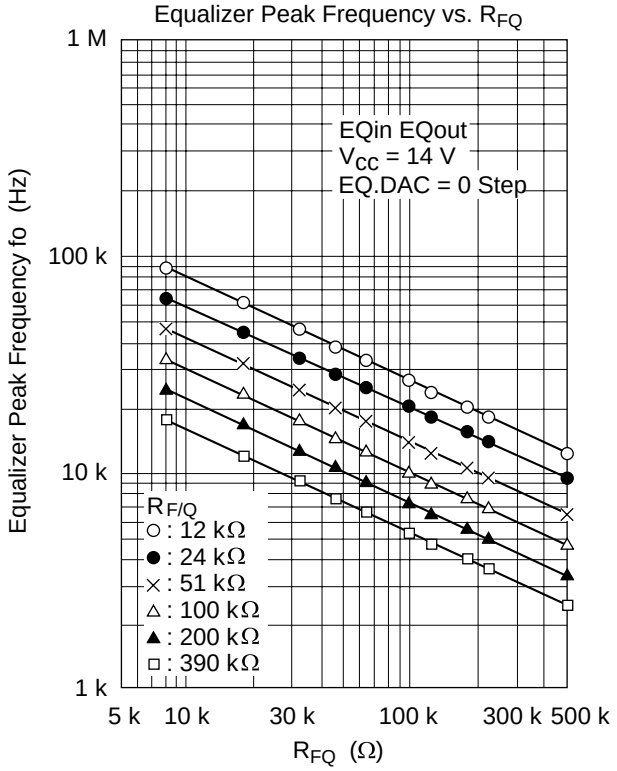
Equalizer Amp. Gain vs. R_{GH}



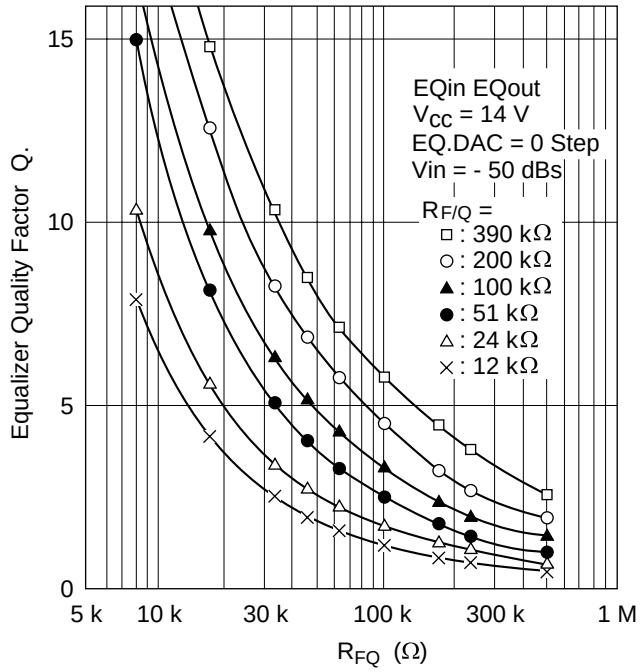
Equalizer Amp. Gain vs. R_{GP}



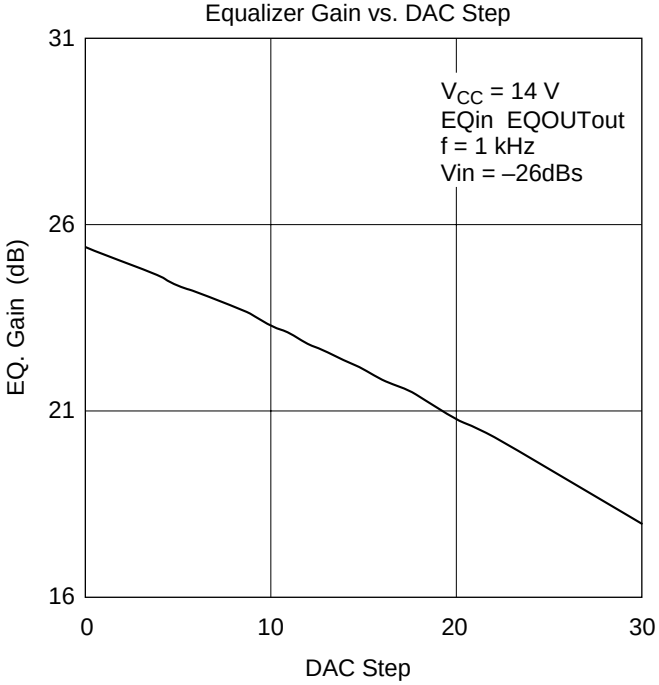

Equalizer Cutoff Frequency vs. R_{FM}
100 k
10 k
1 k
100
Equalizer Cutoff Frequency (Hz)
EQin EQout
V_{CC} = 14 V
EQ.DAC=0 Step
R_{GL} = 120 kΩ
R_{GH} = 7.5 kΩ
R_{FQ} = $R_{F/Q}$ = 24kΩ
R_{GP} = 16 kΩ
5 k
10 k
30 k
100 k
300 k
500 k
R_{FM} (Ω)

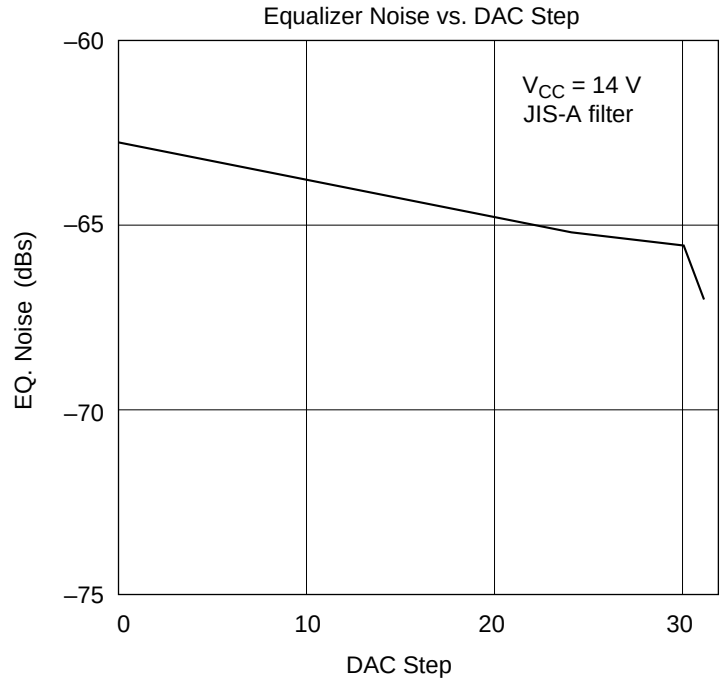

Equalizer Peak Frequency vs. R_{FQ}
1 M
100 k
10 k
1 k
Equalizer Peak Frequency fo (Hz)
EQin EQout
V_{CC} = 14 V
EQ.DAC = 0 Step
$R_{F/Q}$
○ : 12 kΩ
● : 24 kΩ
× : 51 kΩ
△ : 100 kΩ
▲ : 200 kΩ
□ : 390 kΩ
5 k
10 k
30 k
100 k
300 k
500 k
R_{FQ} (Ω)

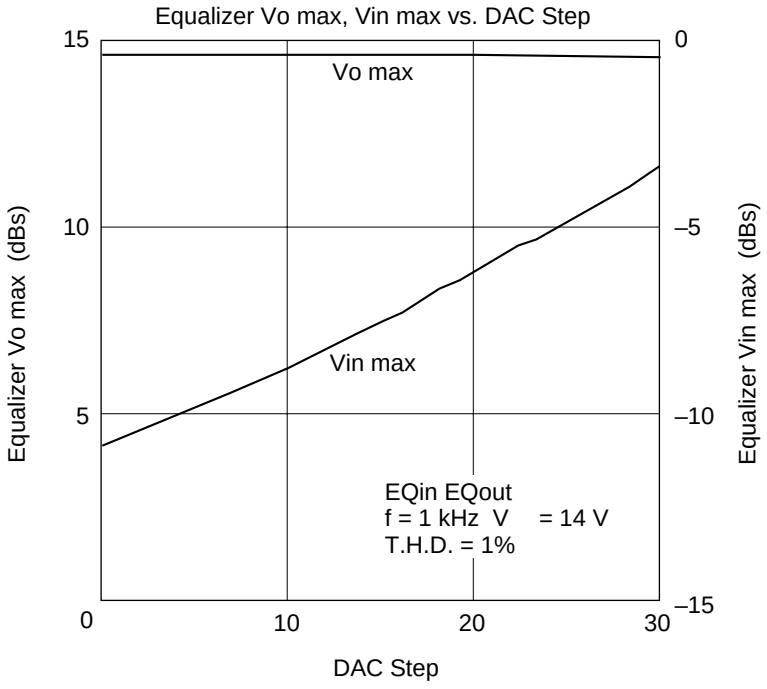
Equalizer Quality Factor vs. R_{FQ}



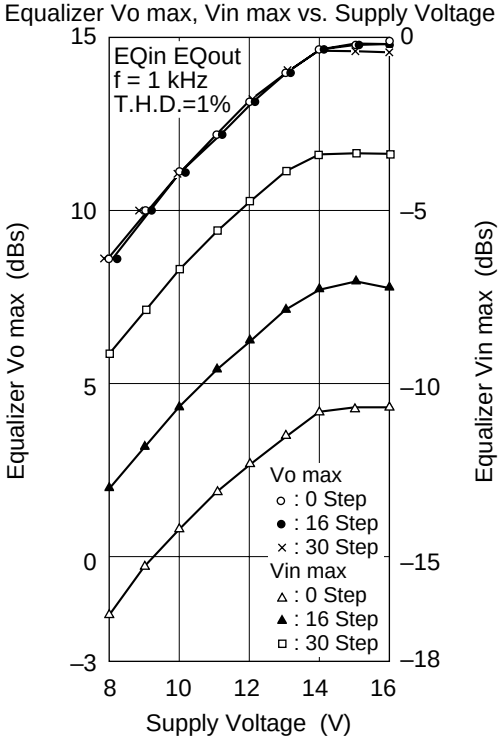
Equalizer Gain vs. DAC Step



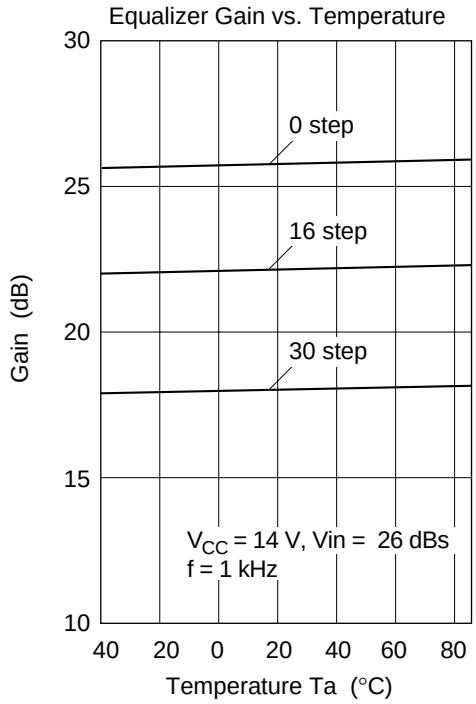

Equalizer Noise vs. DAC Step
–60
–65
–70
–75
EQ. Noise (dBs)
V_{CC} = 14 V
JIS-A filter
0
10
20
30
DAC Step


Equalizer Vo max, Vin max vs. DAC Step
15
10
5
0
Equalizer Vo max (dBs)
Vo max
Vin max
0
–5
–10
–15
Equalizer Vin max (dBs)
EQin EQout
f = 1 kHz V = 14 V
T.H.D. = 1%
0
10
20
30
DAC Step

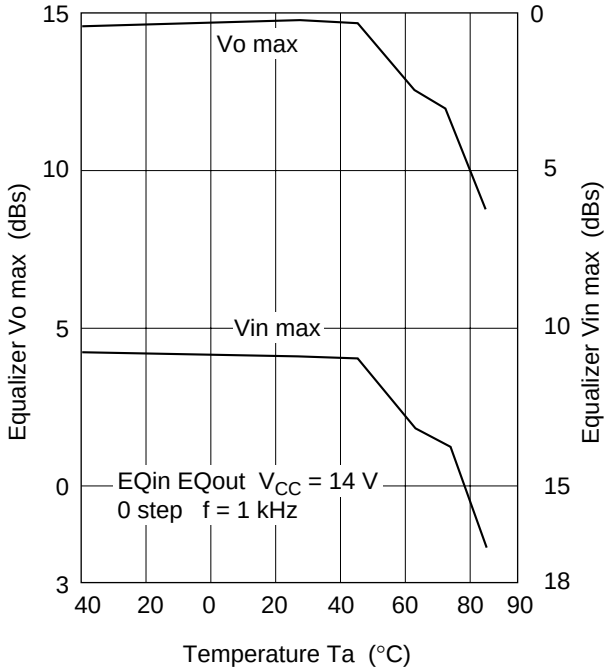
Equalizer Vo max, Vin max vs. Supply Voltage

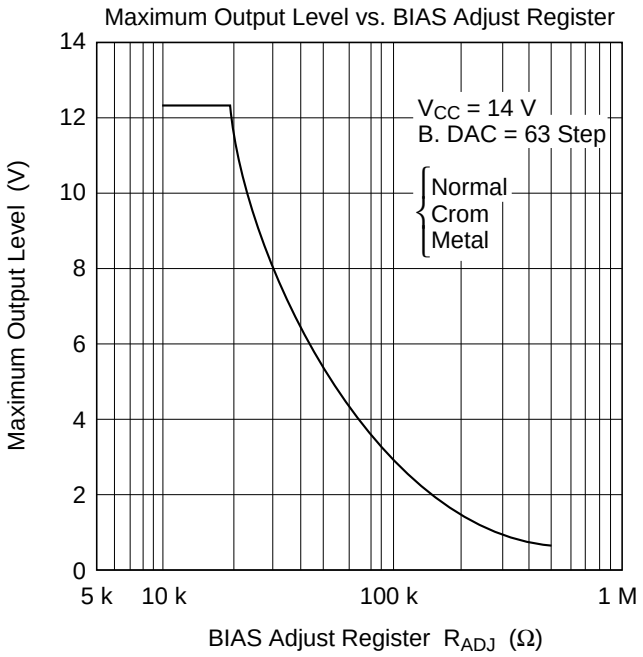


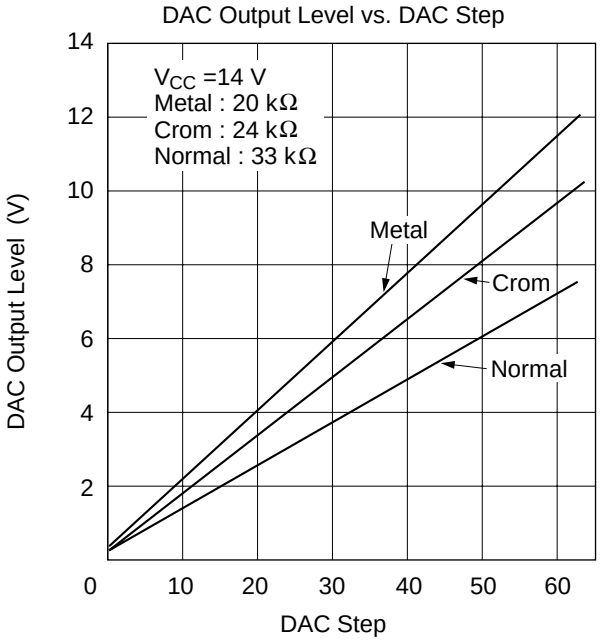
Equalizer Gain vs. Temperature

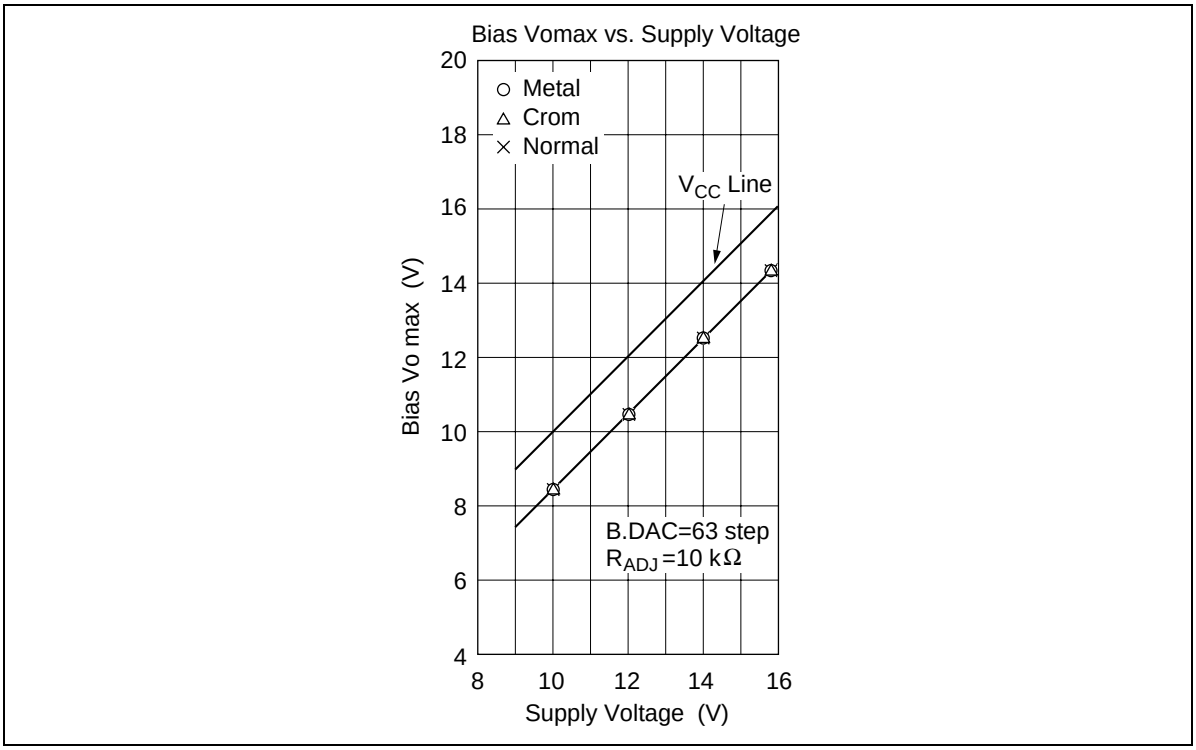


Equalizer Vo max, Vin max vs. Temperature



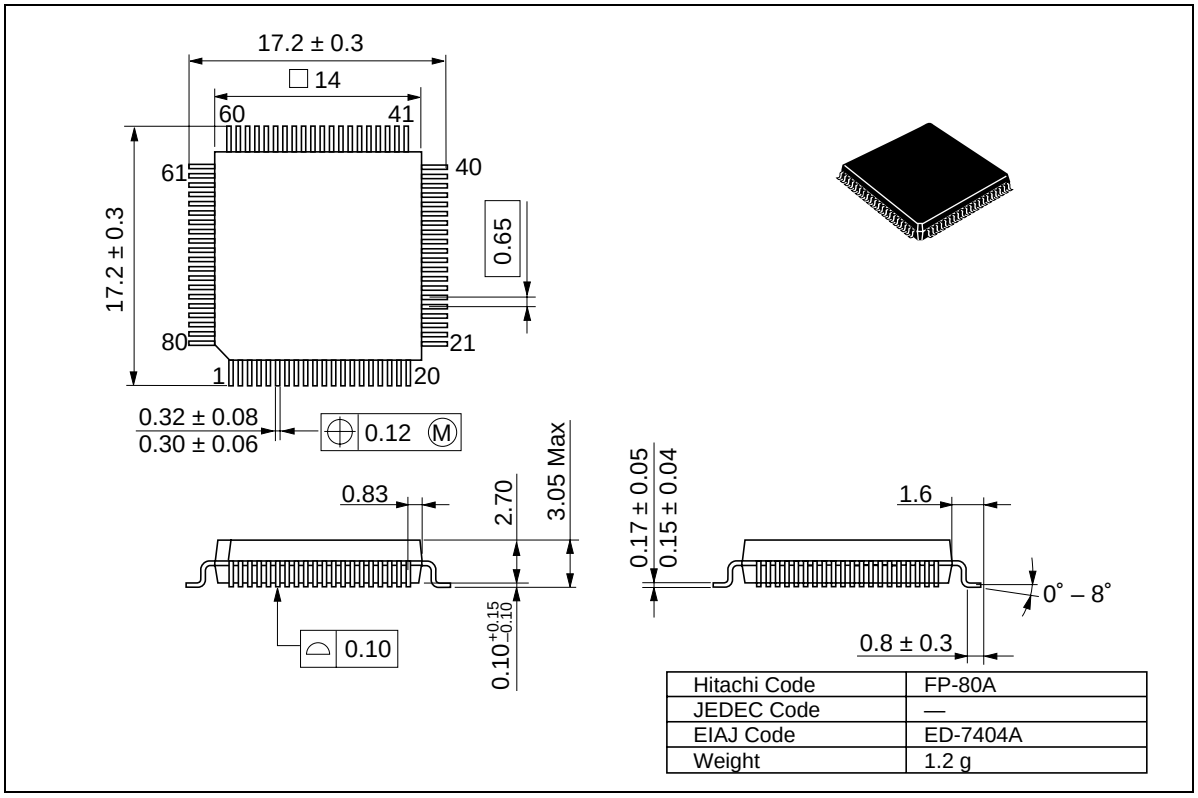

Maximum Output Level vs. BIAS Adjust Register
Maximum Output Level (V)
14
12
10
8
6
4
2
0
5 k
10 k
100 k
1 M
BIAS Adjust Register R_{ADJ} (Ω)
V_{CC} = 14 V
B. DAC = 63 Step
Normal
Crom
Metal


DAC Output Level vs. DAC Step
DAC Output Level (V)
14
12
10
8
6
4
2
0
10
20
30
40
50
60
DAC Step
V_{CC} =14 V
Metal : 20 kΩ
Crom : 24 kΩ
Normal : 33 kΩ
Metal
Crom
Normal


Bias Vomax vs. Supply Voltage
○ Metal
△ Crom
× Normal
V_{CC} Line
B.DAC=63 step
R_{ADJ}=10 kΩ
Bias Vo max (V)
Supply Voltage (V)
20
18
16
14
12
10
8
6
4
8
10
12
14
16

Package Dimensions

Unit: mm



Hitachi Code	FP-80A
JEDEC Code	—
EIAJ Code	ED-7404A
Weight	1.2 g

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