SIEMENS

1-Chip-VPS-Decoder

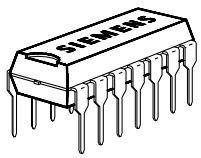
SDA 5642
SDA 5642X

Preliminary Data

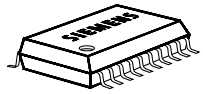
MOS IC

Features

- μC suitable VPS data editing direct from CVBS signal
- n-channel MOS
- Generating of the line synchronous 5-MHz clock for the time base and data clock by means of PLL operation
- Very few external components necessary
- Adaptative data separation
- Frame signal recognition
- Decoder for line 16
- Bi-phase and start code checking
- I^2C-Bus interface
- Operating voltage: 5 V
- Video input signal level 1 … 2.0 V_{pp}



P-DIP-14-1



P-DSO-20-1

Type	Ordering Code	Package
SDA 5642	Q67100-H8547	P-DIP-14-1
SDA 5642X	Q67100-H8637	P-DSO-20-1

Functional Description

The MOS circuit SDA 5642 is used to retrieve the required data for the Video Program System (VPS) service from the data line No. 16 which is included in the CVBS signal. These data are decoded according to the specification given in "Richtlinie ARD/ZDF Nr. 8 R 2".

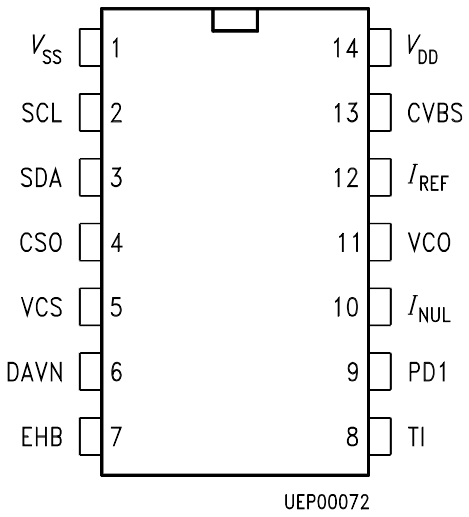
This circuit incorporates the digital functions of the VPS decoder SDA 5640 and the analog functions of the video processor SDA 5232 on one chip. Together with a reduced number of external components this chip is a low cost solution for the VPS detector. The single chip solution can retrieve the data from line 16 of the CVBS signal. These data are decoded, checked for transmission errors and are stored in registers for further processing by a microcontroller. The I^2C-Bus interface is used for communication of a microcontroller with the VPS-decoder.

The recording of programs by a VTR is controlled by the VPS label, a program related datacode which accompanies each TV program during its transmission.

As a result the circuit prevents errors in the recording, as can be seen when using the timer control, when programs are delayed, or are longer than expected.

Pin Configuration
(top view)

P-DIP-14-1



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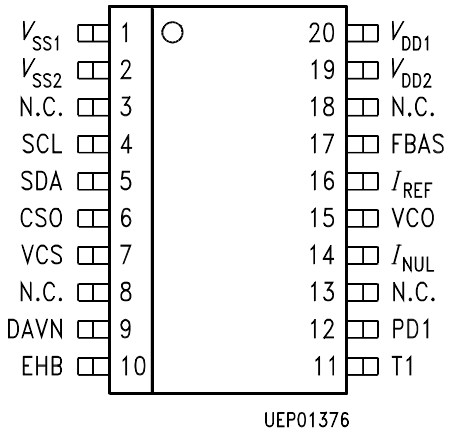
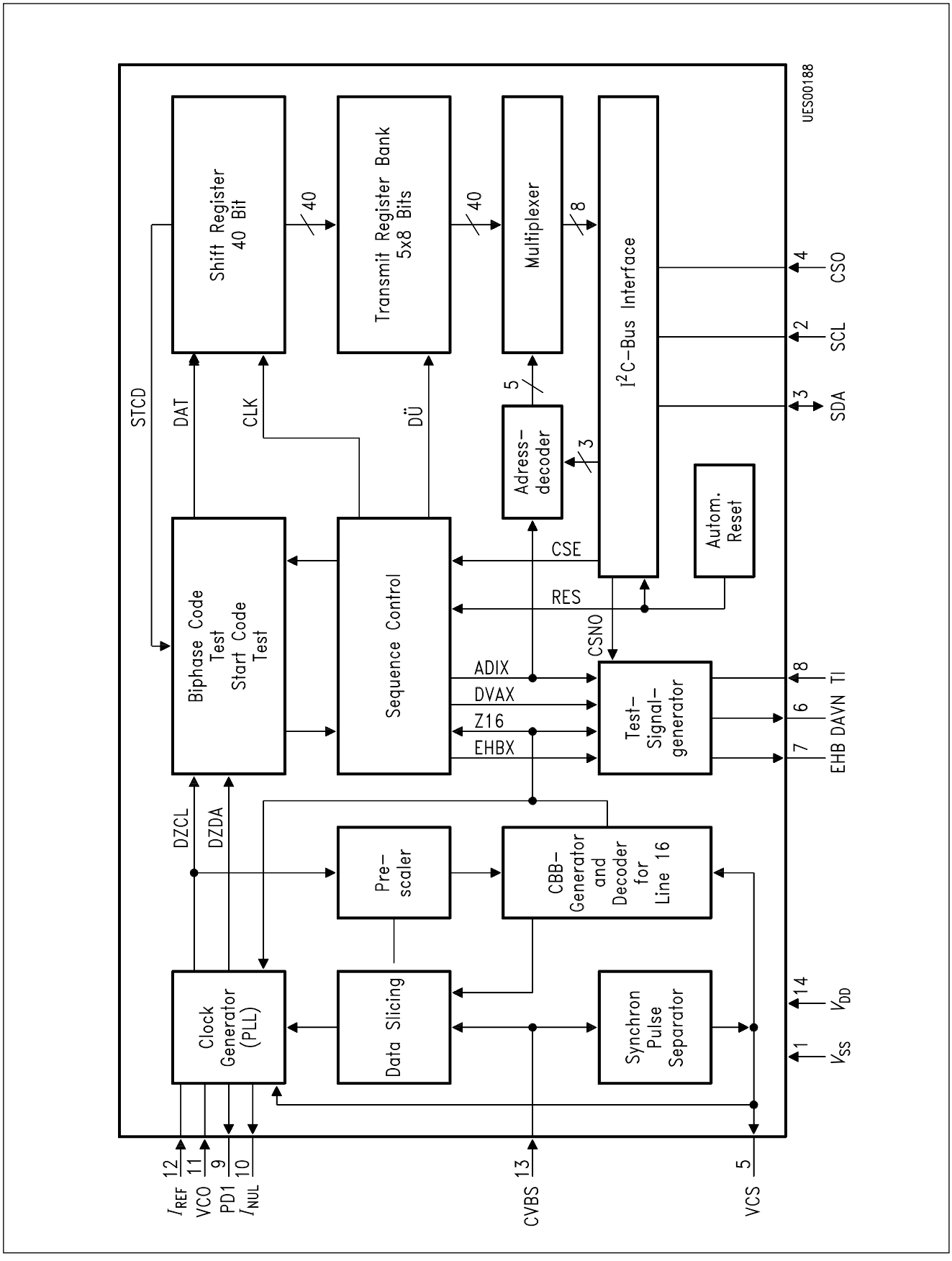


Pin Definitions and Functions

Pin No. P-DIP-14-1	Pin No. P-DSO-20-1	Symbol	Function
1		V_{SS}	Ground (0 V)
	1	$V_{SS\ 1}$	Ground (0 V)
	2	$V_{SS\ 2}$	Ground (0 V)
2	4	SCL	Clock line for I²C-Bus
3	5	SDA	Data line for I²C-Bus
4	6	CSO	To switch the hardware address of the chip from 21 H (CSO = low) to 23 H (CSO = high).
5	7	VCS	Data slicer derives the synchronous signal from the composite video blanking signal.
6	9	DAVN	The form of the output signal provides information whether the set transmitter is transmitting a VPS data line.
7	10	EHB	Output, on "high" level during first half frame.
8	11	TI	By means of the test pins the outputs DAVN and EHB can be switched to test signals outputs; in order to retrieve internal signals for test purposes – depending on the CSO pin.
9	12	PD1	PLL loop filter from system clock phase detector.
10	14	I_{NUL}	Connection for the resistor determining the lower limit of the VCO frequency.
11	15	VCO	Control input for VCO, increase of control voltage raises the VCO frequency.
12	16	I_{REF}	Connection for the resistors determining the upper limit of the VCO frequency.
13	17	CVBS	Video signal input.
14		V_{DD}	Positive voltage supply (+ 5 V)
	20	$V_{DD\ 1}$	Positive voltage supply (+ 5 V)
	19	$V_{DD\ 2}$	Positive voltage supply (+ 5 V)
	3	N.C.	Not connected
	8	N.C.	Not connected
	13	N.C.	Not connected
	18	N.C.	Not connected



Block Diagram for 1-Chip-VPS-Decoder

Circuit Description

The function of this integrated circuit is to regenerate the biphase coded VPS data from the CVBS signal. These data are transferred during line 16, which is part of the vertical blanking time. After decoding and a check for transmission errors, these data can be acquired by a microcontroller for further processing. The function of the circuit is explained in more detail by means of the block diagram.

The CVBS signal (pos. video) from the IF-stage is coupled to the device by means of a capacitor. The required level is typically 1 V_{pp}. Then the signal path is split into two parts:

In the synchronous pulse separator stage the CVBS signal is clamped, filtered and the video signal is clipped away from the synchronization pulses. The output signal of this stage is VCS signal. This is used as the control signal for the line 16 decoder and is also used for the blanking of the color burst. This signal is also used in the regeneration of the internal clock (PLL).

The second signal path leads to the data slicer. After amplification of the video signal the level is averaged and the slicing level is derived from this signal. The slicing level is equal to one half of the level difference between the minimum and the maximum value of the data signal. This assures the optimal slicing of the data from the video signal.

The biphase coded data signal sliced from the video signal and the synchronization pulse signal VCS are used in the clock generator circuit. Based upon a PLL, this circuit generates a clock frequency of 5 MHz from the VCS signal. This clock signal is synchronized to the line frequency. During line 16 the clock is synchronized to the data signal.

The synchronization of the data clock is controlled by the signal Z 16, which is the output of the decoder for line 16. This decoder is used to detect line 16 from the VCS signal and to control the data acquisition during this time. An indication signal for the first field of a frame is generated by measuring the duration of the VCS signal pulses and the interval between them.

The regenerated data signal and the recovered data clock are the input signals for a decoding logic which performs the test for the start code and the biphase code. For this purpose the data signal during line 16 is searched for the start bit. This bit, which is used for the synchronization of the decoding logic, is the only bit which does not comply with the biphase format (Manchester code). The detection of the startcode, which is contained in the next six bits following the start bit, is required for the transfer of the correct data into the output register.

Among the 15 bytes (8 bits/byte), which are transferred by the data line 16, only 5 bytes are important for the operation of VPS in the video recorder. These are the 5th and the 11th through the 14th byte. These 40 bits in total are transferred into a serial operating register buffer. The check for the correct transfer of the data according the biphase code is performed during the complete transfer of the data telegram in line 16. After the end of word 14 the relevant bytes are transferred into the transmission register bank. This is done when a microcontroller can read the data from the transmission register bank via the I^2C-Bus interface. The device can operate on the I^2C-Bus as slave-transmitter device. After reading the data, all registers are set to hex "F". Only after the correct reception of data line 16, is the register content updated again.

1) the start code has been identified
2) the transmission was done correctly according to the biphase code format, and
3) if there is no concurrent access to the device via the I^2C-Bus.

Because of the fact that data line 16 is transmitted only once during a frame (two fields), the reading of the transfer registers has to be done within a period of greater than 40 ms between read operations.

The transfer of the data via I²C-Bus is explained according to the following description and the **figures 5 and 6**. The communication protocol uses the following format:

START	Chip address of Master	AS	Word 11 of Slave	AM	⋯	Word 14 of Slave	AM	Word 5 of Slave	NAM	STOP

The information content of the bytes 11 through 14 and the byte number 5 are given in **figure 7**.

As a chip address for the I²C-Bus the following address is selected

Bit Number:	7	6	5	4	3	2	1	0
	0	0	1	0	0	0	CSO	0

If the device's chip select input is set to a low level or a high level, then bit 1 (CSO) has to be set to "0" or "1"respectively. Bit 0 is the data direction bit and has to be set to "1" because of the fact that only "Read" operations can be performed. (Slave transmitter mode.)

The data transfer between master (microcontroller) and slave (VPS decoder) uses the following procedure **(See figure 5)**:

0. If the bus is not occupied – idle state – then the clock line and the data line are both on logic "high" levels.
1. The master starts the data transmission by generating the start condition. This means that the SDA line is pulled down to a logic "low" level during the time when the SCL line is still on a logic "high" level. The byte address counter in the slave device is reset by this operation and points to byte 11. The following data clock pulses on the SCL line are generated by the master. For the data transfer it has to be observed that changes in the logical level on the SDA line are only possible if the SCL line is kept on a "low" level. The only exceptions are the start and stop conditions on the I²C-Bus.
2. The master sends the chip address on the SDA line with the first 8 data clock pulses on SCL to the VPS decoder.
3. During the 9th clock pulse the master releases the SDA line. Due to the external pull-up, the SDA line goes to a "high" level and the VPS decoder (slave) generates an acknowledge by pulling the SDA line to a "low" level. At this time the slave switches in the transmission mode.
4. During the next 8 clock pulses the slave outputs the data of the addressed data byte to the SDA line.

5. The reception of the byte will be acknowledged by the master during the following clock pulse. This means the master pulls the SDA line to a "low" level. This action increases the byte counter in the slave increments and prepares the output of the next data byte.
6. The slave outputs the next data byte to the SDA line.
7. and 8.

   For every data byte to be transferred, steps 5 and 6 have to be repeated. To conclude the read operation, the master does not acknowledge the last byte – as described in step no.9.
9. During the acknowledge interval the master lets the SDA line remain in the "high" status (so called Non Acknowledge by Master, NAM). The slave understands this NAM as the end of the communication process and switches from transmit mode to receiver mode.
10. The master now has the full control over the SDA line and finishes the communication process by issuing the stop-condition. This means that during the time when the SCL is on "high" level, the microcomputer generates a "low" to "high" transmission on the SDA line. This brings the I^2C-Bus into the idle state.

Description of Added Functions

1. The pin Data-Valid (DAVN) allows very easy control of the availability of the VPS signal by the selected TV transmitter. If the VPS data line is available, this pin will show pulses with the frequency of the frame repetition rate. This output is set "high" at the beginning of line 16 and is reset by the data transfer pulse, an internal signal at the end of byte 14 in the data line 16. If, due to a missing VPS information in the CVBS signal, this data transfer-pulse is not generated, the DAVN pin remains on a "high" level.

   This output is also set "high", when the circuit is accessed via the I^2C-Bus. This may be useful in some cases when the output is low without the presence of a CVBS signal – thus pretending a TV transmitter carrying VPS information.

2. By means of the "Test" pin (TI = "high") it is possible to use the DAVN pin to output internal test signals. Depending on the status of the input CSO, the internal signal Z16N (CSO = "low") or the ADIX signal (CSO = "high") is switched to the DAVN output.

3. The data transfer from the VPS decoder to the microcomputer starts after the master controller has transmitted the chip address of SDA 5642. This chip address has to be identical with the hardware address of the VPS decoder. By means of the CSO input it is possible to switch this hardware address from 21 H (CSO = "low") to 23 H (CSO = "high").

4. The output EHB generates an indication for both of the fields in a frame. During the first-field this pin shows the "high" level. The correct timing of this pulse is given in **figure 4**. For test purpose this pin can be switched to the test signal output mode. This is done by setting the TI pin to high. The output signal in this mode depends on the logical level on the CSO pin. If CSO is "low", the internal signal LL64ON is generated, if the CSO pin is "H" the output signal is DZDAX, which is also an internal test signal, is generated.

Absolute Maximum Ratings
T_A = 25 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ambient temperature	T_A	0		70	˚C	in operation
Storage temperature	T_{stg}	– 40		125	˚C	by storage
Total power dissipation	P_{tot}			300	mW	
Power dissipation per output	P_{DQ}			10	mW	
Input voltage	V_{IM}	– 0.3		6	V	
Supply voltage	V_{DO}	– 0.3		6	V	
Thermal resistance	$R_{th\ SU}$			80	K/W	

Operating Range

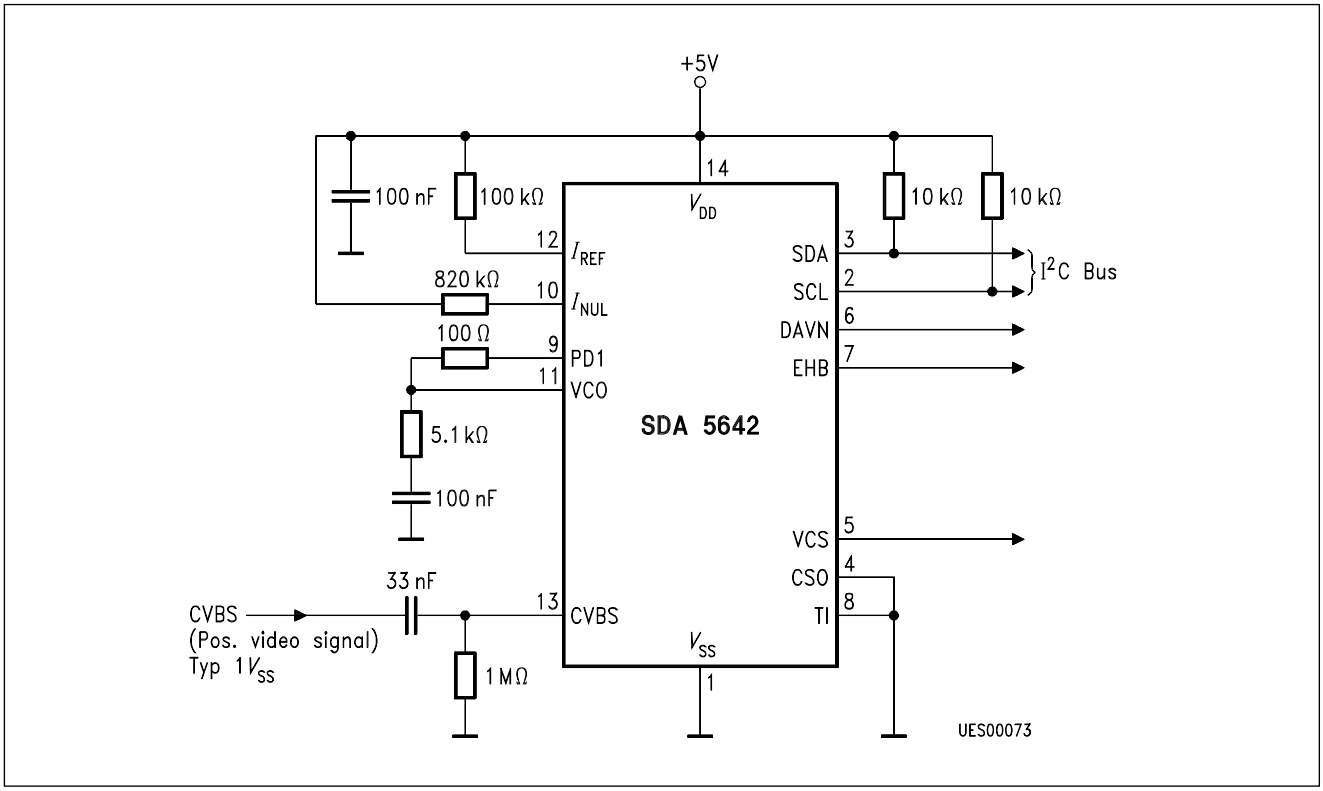
Supply voltage	V_{DD}	4.5	5	5.5	V	
Supply current	I_{DD}			50	mA	
Ambient temperature range	T_A	0		70	˚C	

Characteristics
T_A = 25 ˚C

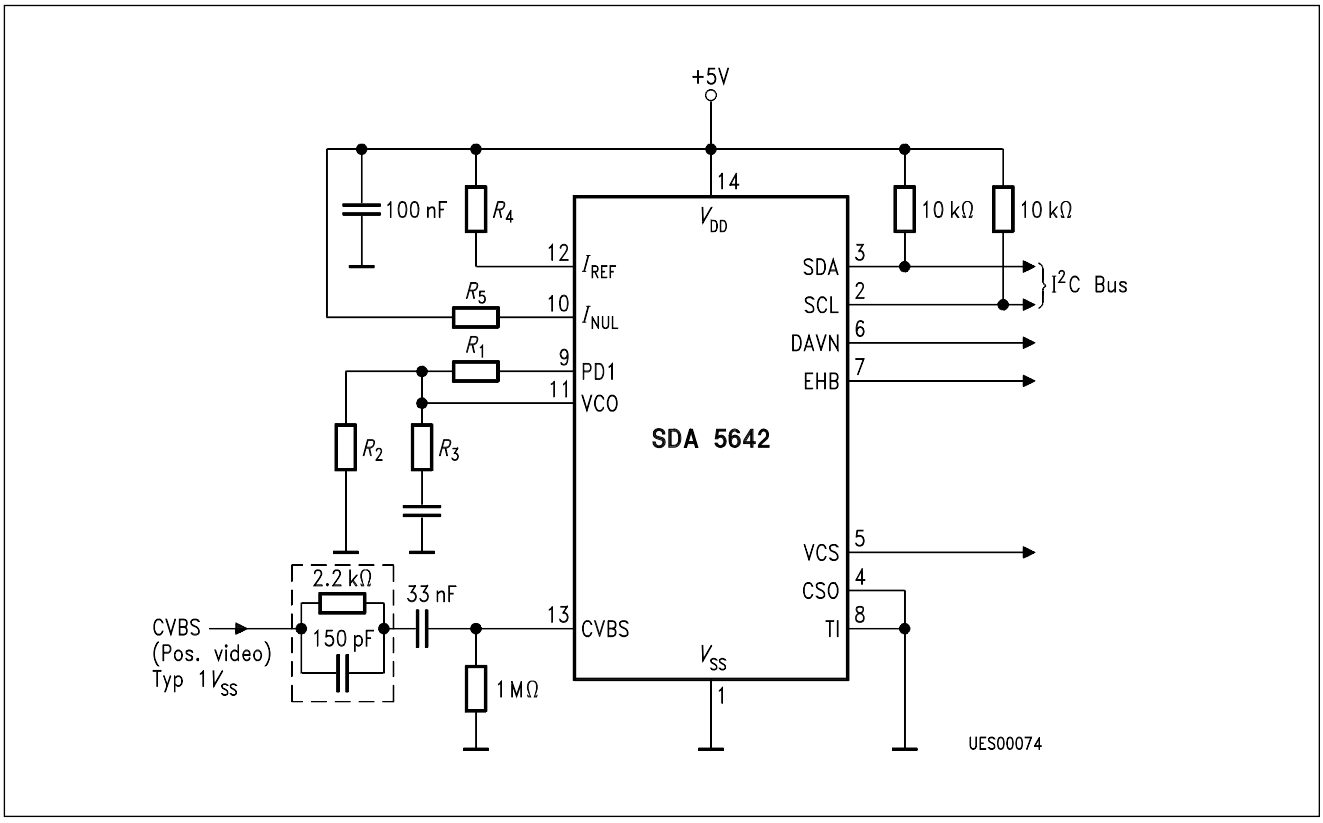
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals SDA, SCL						
H - input voltage	V_{IH}	3.0		V_{DD}	V	
L - input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input voltage	I_{IM}			10	µA	
Input Signals CSO, TI						
H - input voltage	V_{IH}	2.0		V_{DD}	V	
L - input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_{IM}			10	µA	
Input Signals CVBS (pos. Video, neg. Sync)						
Video input signal level	V_{CVBS}	0.7	1.0	2.0	V	
Synchron signal amplitude	V_{SYNC}	0.15	0.3	1.0	V	
Data amplitude	V_{DAT}	0.25	0.5	1.0	V	
Coupling capacitor	C_C		33		nF	
H - input current	I_{IH}			10	µA	V_I = 5 V
L - input current	I_{IL}	– 1000	– 400	– 100	µA	V_I = 0 V
Source impedance	R_S			250	Ω	
Leakage resistance at coupling capacitor	R_C	0.91	1	1.2	MΩ	

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signals DAVN, EHB, VCS						
H - output voltage	V_{QH}	V_{DD} – 0.5			V	I_Q = – 100 µA
L - output voltage	V_{QL}			0.4	V	I_Q = 1.6 mA
Output Signals SDA (Open-Drain-Stage)						
L - output voltage	V_{QL}			0.4	V	I_Q = 3.0 mA
Permissible output voltage				5.5	V	
PLL – Loop Filter Components						
Resistance at PD1	R_1	0	100	150	Ω	
Resistance at VCO	R_2		820		kΩ	
Attenuation resistance	R_3		5.6		kΩ	
Integration capacitor	C		100		nF	
VCO – Frequence Range Adjustment						
Resistance at IREF (for bias current adjustment)	R_4		100		kΩ	
Resistance at INUL (for quiescent current adjustment)	R_5		820		kΩ	



Test Circuit
Data Line Receiver



Application Circuit
Data Line Receiver

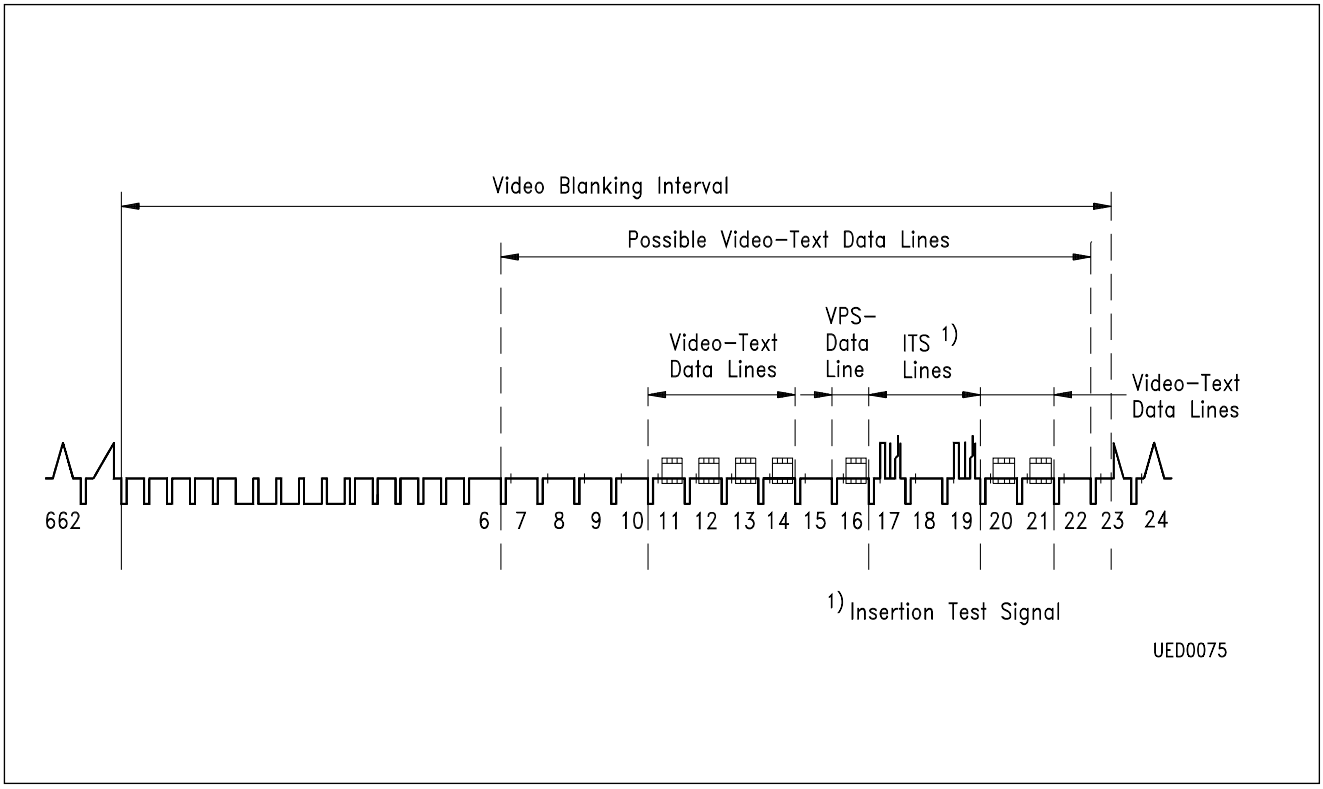


Figure 1
CVBS Signal with Position of VPS Data Line

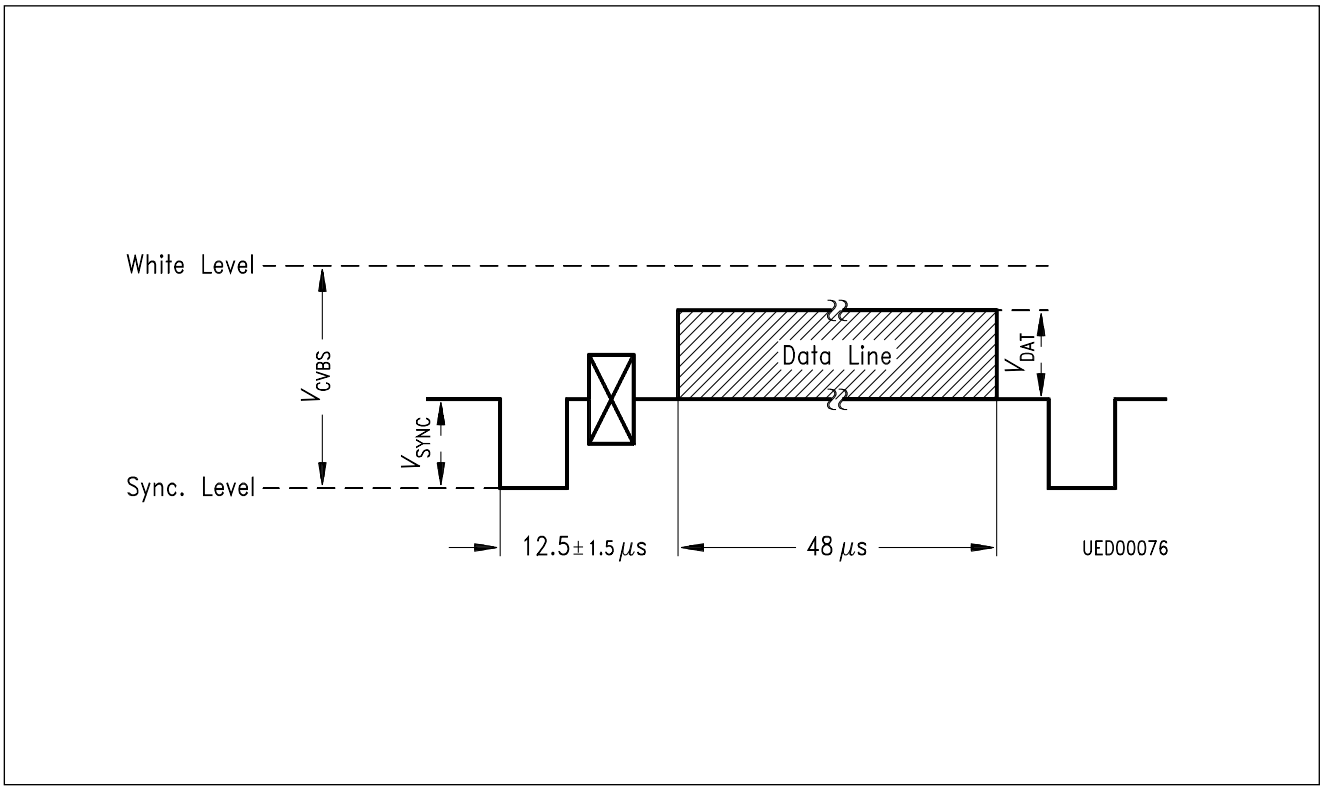


Figure 2
Insertion of Data Line into CVBS Signal

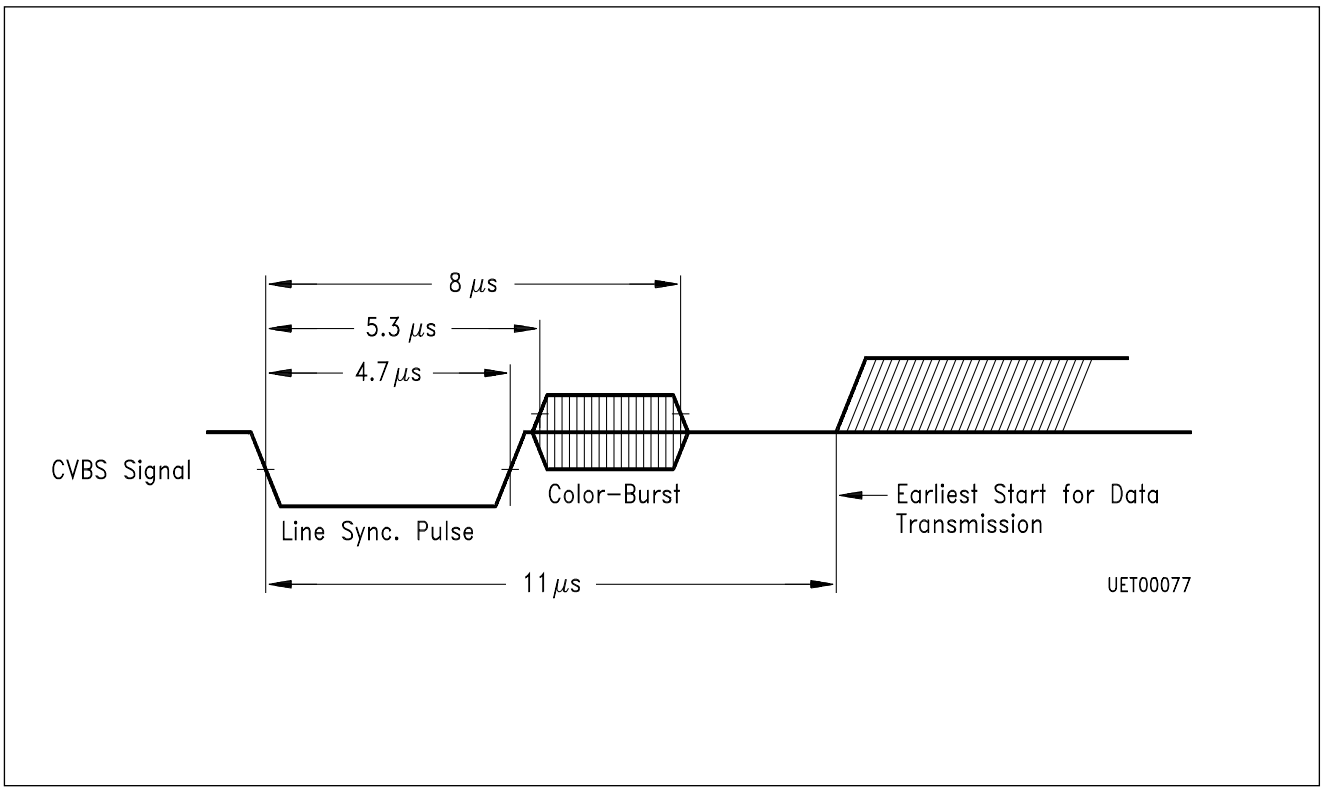


Figure 3
Video Signal

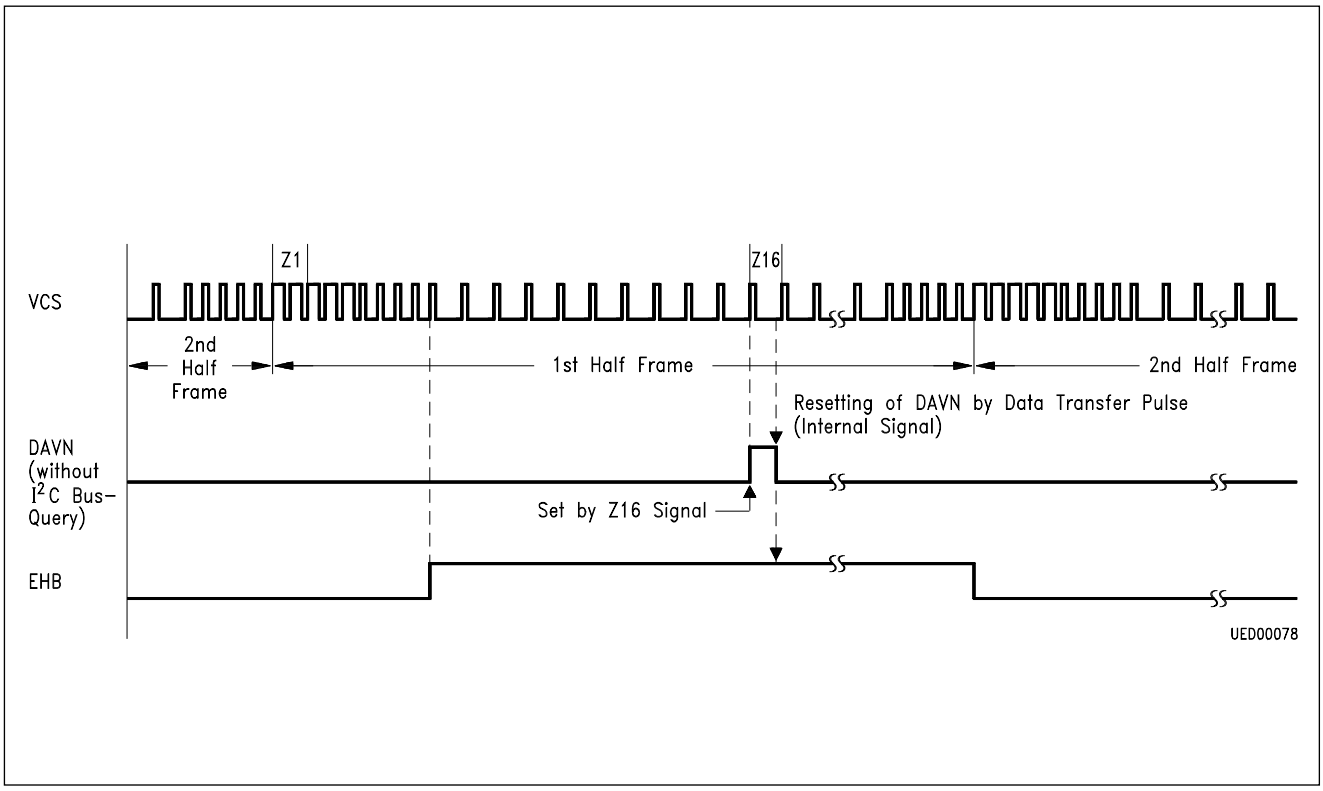


Figure 4
VCS-DAVN-EHB Signal

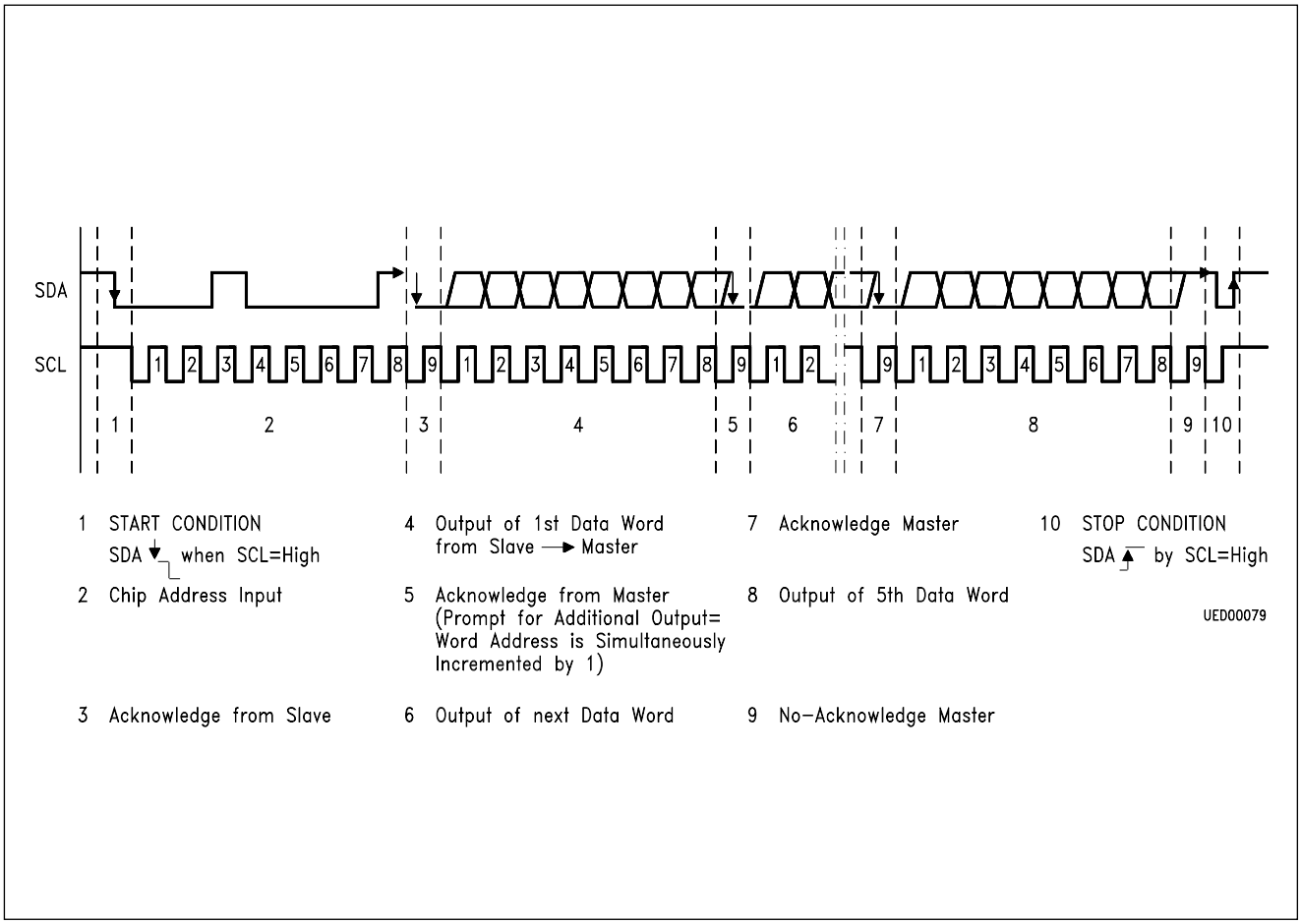


Figure 5
Transfer Protocol for I²C-Bus

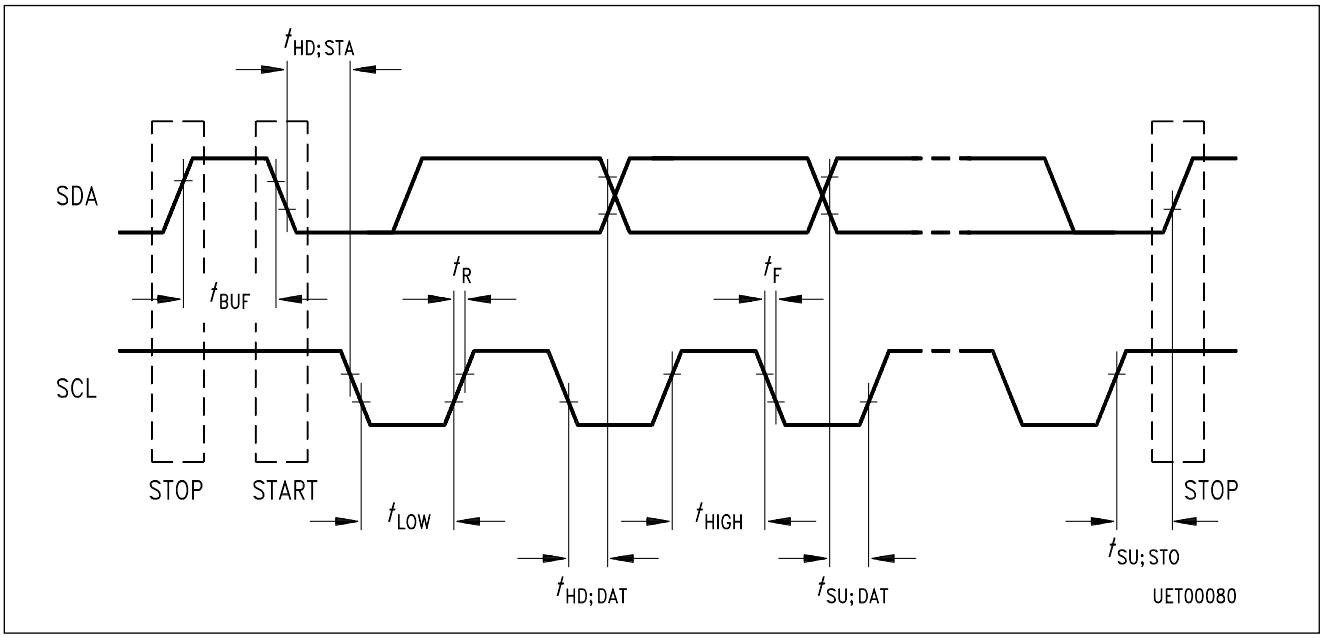


Figure 6
I²C-Bus Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{SCL}	0	100	kHz
Inactive time period prior to new transmission start-up	t_{BUF}	4.7		µs
Hold time during start condition (subsequent to this time period the first Clock pulse will be generated)	$t_{HD;\,STA}$	4.0		µs
LOW-period of clock	t_{LOW}	4.7		µs
HIGH-period of clock	t_{HIGH}	4.0		µs
Set-up time for Data	$t_{SU;\,DAT}$	250		ns
Rise time for SDA and SCL signal	t_R		1	µs
Fall time for SDA and SCL signal	t_F		300	ns
Set-up time for SCL clock during STOP conditions	$t_{SU;\,STO}$	4.7		µs

All values referred to V_{IH} and V_{IL} levels.

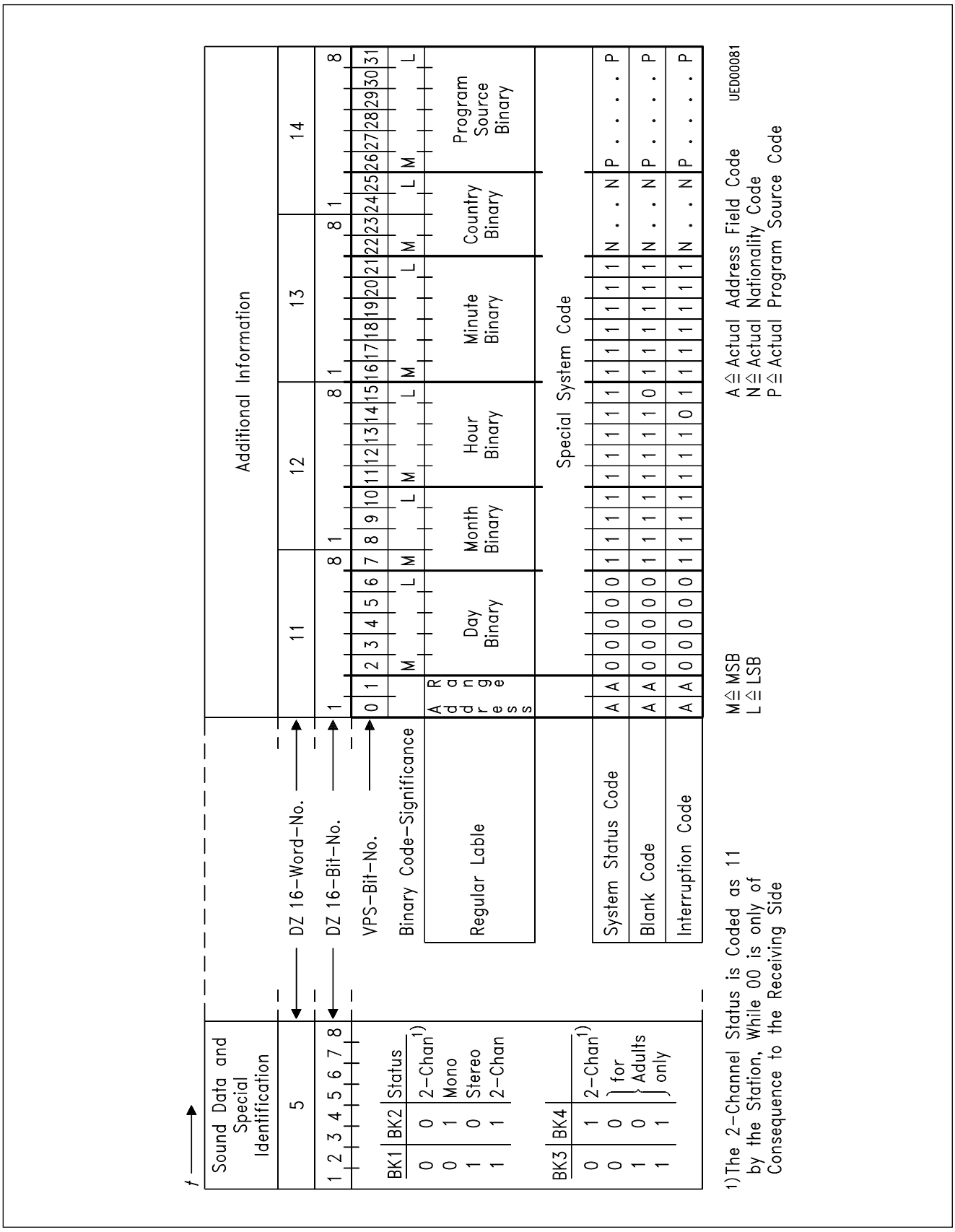


Figure 7
Data Format of Additional Information in Data Line 16