

ICS650-01 System Peripheral Clock Source

Description

The ICS650-01 is a low cost, low jitter, high performance clock synthesizer for system peripheral applications. Using analog/digital Phase-Locked Loop (PLL) techniques, the device accepts a parallel resonant 14.31818 MHz crystal input to produce up to eight output clocks. The device provides clocks for PCI, SCSI, Fast Ethernet, Ethernet, USB, and AC97. The user can select one of three USB frequencies, and also one of three AC97 audio frequencies. The OE pin puts all outputs into a high impedance state for board level testing. All frequencies are generated with less than one ppm error, meeting the demands of SCSI and Ethernet clocking.

The ICS650 can be mask customized to produce any frequencies from 1 to 150 MHz.

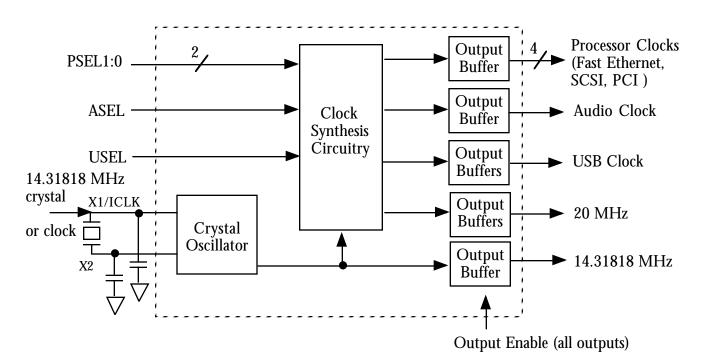
Features

• Packaged in 20 pin tiny SSOP (QSOP)



- Operating VDD of 3.3V or 5V
- Less than one ppm synthesis error in all clocks
- Inexpensive 14.31818 MHz crystal or clock input
- Provides Ethernet and Fast Ethernet clocks
- Provides SCSI clocks
- Provides PCI clocks
- Selectable AC97 audio clock
- Selectable USB clock
- OE pin tri-states the outputs for testing
- Selectable frequencies on three clocks
- Duty cycle of 40/60
- Advanced, low power CMOS process

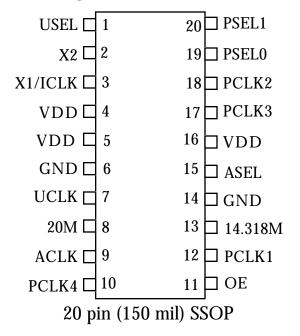
Block Diagram





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Pin Assignment



Processor Clock (MHz)

| PSEL1 | PSEL0 | PCLK1 | PCLK2,3 | PCLK4 |
|-------|-------|---------------------------------|---------|-------|
| 0 | 0 | 25.00 | 50.00 | 18.75 |
| 0 | M | TEST | TEST | TEST |
| 0 | 1 | TEST | TEST | TEST |
| M | 0 | 40.00 | 80.00 | 20.00 |
| M | M | 33.3334 | 66.6667 | 25.00 |
| M | 1 | 20.00 | 40.00 | 25.00 |
| 1 | 0 | 20.00 | 33.3334 | 25.00 |
| 1 | M | 20.00 | 66.6667 | 25.00 |
| 1 | 1 | Stops low all clocks except 20M | | |

Audio Clock (MHz)

| ASEL | ACLK |
|------|--------|
| 0 | 49.152 |
| M | 24.576 |
| 1 | 12.288 |
| | |

USB Clock (MHz)

| USEL | UCLK |
|------|------|
| 0 | 12 |
| M | 24 |
| 1 | 48 |

0 = connect directly to ground, 1 = connect directly to VDD, M=leave unconnected (floating)

Pin Descriptions

| Pin # | Name | Type | Description |
|-------|---------|------|--|
| 1 | USEL | I | UCLK Select pin. Determines frequency of USB clock per table above. |
| 2 | X2 | XO | Crystal connection. Connect to parallel mode 14.31818 MHz crystal. Leave open for clock. |
| 3 | X1/ICLK | XI | Crystal connection. Connect to parallel mode 14.31818 MHz crystal, or clock. |
| 4 | VDD | P | Connect to VDD. Must be same value as other VDD. Decouple with pin 6. |
| 5 | VDD | P | Connect to VDD. Must be same value as other VDD. |
| 6 | GND | P | Connect to ground. |
| 7 | UCLK | О | USB clock output per table above. |
| 8 | 20M | О | Fixed 20 MHz output for Ethernet. Only clock that runs when PSEL1=PSEL0=1. |
| 9 | ACLK | О | AC97 Audio clock output per table above. |
| 10 | PCLK4 | О | PCLK output number 4 per table above. |
| 11 | OE | I | Output Enable. Tri-states all outputs when low. |
| 12 | PCLK1 | О | PCLK output number 1 per table above. |
| 13 | 14.318M | О | 14.31818 MHz buffered reference clock output. |
| 14 | GND | P | Connect to ground. |
| 15 | ASEL | I | ACLK Select pin. Determines frequency of Audio clock per table above. |
| 16 | VDD | P | Connect to VDD. Must be same value as other VDD. Decouple with pin 14. |
| 17 | PCLK3 | О | PCLK output number 3 per table above. |
| 18 | PCLK2 | О | PCLK output number 2 per table above. |
| 19 | PSEL0 | I | Processor Select pin #0. Determines frequencies on PCLKs 1-4 per table above. |
| 20 | PSEL1 | I | Processor Select pin #1. Determines frequencies on PCLKs 1-4 per table above. |

Key: I = Input; XO/XI = crystal connections; O = output; P = power supply connection

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Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units | | |
|--|-----------------------|---------|----------|---------|-------|--|--|
| ABSOLUTE MAXIMUM RATINGS (note 1) | | | | | | | |
| Supply voltage, VDD | Referenced to GND | | | 7 | V | | |
| Inputs and Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V | | |
| Ambient Operating Temperature | | 0 | | 70 | С | | |
| Soldering Temperature | Max of 10 seconds | | | 260 | С | | |
| Storage temperature | | -65 | | 150 | С | | |
| DC CHARACTERISTICS (VDD = 3.3V or 5V unless noted) | | | | | | | |
| Operating Voltage, VDD | | 3.0 | | 5.5 | V | | |
| Input High Voltage, VIH | Select inputs, OE | 2 | | | V | | |
| Input Low Voltage, VIL | Select inputs, OE | | | 0.8 | V | | |
| Output High Voltage, VOH | VDD=3.3V, IOH=-8mA | 2.4 | | | V | | |
| Output Low Voltage, VOL | VDD=3.3V, IOL=8mA | | | 0.4 | V | | |
| Output High Voltage, VOH, VDD = 3.3 or 5V | IOH=-8mA | VDD-0.4 | | | V | | |
| Operating Supply Current, IDD, at 5V | No Load, note 2 | | 50 | | mA | | |
| Operating Supply Current, IDD, at 3.3V | No Load, note 2 | | 30 | | mA | | |
| Short Circuit Current, VDD = 3.3 | Each output | | ±50 | | mA | | |
| Input Capacitance | Except X1 | | 7 | | pF | | |
| AC CHARACTERISTICS (VDD = 3.3) | V or 5V unless noted) | | | | | | |
| Input Crystal or Clock Frequency | | | 14.31818 | | MHz | | |
| Output Clocks Accuracy (synthesis error) | All clocks | | | 1 | ppm | | |
| Output Clock Rise Time | 0.8 to 2.0V | | | 1.5 | ns | | |
| Output Clock Fall Time | 2.0 to 0.8V | | | 1.5 | ns | | |
| Output Clock Duty Cycle | At VDD/2 | 40 | 50 | 60 | % | | |
| One Sigma Jitter, except ACLK | | | 75 | | ps | | |
| One Sigma Jitter, ACLK | | | 170 | | ps | | |
| Absolute Clock Period Jitter PCLK, UCLK, 20M | | - 500 | | 500 | ps | | |

Notes:

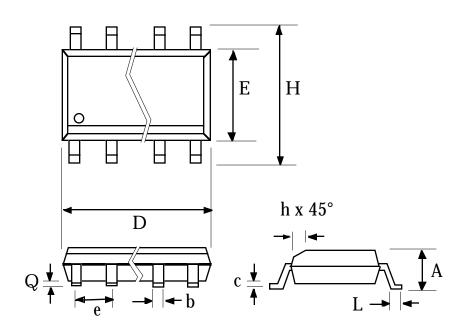
- 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
- 2. With all clocks at highest frequencies.

External Components

The ICS650 requires a minimum number of external components for proper operation. Decoupling capacitors of $0.1\mu F$ should be connected between VDD and GND (on pins 4 and 6, and pins 16 and 14), as close to the chip as possible. A series termination resistor of 33Ω may be used for each clock output. The 14.31818 MHz crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode, parallel resonant, 30ppm or better (to meet the Ethernet specs). Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = (C_L -12) x 2. So for a crystal with 16pF load capacitance, two 8pF caps should be used. If a clock input is used, drive it into X1 and leave X2 unconnected.



Package Outline and Package Dimensions



20 pin SSOP

| | Millimeters | | |
|--------|-------------|-------|--|
| Symbol | Min | Max | |
| A | 1.55 | 1.73 | |
| b | 0.203 | 0.305 | |
| c | 0.190 | 0.254 | |
| D | 8.560 | 8.740 | |
| E | 3.810 | 4.000 | |
| Н | 5.840 | 6.200 | |
| e | 0.635 BSC | | |
| h | | 0.410 | |
| L | 0.406 | 0.889 | |
| Q | 0.127 | 0.250 | |

Ordering Information

| Part/Order Number | Marking | Package | Shipping | Temperature |
|-------------------|-------------|-------------|---------------|-------------|
| ICS650R-01 | ICS650R-01 | 20 pin SSOP | Tubes | 0 to 70 C |
| ICS650R-01T | ICS650R-01 | 20 pin SSOP | Tape and Reel | 0 to 70 C |
| ICS650R-01I | ICS650R-01I | 20 pin SSOP | Tubes | -40 to 85 C |
| ICS650R-01IT | ICS650R-01I | 20 pin SSOP | Tape and Reel | -40 to 85 C |

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