ICS501
LOCO™ PLL Clock Multiplier

Description

The ICS501 LOCO™ is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. The name LOCO stands for LOw Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

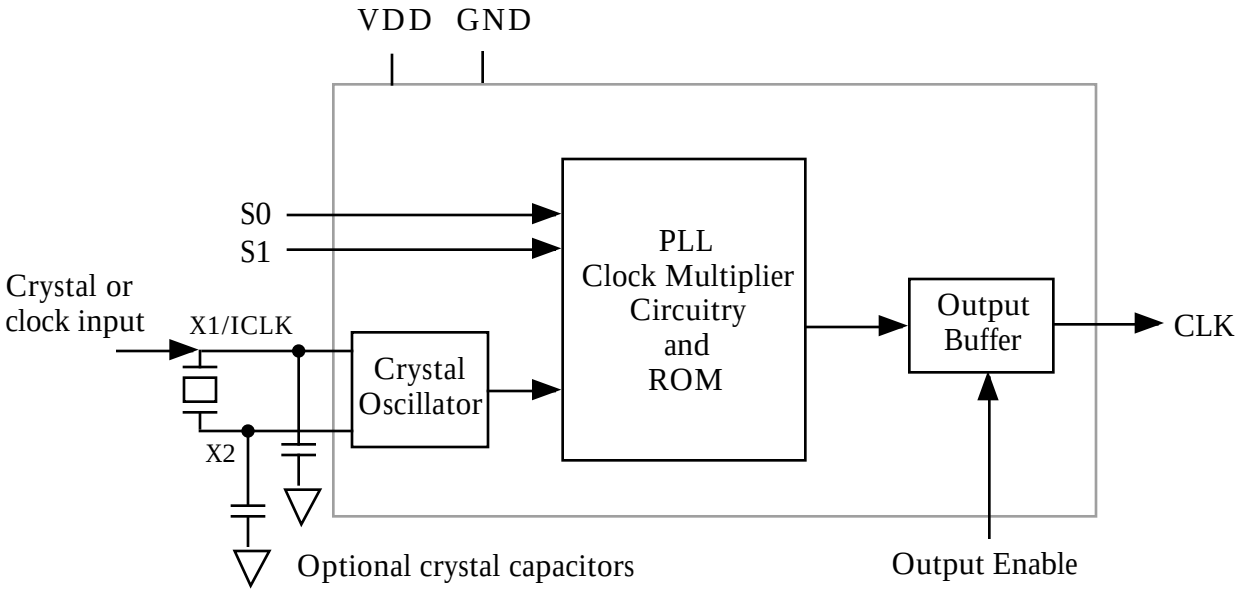
Stored in the chip's ROM is the ability to generate 9 different multiplication factors, allowing one chip to output many common frequencies (see page 2).

The device also has an Output Enable pin that tri-states the clock output when the OE pin is taken low.

Features

- Packaged as 8 pin SOIC or die
- ICS' lowest cost PLL clock
- Zero ppm multiplication error
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 160 MHz
- Extremely low jitter - 25 ps one sigma
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 160 MHz
- Mask option for 9 selectable frequencies
- Operating voltages of 3.0 to 5.5V
- Tri-state output for board level testing
- 25mA drive capability at TTL levels
- Ideal for oscillator replacement
- Industrial temperature version available
- Advanced, low power CMOS process

Block Diagram



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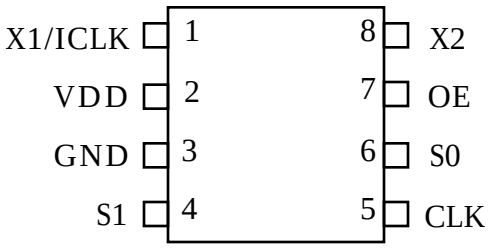
Pin Assignment



Clock Output Table

S1	S0	CLK	Minimum Input
0	0	4X input	per page 3
0	M	5.3125X input	20MHz
0	1	5X input	per page 3
M	0	6.25X input	4MHz
M	M	2X input	per page 3
M	1	3.125X input	8MHz
1	0	6X input	per page 3
1	M	3X input	per page 3
1	1	8X input	per page 3

0 = connect directly to ground.
1 = connect directly to VDD.
M = leave unconnected (floating).

Common Output Frequencies Examples (MHz)

Output	20	24	30	32	33.33	37.5	40	48	50	60	62.5
Input	10	12	10	16	16.66	12	10	12	16.66	10	20
Selection (S1, S0)	M, M	M, M	1, M	M, M	M, M	M, 1	0, 0	0, 0	1, M	1, 0	M, 1
Output	64	66.66	72	75	80	83.33	90	100	106.25	120	125
Input	16	16.66	12	12	10	16.66	15	20	20	15	20
Selection (S1, S0)	0, 0	0, 0	1, 0	M, 0	1, 1	0, 1	1, 0	0, 1	0, M	1, 1	M, 0

Note that all of the above outputs are achieved by using a common, inexpensive 10MHz to 20MHz crystal. Consult MicroClock/ICS on how to achieve other output frequencies.

Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection or clock input.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	S1	TI	Select 1 for output clock. Connect to GND or VDD or float.
5	CLK	O	Clock output per Table above.
6	S0	TI	Select 0 for output clock. Connect to GND or VDD or float.
7	OE	I	Output Enable. Tri-states CLK output when low. Internal pull-up.
8	X2	O	Crystal connection. Leave unconnected for clock input.

Key: I = Input, TI = Tri-Level Input, O = output, P = power supply connection

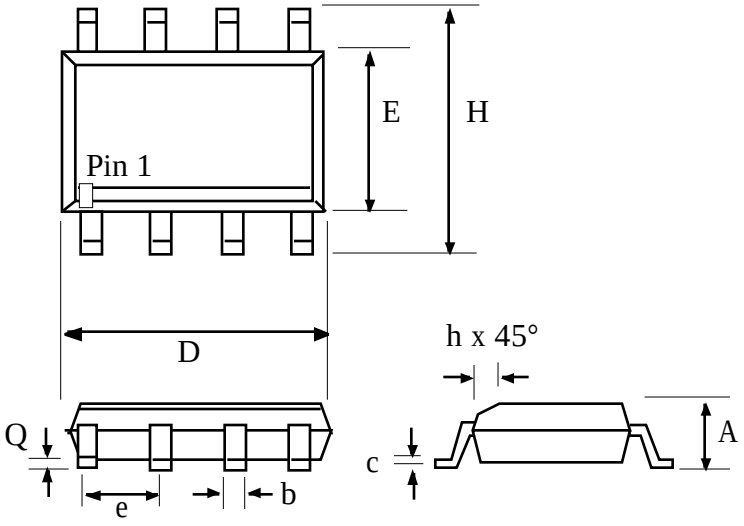
Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
	ICS501MI only	-40		85	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Operating Voltage, VDD		3		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1			V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)			(VDD/2)-1	V
Input High Voltage, VIH	OE (Pin 7)	2			V
Input Low Voltage, VIL	OE (Pin 7)			0.8	V
Input High Voltage, VIH	S0, S1	VDD-0.5			V
Input Low Voltage, VIL	S0, S1			0.5	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal	No Load, 100MHz		20		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor	Pin 7		270		kΩ
Input Capacitance, S1, S0 , and OE	Pins 4, 6, 7		4		pF
AC CHARACTERISTICS (VDD = 5.0V unless otherwise noted)					
Input Frequency, crystal input		5		27	MHz
Input Frequency, clock input		2		50	MHz
Output Frequency, VDD = 4.5 to 5.5V	0 C to +70 C	14		160	MHz
	-40 C to +85 C	14		140	MHz
Output Frequency, VDD = 3.0 to 3.6V	0 C to +70 C	14		100	MHz
	-40 C to +85 C	14		90	MHz
Output Clock Rise Time	0.8 to 2.0V		1		ns
Output Clock Fall Time	2.0 to 0.8V		1		ns
Output Clock Duty Cycle	1.5V, up to 160 MHz	45	49 to 51	55	%
PLL Bandwidth		10			kHz
Output Enable Time, OE high to output on				50	ns
Output Disable Time, OE low to tri-state				50	ns
Absolute Clock Period Jitter	Deviation from mean		±70		ps
One Sigma Clock Period Jitter			25		ps

External Components / Crystal Selection

The ICS501 requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS501 to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 12 pF, so a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 12 pF, crystal capacitors should be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L-12)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS501M	ICS501M	8 pin SOIC	0 to 70 °C
ICS501MT	ICS501M	8 pin SOIC on tape and reel	0 to 70 °C
ICS501MI	ICS501I	8 pin SOIC	-40 to +85 °C
ICS501MIT	ICS501I	8 pin SOIC on tape and reel	-40 to +85 °C
ICS501-DWF	-	Die on uncut, probed wafers	0 to 70 °C
ICS501-DPK	-	Tested die in waffle pack	0 to 70 °C