



ICS508

PECL TO CMOS CONVERTER

Description

The ICS508 is the most cost effective way to generate a high quality, high frequency CMOS clock output from a PECL clock input.

The ICS508 has separate VDD supplies for the PECL input buffer and the output buffer, allowing different voltages to be used. For example, the input clock could use a 3.3 V supply while the output operates from 2.5V.

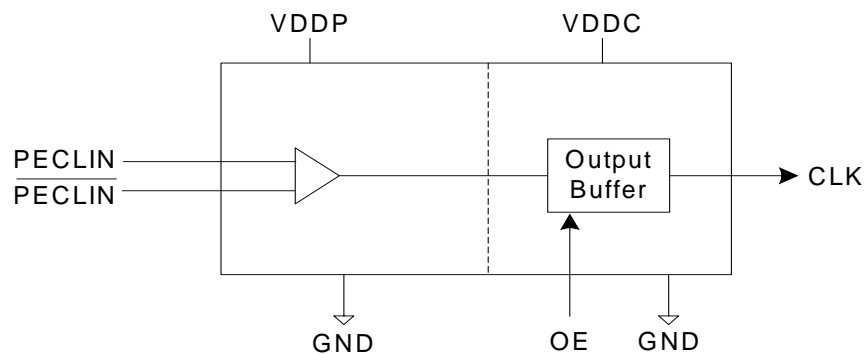
The device has an Output Enable pin that tri-states the clock output when the OE pin is taken low.

The ICS508 is a member of ICS' ClockBlocks™ family.

Features

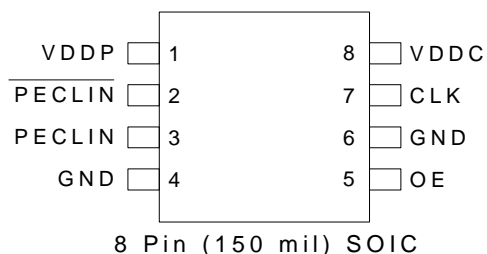
- Packaged in 8 pin SOIC or die
- Separate VDD supplies allow voltage translation
- Clock frequency of 0 - 250 MHz
- Duty cycle of 45/55
- Operating voltages of 2.375 to 5.5V
- Tri-state output for board level testing
- 24mA output drive capability
- Industrial temperature version available
- Advanced, low power, sub-micron CMOS process

Block Diagram





Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDDP	Output	Connect to 3.3V or 5V. Supplies PECL input buffer.
2	$\overline{\text{PECLIN}}$	Input	Complementary PECL clock input.
3	PECLIN	Input	PECL clock input.
4	GND	Power	Connect to ground.
5	OE	Input	Output enable. Tri-states CLK output when low. Internal pull-up to VDDC.
6	GND	Power	Connect to ground.
7	CLK	Output	Clock output.
8	VDDC	Power	Connect to 2.5V, or 3.3V, or 5V. Supplies output buffer and OE pin.

External Components

The ICS508 requires two 0.01 μ F decoupling capacitors to be connected between VDDP and GND and between VDDC and GND. They must be connected close to the ICS508 to minimize lead inductance. A 33 Ω series terminating resistor can be used next to the CLK pin.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS508. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDDP and VDDC	7V
PECL Inputs	-0.5V to VDDP+0.5V
Clock Output and OE Pin	-0.5V to VDDC+0.5V
Ambient Operating Temperature, ICS508	0 to +70°C
Ambient Operating Temperature, ICS508MI	-40 to +85°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature, ICS508M	0		+70	°C
Ambient Operating Temperature, ICS508MI	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.15		+3.45	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDDP = VDDC = 3.3V ±5% , Ambient temperature 0 to +70°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD	VDDP	3		5.5	V
	VDD	VDDC	2.375		5.5	V
Peak to Peak Input Voltage		PECLIN	0.3		1	V
Common Mode Range		PECLIN VDDP = 5V	VDDP - 3.7		VDDP - 0.6	V
		PECLIN VDDP = 3.3V	VDDP - 2.0		VDDP - 0.6	V
Input High Voltage	V _{IH}	OE only	2		VDDC	V
Input Low Voltage	V _{IL}	OE only			0.8	V



Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	VDDC = 5V IOH = -24 mA	VDDC - 0.4			V
		VDDC = 3.3V IOH = -18 mA	VDDC - 0.4			V
		VDDC = 2.5V IOH = -8 mA	VDDC - 0.4			V
Output Low Voltage	V_{OL}	VDDC = 5V IOL = 24 mA			0.4	V
		VDDC = 3.3V IOL = 18 mA			0.4	V
		VDDC = 2.5V IOL = 8 mA			0.4	V
On Chip Pull-up Resistor	R_{PU}	OE		250		k Ω
Operating Supply Current	IDDP	100 MHz, no load		1.5		mA
	IDDC	100 MHz, no load		8		mA

Note 1: VDDP must always be greater than or equal to VDDC

AC Electrical Characteristics

VDDP = VDDC = 3.3V \pm 5%, Ambient Temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}		0		250	MHz
Output Clock Rise Time		0.8V to 2.0V, VDDC = 5V		0.4		ns
		0.8V to 2.0V, VDDC = 3.3V		0.6		ns
		0.8V to 2.0V, VDDC = 2.5V		1		ns
Output Clock Fall Time		2.0V to 0.8V, VDDC = 5V		0.4		ns
		2.0V to 0.8V, VDDC = 5V		0.6		ns
		2.0V to 0.8V, VDDC = 5V		1		ns
Output Enable Time		OE high to output on		7	20	ns
Output Disable Time		OE low to tri-state		7	20	ns
Propagation Delay		VDDP = 5V, VDDC = 5V		4	6	ns
		VDDP = 5V, VDDC = 3.3V		4.5	7	ns
		VDDP = 5V, VDDC = 2.5V		5.5	9	ns
		VDDP = 3.3V, VDDC = 3.3V		4.5	7	ns
		VDDP = 3.3V, VDDC = 2.5V		5.5	9	ns
Output Clock Duty Cycle 0 - 100 MHz		Any VDD combination	45		55	%

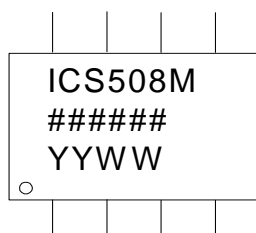


Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Duty Cycle 100 - 166 MHz		VDDP = 5V, VDDC = 5V	45		55	%
		VDDP = 5V, VDDC = 3.3V	45		55	%
		VDDP = 5V, VDDC = 2.5V	40		60	%
		VDDP = 3.3V, VDDC = 3.3V	40		60	%
		VDDP = 3.3V, VDDC = 2.5V	45		55	%
Output Clock Duty Cycle 166 - 250 MHz		VDDP = 5V, VDDC = 5V	40		60	%
		VDDP = 5V, VDDC = 3.3V	40		60	%
		VDDP = 5V, VDDC = 2.5V	35		65	%
		VDDP = 3.3V, VDDC = 3.3V	35		65	%
		VDDP = 3.3V, VDDC = 2.5V	40		60	%

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Marking Diagram



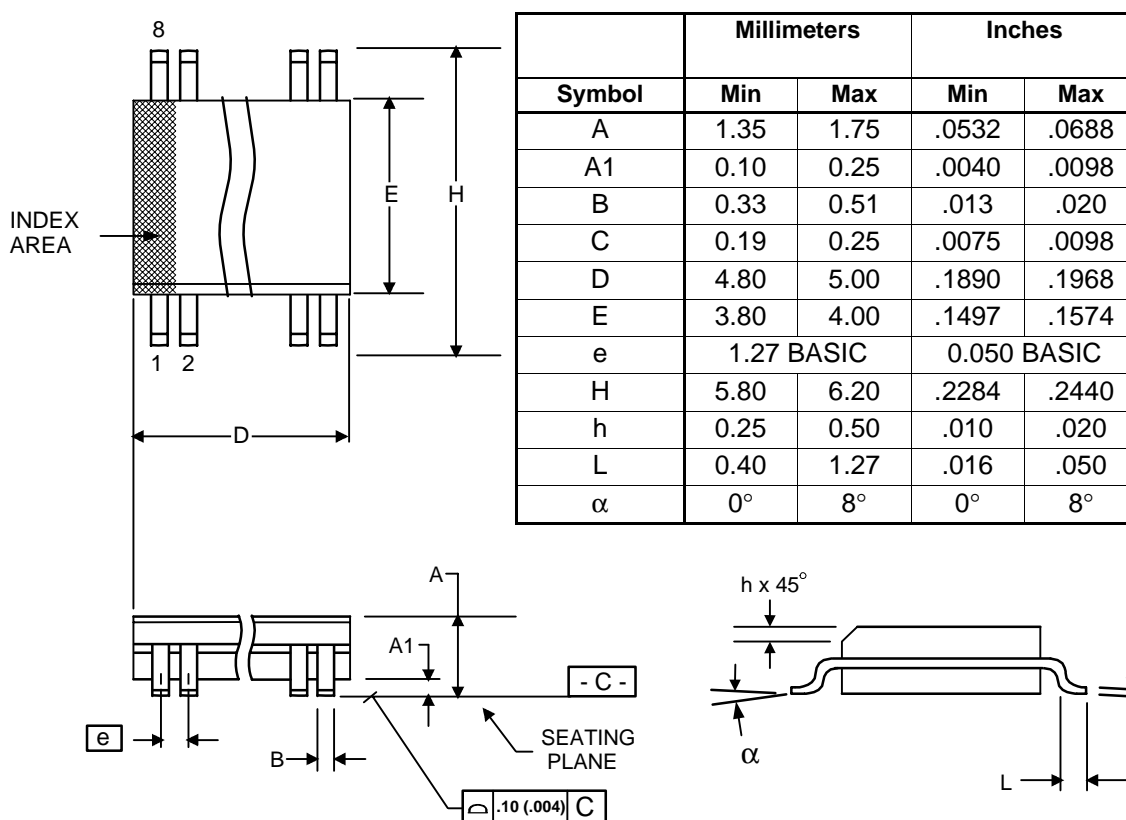
Notes:

1. ##### is the lot number
2. YYWW is the last two digits of the year and the week number that the part was assembled



Package Outline and Package Dimensions (8 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
ICS508M	ICS508M	Tubes	8 pin SOIC	0 to +70° C
ICS508MT	ICS508M	Tape and Reel	8 pin SOIC	0 to +70° C
ICS508MI	ICS508I	Tubes	8 pin SOIC	-40 to +85° C
ICS508MIT	ICS508I	Tape and Reel	8 pin SOIC	-40 to +85° C
ICS508-DWF	-	Die on uncut, probed wafers		0 to +70° C
ICS508-DPK	-	Tested die in waffle pack		0 to +70° C

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