ICS670-02
Low Phase Noise Zero Delay Buffer and Multiplier

Description

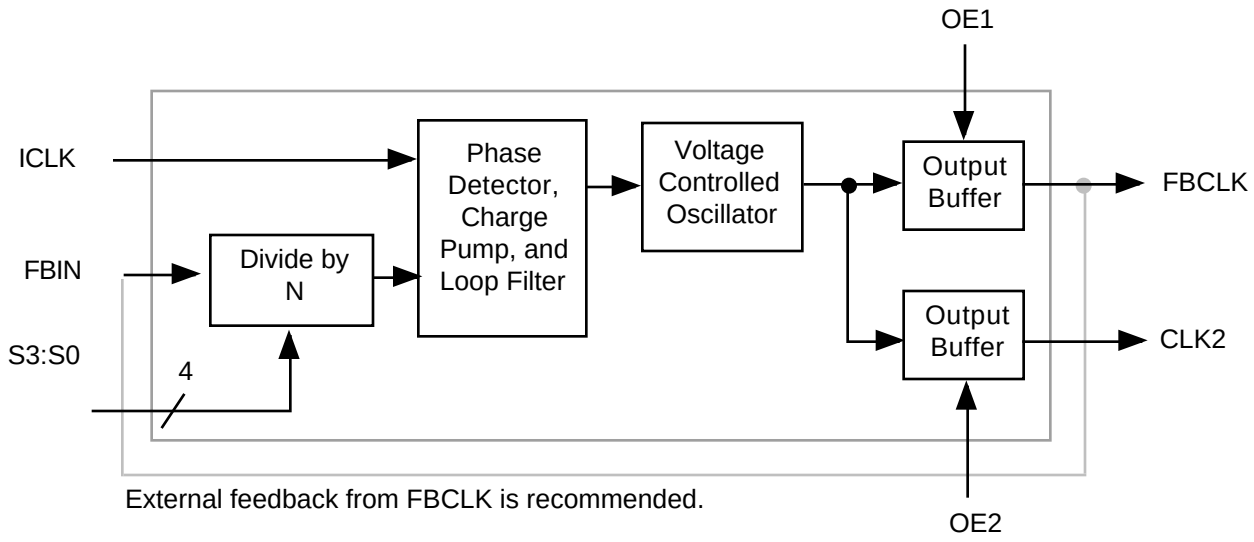
The ICS670-02 is a high speed, low phase noise Zero Delay Buffer (ZDB) which integrates ICS' proprietary analog/digital Phase Locked Loop (PLL) techniques. Part of ICS' ClockBlocks™ family, the zero delay feature means that the rising edge of the input clock aligns with the rising edges of the outputs, giving the appearance of no delay through the device. There are two identical outputs on the chip. The FBCLK should be used to connect to the FBIN. Each output has its own output enable pin.

The chip is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing off-chip feedback paths, the ICS670-02 can eliminate the delay through other devices. The 15 different on-chip multipliers work in a variety of applications. For other multipliers, including fractional multipliers, see the ICS527.

Features

- Packaged in 16 pin SOIC
- Clock inputs from 5 to 160 MHz (see page 2)
- Patented PLL with the lowest phase noise
- Output clocks up to 160 MHz at 3.3 V
- 15 selectable on-chip multipliers
- Power down mode available
- Low phase noise: -124 dBc/Hz at 10 kHz
- Output Enable function tri-states outputs
- Low jitter 15 ps one sigma
- Full swing CMOS outputs with 25 mA drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3 V or 5 V operation

Block Diagram



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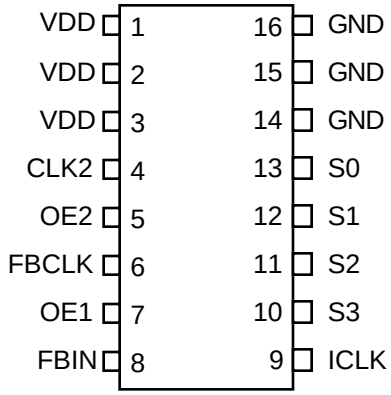
Pin Assignment



ICS670-02

Multiplier Select Table

S3	S2	S1	S0	CLK2 (and FBCLK)	Input Range (MHz)
0	0	0	0	Low (Power down entire chip)	-
0	0	0	1	Input x1.333	18 - 120
0	0	1	0	Input x6	5 - 26.67
0	0	1	1	Input x1.5	16.67 - 107
0	1	0	0	Input x3.333	7.5 - 48
0	1	0	1	Input x2.50	10 - 64
0	1	1	0	Input x4	6 - 40
0	1	1	1	Input x1	25 - 160
1	0	0	0	Input x2.333	11 - 69
1	0	0	1	Input x2.666	10 - 60
1	0	1	0	Input x12	5 - 13.33
1	0	1	1	Input x3	8 - 53.33
1	1	0	0	Input x10	5 - 16
1	1	0	1	Input x5	6 - 32
1	1	1	0	Input x8	5 - 20
1	1	1	1	Input x2	12 - 80

0=connect directly to ground
1=connect directly to VDD

Pin Descriptions

Number	Name	Type	Description
1	VDD	P	Connect to +3.3V or +5V. Must match other VDDs.
2	VDD	P	Connect to +3.3V or +5V. Must match other VDDs.
3	VDD	P	Connect to +3.3V or +5V. Must match other VDDs.
4	CLK2	O	Clock output from VCO. Output frequency equals the input frequency times multiplier.
5	OE2	I	Output clock enable 2. Tri-states the clock 2 output when low.
6	FBCLK	O	Clock ouput from VCO. Output frequency equals the input frequency times multiplier.
7	OE1	I	Output clock enable 1. Tri-states the feedback clock output when low.
8	FBIN	CI	Feedback clock input.
9	ICLK	CI	Clock input. Connect to a 5 - 160 MHz clock.
10	S3	I	Multiplier select pin 3. Determines outputs per table above. Internal pull-up.
11	S2	I	Multiplier select pin 2. Determines outputs per table above. Internal pull-up.
12	S1	I	Multiplier select pin 1. Determines outputs per table above. Internal pull-up.
13	S0	I	Multiplier select pin 0. Determines outputs per table above. Internal pull-up.
14	GND	P	Connect to ground.
15	GND	P	Connect to ground.
16	GND	P	Connect to ground.

Key: I = Input with internal pull-up resistor; O = output; P = power supply connection; CI = clock input.

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Operating Voltage, VDD		3.0		5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH, CMOS level	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Operating Supply Current, IDD	No Load		35		mA
Short Circuit Current	Each output		±50		mA
Internal Pull-up Resistor	OE, select pins		200		kΩ
Input Capacitance	OE, select pins		5		pF
AC CHARACTERISTICS (VDD = 3.3 V unless noted)					
Input Frequency (see table on page 2)	Depends on multiplier	5		160	MHz
Output Frequency	at 3.3V or 5V			160	MHz
Output Clock Rise Time	0.8 to 2.0V, no load			1.5	ns
Output Clock Fall Time	0.8 to 2.0V, no load			1.5	ns
Output Clock Duty Cycle	At VDD/2	45	50	55	%
Input to output skew, rising edges	Note 2		±100		ps
Maximum Absolute Jitter, short term			±45		ps
Maximum Jitter, one sigma			15		ps
Phase Noise, relative to carrier, 125 MHz (x5)	100 Hz offset		-110		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)	1 kHz offset		-122		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)	10 kHz offset		-121		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)	100 kHz offset		-117		dBc/Hz

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.

2. Rising edge of ICLK compared with rising edge of CLK2, with FBCLK connected to FBIN, and 15 pF load on CLK2.
See the graph on page 4 for skew versus frequency and loading.

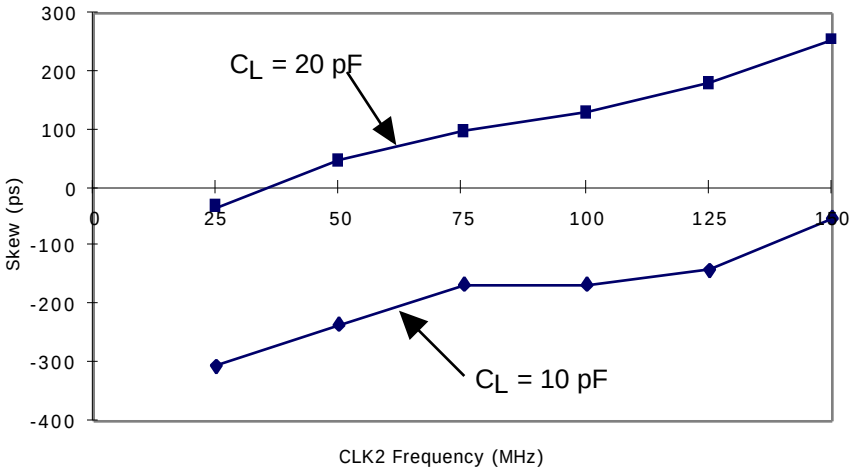


Figure 1. ICS670-02 skew from ICLK to CLK2, with change in load capacitance. VDD = 3.3 V.

Adjusting Input/Output Skew

The data in Figure 1 can be used to adjust individual circuit characteristics and achieve the minimum possible skew between ICLK and CLK2. With a 125 MHz output, for example, having a total load capacitance of 15 pF will result in nearly zero skew between ICLK and CLK2. Note that the load capacitance includes board trace capacitance, input capacitance of the load being driven by the ICS670-02, and any additional capacitors connected to CLK2.

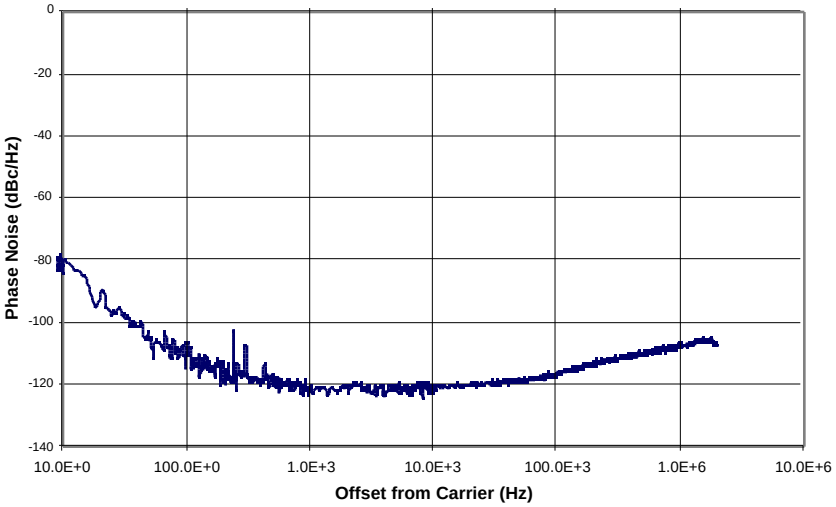
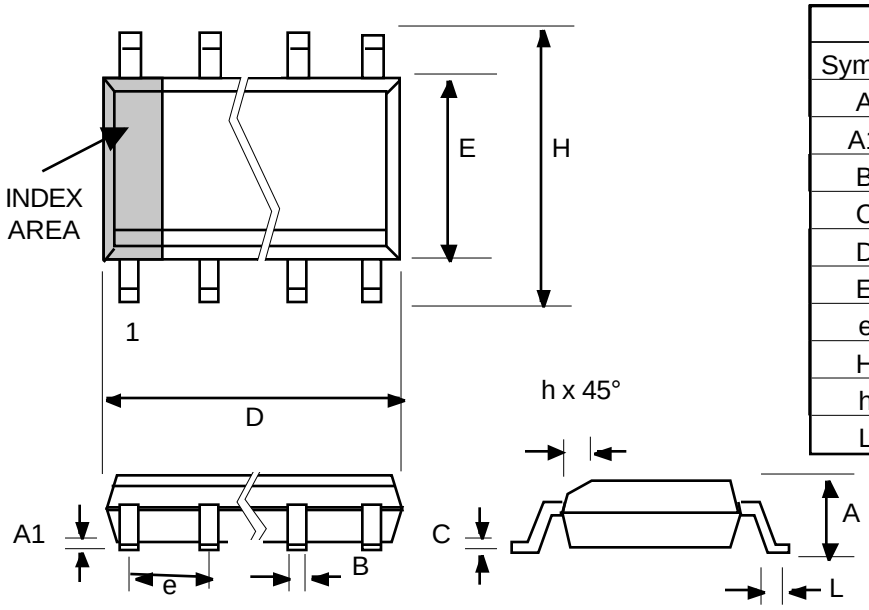


Figure 2. Phase Noise of ICS670-02 at 125 MHz out, 25 MHz clock input. VDD = 3.3 V.

External Components Selection

The ICS670-02 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD and GND, as close to the part as possible. A series termination resistor of 33 Ω may be used for each clock output.

Package Outline and Package Dimensions
(For current dimensional specifications, see JEDEC Publication No. 95.)



16 pin SOIC narrow

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	.050 BSC		1.27 BSC	
H	0.2284	0.2440	5.80	6.20
h	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
ICS670M-02	ICS670M-02	tubes	16 pin narrow SOIC	0 to 70 °C
ICS670M-02T	ICS670M-02	tape and reel	16 pin narrow SOIC	0 to 70 °C