



## GENERAL DESCRIPTION

The M2006-12 is a VCSO (Voltage Controlled SAW Oscillator) based clock generator PLL designed for clock frequency translation and jitter attenuation. The device supports both forward and inverse FEC (Forward Error Correction) clock multiplication ratios. Multiplication ratios are pin-selected from pre-programming look-up tables.



## FEATURES

- ◆ Similar to the [M2006-02](#) (and pin-compatible), but with an automatic protection switch (APS) function
- ◆ APS engages when a 4 ns or greater clock phase change is detected at the phase detector, such as might occur when reselecting reference clocks
- ◆ APS helps to ensure MTIE compliance by lowering loop bandwidth during the phase realignment
- ◆ APS is not recommended for complex FEC ratio translation when using an unstable reference; the M2006-02 is recommended for these applications
- ◆ In addition to the APS circuit, the APC (automatic phase compensation) pin enables absorption of the input phase change.
- ◆ Supports input reference and VCSO frequencies up to 700MHz, supports loop timing modes
- ◆ Single 3.3V power supply
- ◆ Small 9 x 9 mm SMT (surface mount) package

## SIMPLIFIED BLOCK DIAGRAM

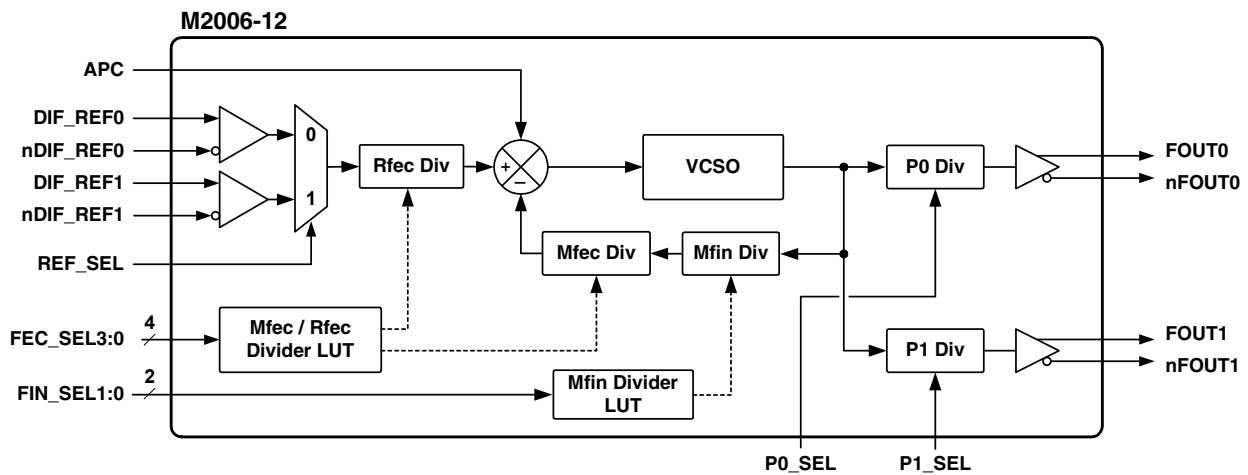


Figure 2: Simplified Block Diagram

## PIN ASSIGNMENT (9 x 9 mm SMT)

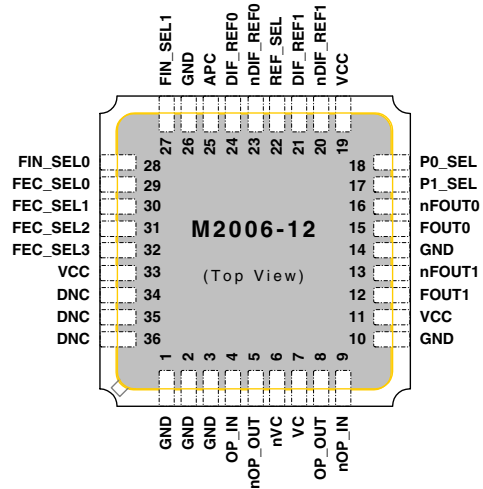


Figure 1: Pin Assignment

### Example I/O Clock Frequency Combinations Using M2006-12-622.0800 and Inverse FEC Ratios

| FEC PLL Ratio<br>Mfec / Rfec | Base Input Rate <sup>1</sup><br>(MHz) | Output Clock<br>(either output)<br>MHz |
|------------------------------|---------------------------------------|--|
| 1/1                          | 622.0800                              |  |
| 239/255                      | 663.7255                              | 622.08                                 |
| 238/255                      | 666.5143                              | or                                     |
| 237/255                      | 669.3266                              | 155.52                                 |
| 236/255                      | 672.1627                              |  |

Table 1: Example I/O Clock Frequency Combinations

Note 1: Input reference clock can be the base frequency shown divided by "Mfin" (as shown in Table 3 on [pg. 3](#)).



## DETAILED BLOCK DIAGRAM

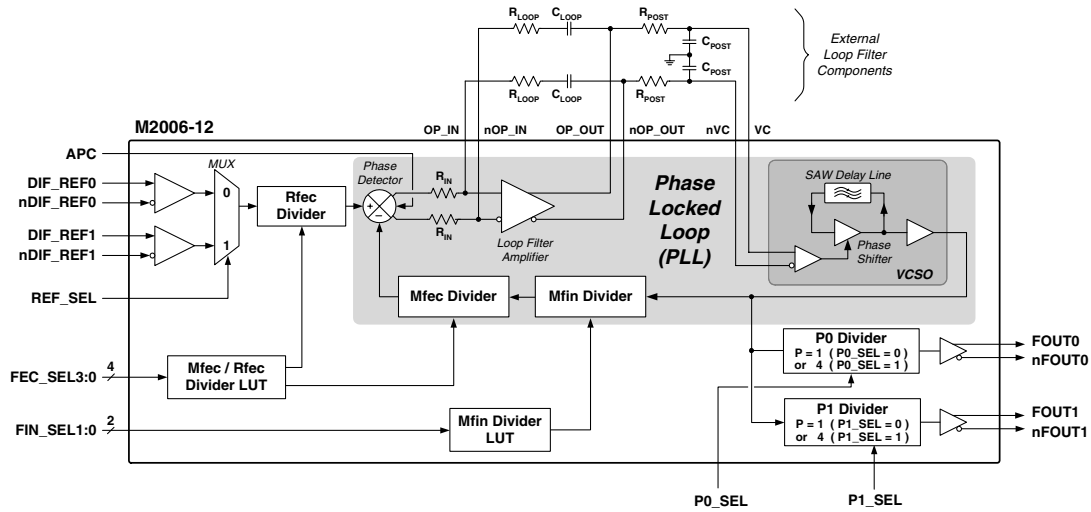


Figure 3: Detailed Block Diagram

## PIN DESCRIPTIONS

| Number              | Name          | I/O    | Configuration                            | Description  |
|---------------------|---------------|--------|--|--|
| 1, 2, 3, 10, 14, 26 | GND           | Ground |  | Power supply ground connections.   |
| 4                   | OP_IN         | Input  |  | External loop filter connections. See Figure 4.  |
| 9                   | nOP_IN        | Input  |  |  |
| 5                   | nOP_OUT       | Output |  |  |
| 8                   | OP_OUT        | Output |  |  |
| 6                   | nVC           | Input  |  | Power supply connection, connect to +3.3V.   |
| 7                   | VC            | Input  |  |  |
| 11, 19, 33          | VCC           | Power  |  | Clock output pairs. Differential LVPECL.   |
| 12, 13              | FOUT1, nFOUT1 | Output | No internal terminator                   |  |
| 15, 16              | FOUT0, nFOUT0 | Output | No internal terminator                   | P Divider controls. LVCMOS/LVTTL.<br>(For P0_SEL, P1_SEL, see Table 5 on pg. 3.  |
| 17                  | P1_SEL        | Input  | Internal pull-down resistor <sup>1</sup> |  |
| 18                  | P0_SEL        | Input  | Internal pull-down resistor <sup>1</sup> | Reference clock input pair 1. Differential LVPECL or LVDS.   |
| 20                  | nDIF_REF1     | Input  | Internal pull-down resistor <sup>1</sup> |  |
| 21                  | DIF_REF1      | Input  | Internal pull-down resistor <sup>1</sup> | Reference clock input selection. LVCMOS/LVTTL:<br>Logic 1 selects DIF_REF1, nDIF_REF1.<br>Logic 0 selects DIF_REF0, nDIF_REF0.                 |
| 22                  | REF_SEL       | Input  | Internal pull-down resistor <sup>1</sup> |  |
| 23                  | nDIF_REF0     | Input  | Internal pull-down resistor <sup>1</sup> | Reference clock input pair 0. Differential LVPECL or LVDS.   |
| 24                  | DIF_REF0      | Input  | Internal pull-down resistor <sup>1</sup> |  |
| 25                  | APC           | Input  | Internal pull-down resistor <sup>1</sup> | Automatic Phase Compensation. LVCMOS/LVTTL:<br>Logic 1 - Device absorbs input phase transients.<br>Logic 0 - Device doesn't absorb transients. |
| 27                  | FIN_SEL1      | Input  | Internal pull-down resistor <sup>1</sup> | Input clock frequency selection. LVCMOS/LVTTL.<br>(For FIN_SEL1:0, see Table 3 on pg. 3.   |
| 28                  | FIN_SEL0      | Input  | Internal pull-down resistor <sup>1</sup> |  |
| 29                  | FEC_SEL0      | Input  | Internal pull-up resistor <sup>1</sup>   | FEC PLL divider ratio selection. LVCMOS/LVTTL.<br>(For FEC_SEL3:0, see Table 4 on pg. 3.)  |
| 30                  | FEC_SEL1      |        |  |  |
| 31                  | FEC_SEL2      |        |  |  |
| 32                  | FEC_SEL3      |        |  |  |
| 34, 35, 36          | DNC           |        |  | Do Not Connect.  |

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see DC Characteristics (Pull-down and Pull-up) on pg. 7.



## PLL DIVIDER LOOK-UP TABLES

### Mfin (Frequency Input) Divider Look-Up Table (LUT)

The FIN\_SEL1:0 pins select the feedback divider value ("Mfin").

| M2006-12-622.0800 |            |                                      |
|-------------------|------------|--------------------------------------|
| FIN_SEL1:0        | Mfin Value | Sample Ref. Freq. (MHz) <sup>1</sup> |
| 1 1               | 1          | 622.08 <sup>2</sup>                  |
| 1 0               | 4          | 155.52                               |
| 0 1               | 8          | 77.76                                |
| 0 0               | 32         | 19.44                                |

Table 3: Mfin (Frequency Input) Divider Look-Up Table (LUT)

Note 1: Example with M2006-12-622.0800 and "Non-FEC ratio" selection made from Table 4 (FEC\_SEL2=1).

Note 2: Do not use with FEC\_SEL3:0=1100 or 1101.

### FEC PLL Ratio Dividers Look-up Table (LUT)

The FEC\_SEL3:0 pins select the FEC feedback and reference divider values Mfec and Rfec.

| FEC_SEL3:0 | Mfec | Rfec | Description   |
|------------|------|------|---|
| 0 0 0 0    | 236  | 255  | Inverse FEC ratio   |
| 0 0 0 1    | 79   | 85   | Inverse FEC ratio, equivalent to 237/255  |
| 0 0 1 0    | 14   | 15   | Inverse FEC ratio, equivalent to 238/255  |
| 0 0 1 1    | 239  | 255  | Inverse FEC ratio   |
| 0 1 0 0    | 236  | 236  | Non-FEC ratio, complement to 000 <sup>1</sup>   |
| 0 1 0 1    | 79   | 79   | Non-FEC ratio, complement to 001 <sup>1</sup>   |
| 0 1 1 0    | 14   | 14   | Non-FEC ratio, complement to 010 <sup>1</sup>   |
| 0 1 1 1    | 239  | 239  | Non-FEC ratio, complement to 011 <sup>1</sup>   |
| 1 0 0 0    | 255  | 236  | FEC ratio   |
| 1 0 0 1    | 85   | 79   | FEC ratio, equivalent to 255/237  |
| 1 0 1 0    | 15   | 14   | FEC ratio, equivalent to 255/238  |
| 1 0 1 1    | 255  | 239  | FEC ratio   |
| 1 1 0 0    | 1    | 1    | Non-FEC ratio. Do not use when FIN_SEL1:0=11. The maximum phase detector frequency is 175MHz <sup>2</sup> |
| 1 1 0 1    | 2    | 2    |   |
| 1 1 1 0    | 4    | 4    |   |
| 1 1 1 1    | 8    | 8    | Non-FEC ratio <sup>2</sup>  |

Table 4: FEC PLL Ratio Dividers Look-up Table (LUT)

Note 1: The complementary "Inverse FEC ratio" and "Non-FEC ratio" selections use the same Mfec Divider ratio. This results in the same PLL loop bandwidth and damping factor for both selections, enabling them to be actively switched in a given application. See "Maintaining PLL Lock:" on pg. 4.

Note 2: The various "Non-FEC ratio" settings can be used to actively change PLL loop bandwidth in a given application.

### Post-PLL Dividers

The M2006-12 also features two post-PLL dividers, one for each output pair. The "P1" divider is for FOUT1 and nFOUT1; the "P0" divider is for FOUT0 and nFOUT0.

Each divides the VCSO frequency to produce one of two output frequencies (1/4 or 1/1 of the VCSO frequency). The P1\_SEL and P0\_SEL pins each select the value for their corresponding divider.

| P1_SEL, P0_SEL | P Value | M2006-12-622.0800<br>Output Frequency (MHz) |
|----------------|---------|---|
| 1              | 4       | 155.52                                      |
| 0              | 1       | 622.08                                      |

Table 5: P Divider Selector, Values, and Frequencies

## FUNCTIONAL DESCRIPTION

The M2006-12 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks.

An internal high "Q" SAW filter provides low jitter signal performance and controls the output frequency of the VCSO (Voltage Controlled SAW Oscillator).

Configurable FEC feedback and reference dividers (the "Mfec Divider" and "Rfec Divider") provide the multiplication ratios necessary to accommodate clock translation for both forward and inverse Forward Error Correction.

In addition, a configurable feedback divider (labeled "Mfin Divider") provides the broader division options needed to accommodate various reference clock frequencies.

For example, the M2006-12-622.0800 (see "Ordering Information" on pg. 8) has a 622.08MHz VCSO frequency:

- The inverse FEC PLL ratios (at top of Table 4) enable the M2006-12-622.0800 to accept "base" input reference frequencies of: 663.7255, 666.5143, 669.3266, 672.1627, and 622.08MHz.
- The Mfin feedback divider enables the actual input reference clock to be the "base" input frequency divided by 1, 4, 8, or 32. Therefore, for the base input frequency of 622.08MHz, the actual input reference clock frequencies can be: 622.08, 155.52, 77.76, and 19.44MHz. (See Table 3 on pg. 3.)



### The PLL

The PLL uses a phase detector and configurable dividers to synchronize the output of the VCSO with selected reference clock.

The “Mfin Divider” and “Mfec Divider” divide the VCSO frequency, feeding the result into the phase detector.

The selected input reference clock is divided by the “Rfec Divider”. The result is fed into the other input of the phase detector.

The phase detector compares its two inputs. It then outputs pulses to the loop filter as needed to increase or decrease the VCSO frequency and thereby match and lock the divider output’s frequency and phase to those of the input reference clock.

Due to the narrow tuning range of the VCSO ( $\pm 200$ ppm), appropriate selection of all of the following are required for the PLL be able to lock: VCSO center frequency, input frequency, and divider selections.

*See also “Maintaining PLL Lock:” on pg. 4.*

### Relationship Among Frequencies and Dividers

The VCSO center frequency must be specified at time of order. The relationship between the VCSO (Fvcso) frequency, the Mfin divider, the Mfec divider, the Rfec divider, and the input reference frequency (Fin) is:

$$F_{vcso} = F_{in} \times M_{fin} \times \frac{M_{fec}}{R_{fec}}$$

As an example, for the M2006-12-622.0800, the first five PLL ratios in Table 4 enable use with these corresponding input reference frequencies:

| M2006-12-622.0800<br>VCSO Clock<br>Frequency (MHz) ÷ | FEC Ratio | M2006-12-622.0800<br>Base Input Ref.<br>= Frequency (MHz) <sup>1</sup> |
|--|-----------|--|
| 622.08   | 1 / 1     | 622.0800   |
|  | 239 / 255 | 663.7255   |
|  | 238 / 255 | 666.5143   |
|  | 237 / 255 | 669.3266   |
|  | 236 / 255 | 672.1627   |

**Table 6: Example FEC PLL Ratios and Input Reference Frequencies**  
Note 1: Input reference clock (“Fin”) can be the base frequency shown divided by “Mfin” (as shown in Table 3 on pg. 3).

### Maintaining PLL Lock:

The narrow tuning range of the VCSO requires that the input reference frequency must remain suitable for the current look-up table selection. For example, when switching between “Inverse FEC ratio” and “Non-FEC ratio” look-up table selections (see Table 4 on pg. 3), the input reference frequency must change accordingly in order for the PLL to lock.

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*An out-of-lock condition due to an inappropriate configuration will typically result in the VCSO operating at its lower or upper frequency rail, which is approximately 200ppm above or below the nominal VCSO center frequency.*

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See also “Automatic Protection Switch (APS)” (next) for an additional issue with regard to phase locking.

### Automatic Protection Switch (APS)

The M2006-12 includes a proprietary automatic protection switch (APS) circuit that prevents excessive phase transients of the output clocks upon input reference rearrangement. Upon the occurrence of an input reference phase change, or phase transient, PLL bandwidth is lowered by the APS circuit. This limits the rate of phase change in the output clocks. With proper configuration of the external loop filter, the output clocks will comply with MTIE (maximum time interval error) specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The APS circuit uses a phase error detector at the phase detector to detect a clock phase change. During normal operation with a stable reference clock, the PLL will be frequency locked and phase locked, resulting in very little error at the phase detector (<1 ns). Upon the selection of a new input reference clock at a different clock phase, a phase error will occur at the phase detector. The APS circuit is triggered with a phase error greater than 4 ns, upon which a narrow PLL bandwidth is applied. When the PLL locks to within 2 ns error at the phase detector, wide bandwidth (normal) operation is resumed.

The APS circuit is not suitable for situations in which an unstable reference is used. Under normal conditions the reference clock jitter should not induce phase jitter at the phase detector beyond 2 ns. (This includes when subjecting the system to jitter tolerance compliance testing.) Because of this, the M2006-12 is not recommended for use with some Stratum DPLL clock sources, or with unstable recovered network clocks intended for loop timing configuration. It is also not recommended for complex FEC ratios where the phase detector is operated at less 1 MHz. For these applications the M2006-02 is suggested. The M2006-02 is identical to the M2006-12 except that it does not include the APS function or the APC function discussed in the following section.



### Automatic Phase Compensation (APC) Pin

The M2006-12 also includes an automatic phase compensation (APC) circuit that can be selectively enabled by asserting the APC input (pin 25) to logic 1. The APC circuit works in conjunction with the APS circuit. When asserted, the APC circuit enables the PLL to absorb most of the phase change of the input clock which reduces re-lock time and the generation of wander. (Wander is created in this case by the generation of extra output clock cycles.)

When asserted, the APC circuit is triggered by same >4 ns phase transient (at the phase detector) that triggers the APS circuit. Once triggered, a new VCSO clock edge is selected for the phase comparator feedback input. (The clock edge selected is the one closest in phase to the new input clock phase.) The residual phase detector phase error following reselection is approximately 3-to-4 ns. The narrow bandwidth selected by the APS circuit minimizes VCSO drifting and switch transients during the process.

It is recommended that APC remain disabled (APC pin low) when the phase detector frequency is less than 4 MHz. Otherwise, the M2006-12 may have difficulty locking to reference upon power-up.

### Outputs

The M2006-12 provides a total of two differential LVPECL output pairs: FOUT1 and FOUT0. Because each output pair has its own P divider, the FOUT1 pair and the FOUT\_0 can output the two different frequencies at the same time. For example, FOUT1 can output 155.52MHz while FOUT0 outputs 622.08MHz.

### External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2006-12 requires the use of an external loop filter. This is provided via the provided filter pins (see Figure 4).

Due to the differential signal path design, the implementation requires two identical complementary RC filters as shown here.

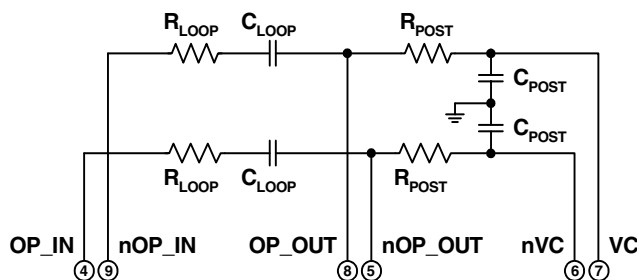


Figure 4: External Loop Filter

PLL bandwidth is affected by the “Mfec” value and the “Mfin” value, as well as the VCSO frequency.

The various “Non-FEC ratio” settings can be used to actively change PLL loop bandwidth in a given application. See “FEC PLL Ratio Dividers Look-up Table (LUT)” on pg. 3.

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*Consult factory for external loop filter component values.*

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## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

| Symbol   | Parameter            | Rating                 | Unit |
|----------|----------------------|------------------------|------|
| $V_I$    | Inputs               | -0.5 to $V_{CC} + 0.5$ | V    |
| $V_O$    | Outputs              | -0.5 to $V_{CC} + 0.5$ |      |
| $V_{CC}$ | Power Supply Voltage | 4.6                    |      |
| $T_S$    | Storage Temperature  | -45 to +100            | °C   |

Table 7: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in [Recommended Conditions of Operation](#), [DC Characteristics](#), or [AC Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## RECOMMENDED CONDITIONS OF OPERATION

| Symbol   | Parameter                     | Min   | Typ | Max   | Unit |
|----------|-------------------------------|-------|-----|-------|------|
| $V_{CC}$ | Positive Supply Voltage       | 3.135 | 3.3 | 3.465 | V    |
| $T_A$    | Ambient Operating Temperature | 0     |     | +70   | °C   |

Table 8: Recommended Conditions of Operation



## ELECTRICAL SPECIFICATIONS

### DC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3 \text{ Volts} \pm 5\%$ ,  $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ , VCSO Frequency = 622-675MHz, Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

|                        | Symbol            | Parameter                   |  | Min            | Typ            | Max            | Unit          | Test Conditions |
|------------------------|-------------------|-----------------------------|--|----------------|----------------|----------------|---------------|-----------------|
| Power Supply           | $V_{CC}$          | Positive Supply             |  | 3.135          | 3.3            | 3.465          | V             |                 |
|                        | $I_{CC}$          | Power Supply Current        |  |                | 162            |                | mA            |                 |
| Differential Inputs    | $I_{IH}$          | Input High Current          | nDIF_REF0, nDIF_REF1                       |                |                | 5              | $\mu\text{A}$ |                 |
|                        |                   |                             | DIF_REF0, nDIF_REF0                        |                |                | 150            | $\mu\text{A}$ |                 |
|                        | $I_{IL}$          | Input Low Current           | nDIF_REF0, nDIF_REF1                       | -150           |                |                | $\mu\text{A}$ |                 |
|                        |                   |                             | DIF_REF0, nDIF_REF0                        | -5             |                |                | $\mu\text{A}$ |                 |
|                        | $V_{P-P}$         | Peak to Peak Input          | DIF_REF0, nDIF_REF0,                       | 0.15           |                |                | V             |                 |
| $V_{CMR}$              | Common Mode Input | DIF_REF1, nDIF_REF1         | 0.5  |                | $V_{CC} - .85$ | V              |               |                 |
| LVCMOS / LVTTTL Inputs | $V_{IH}$          | Input High Voltage          | REF_SEL,                                   | 2              |                | $V_{CC} + 0.3$ | V             |                 |
|                        | $V_{IL}$          | Input Low Voltage           | FIN_SEL1, FIN_SEL0,<br>FEC_SEL0, FEC_SEL1, | -0.3           |                | 0.8            | V             |                 |
|                        | $C_{in}$          | Input Capacitance           | FEC_SEL2, FEC_SEL3                         |                |                | 4              | pF            |                 |
| Pull-down              | $R_{pulldown}$    | Internal Pull-down Resistor | (All Inputs except FEC_SEL3:0)             |                | 51             |                | k $\Omega$    |                 |
|                        | $I_{IH}$          | Input High Current          |  |                |                | 150            | $\mu\text{A}$ |                 |
|                        | $I_{IL}$          | Input Low Current           |  | -5             |                |                | $\mu\text{A}$ |                 |
| Pull-up                | $R_{pullup}$      | Internal Pull-down Resistor | FEC_SEL0, FEC_SEL1,<br>FEC_SEL2, FEC_SEL3  |                | 51             |                | k $\Omega$    |                 |
|                        | $I_{IH}$          | Input High Current          |  |                |                | 5              | $\mu\text{A}$ |                 |
|                        | $I_{IL}$          | Input Low Current           |  | -150           |                |                | $\mu\text{A}$ |                 |
| Differential Outputs   | $V_{OH}$          | Output High Voltage         |  | $V_{CC} - 1.4$ |                | $V_{CC} - 1.0$ | V             |                 |
|                        | $V_{OL}$          | Output Low Voltage          | FOUT_0, nFOUT_0,<br>FOUT_1, nFOUT_1        | $V_{CC} - 2.0$ |                | $V_{CC} - 1.7$ | V             |                 |
|                        | $V_{P-P}$         | Peak to Peak Output         |  | 0.6            |                | 0.85           | V             |                 |

Table 9: DC Characteristics

### AC Characteristics

Unless stated otherwise,  $V_{CC} = 3.3 \text{ Volts} \pm 5\%$ ,  $T_A = 0^\circ\text{C to } 70^\circ\text{C}$ , VCSO Frequency = 622-675MHz, Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$

|                       | Symbol     | Parameter                                |   | Min       | Typ       | Max | Unit   | Test Conditions   |
|-----------------------|------------|--|---|-----------|-----------|-----|--------|---|
| Input Frequency Range | $F_{IN}$   | Input Frequency                          | DIF_REF0, nDIF_REF0,<br>DIF_REF1, nDIF_REF1 | 10        |           | 700 | MHz    |   |
|                       |            |  |   |           |           |     |        |   |
| Output Frequency      | $F_{FOUT}$ | Output Frequency Range                   | FOUT_0, nFOUT_0,<br>FOUT_1, nFOUT_1         | 100       |           | 700 | MHz    |   |
|                       | APR        | VCSO Pull-Range                          |   | $\pm 125$ | $\pm 200$ |     | ppm    |   |
|                       | $\Phi_n$   | Single Side Band Phase Noise @ 622.08MHz | 1kHz Offset                                 |           | -72       |     | dBc/Hz | $F_{in}=19.44\_MHz$<br>$M_{min}=32, M_{fec}=1, R_{fec}=1$ |
|                       |            |  | 10kHz Offset                                |           | -94       |     | dBc/Hz |   |
|                       |            |  | 100kHz Offset                               |           | -123      |     | dBc/Hz |   |
|                       | J(t)       | Jitter (rms) @ 622.08MHz                 | 12kHz to 20MHz                              |           | 0.5       |     | ps     |   |
|                       | $t_{PW}$   | Output Duty Cycle <sup>1</sup>           |   | 40        | 50        | 60  | %      | P0, P1 = 1 or 4   |
|                       | $t_R$      | Output Rise Time <sup>1</sup>            |   | 325       | 450       | 500 | ps     | 20% to 80%  |
|                       | $t_F$      | Output Fall Time <sup>1</sup>            |   | 325       | 450       | 500 | ps     | 20% to 80%  |

Table 10: AC Characteristics

Note 1: See [Parameter Measurement Information](#) on pg. 8.



## PARAMETER MEASUREMENT INFORMATION

### Output Rise and Fall Time

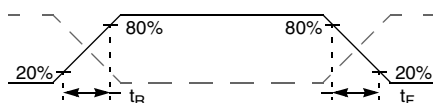


Figure 5: Output Rise and Fall Time

### Duty Cycle

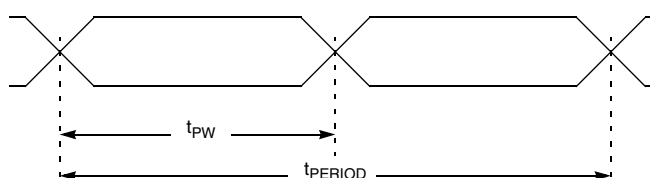


Figure 6: Duty Cycle

## DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

### Mechanical Dimensions:

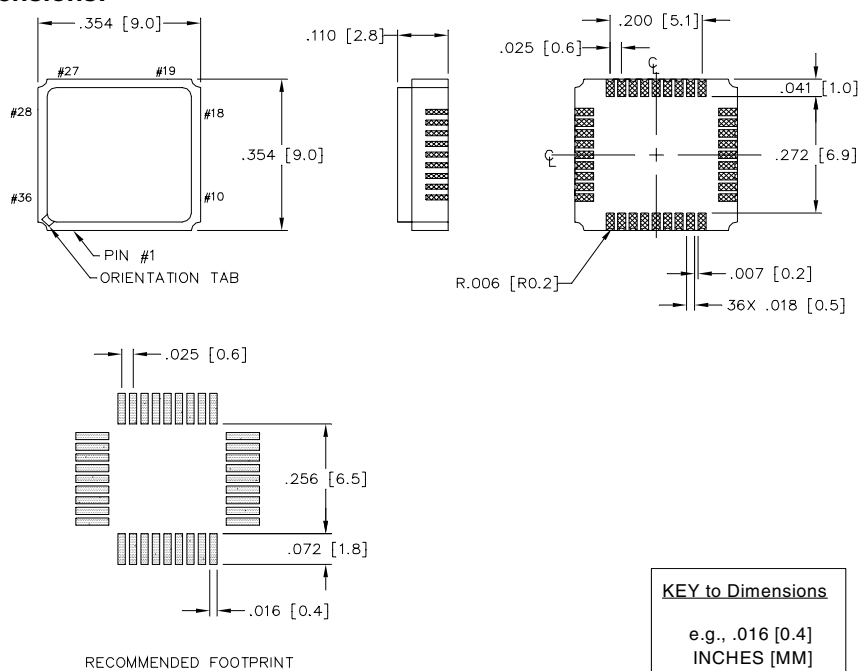


Figure 7: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

## ORDERING INFORMATION

| For VCSO Frequency (MHz) | Order Part Number |
|--------------------------|-------------------|
| 622.08                   | M2006-12-622.0800 |
| 625.00                   | M2006-12-625.0000 |
| 669.3266                 | M2006-12-669.3266 |
| 669.6429                 | M2006-12-669.6429 |

Table 11: Ordering Information

*Consult ICS for the availability of other VCSO frequencies.*

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