



Integrated
Circuit
Systems, Inc.

PRELIMINARY

ICS844008I-15

FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION



The ICS844008I-15 is an 8 output LVDS Synthesizer optimized to generate PCI Express reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz parallel resonant crystal, the following frequencies can be generated based on F_SEL pin: 100MHz or 125MHz. The ICS844008I-15 uses ICS' 3rd generation low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting PCI Express jitter requirements. The ICS844008I-15 is packaged in a 32-pin LQFP package.

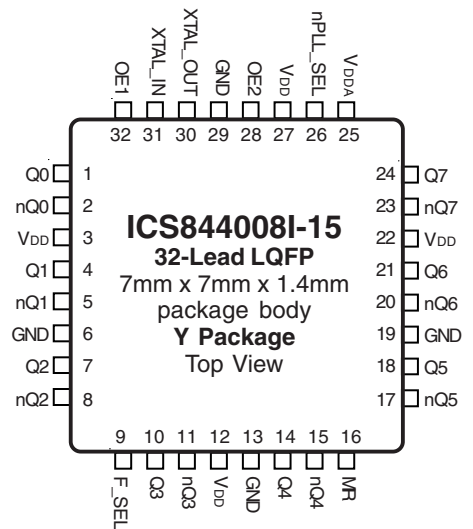
FEATURES

- Eight LVDS outputs
- Crystal oscillator interface
- Supports the following output frequencies: 100MHz or 125MHz
- VCO: 500MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.42ps (typical)
- Full 3.3V supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

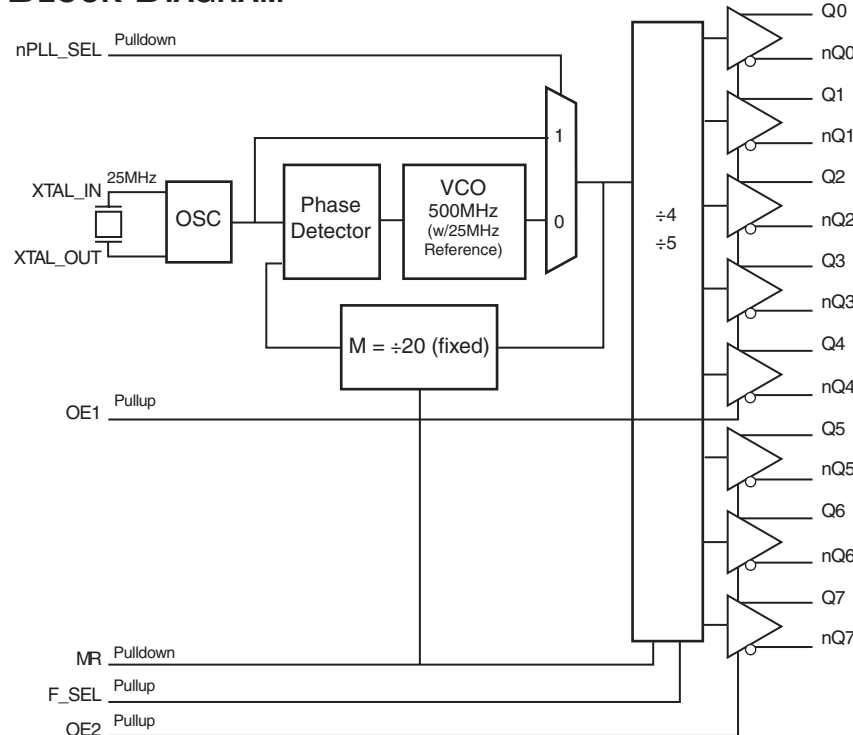
FREQUENCY SELECT FUNCTION TABLE

| Input | | | | | Output Frequency (MHz) |
|-----------------------|-------|-----------------|-----------------|-------------------|------------------------|
| Input Frequency (MHz) | F_SEL | M Divider Value | N Divider Value | M/N Divider Value | |
| 25MHz | 0 | 20 | 4 | 5 | 125 |
| 25MHz | 1 | 20 | 5 | 4 | 100 |

PIN ASSIGNMENT



BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.



TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|------------------|----------------------|--------|----------|---|
| 1, 2 | Q0, nQ0 | Output | | Differential output pair. LVDS interface levels. |
| 3, 12, 22, 27 | V _{DD} | Power | | Core supply pin. |
| 4, 5 | Q1, nQ1 | Output | | Differential output pair. LVDS interface levels. |
| 6, 13, 19, 29 | GND | Power | | Power supply ground. |
| 7, 8 | Q2, nQ2 | Output | | Differential output pair. LVDS interface levels. |
| 9 | F_SEL | Input | Pullup | Frequency select pin LVCMOS/LVTTL interface levels. |
| 10, 11 | Q3, nQ3 | Output | | Differential output pair. LVDS interface levels. |
| 14, 15 | Q4, nQ4 | Output | | Differential output pair. LVDS interface levels. |
| 16 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 17, 18 | nQ5, Q5 | Output | | Differential output pair. LVDS interface levels. |
| 20, 21 | nQ6, Q6 | Output | | Differential output pair. LVDS interface levels. |
| 23, 24 | nQ7, Q7 | Output | | Differential output pair. LVDS interface levels. |
| 25 | V _{DDA} | Power | | Analog supply pin. |
| 26 | nPLL_SEL | Input | Pulldown | Selects between the PLL and REF_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels. |
| 28 | OE2 | Input | Pullup | Output enable for Q5/nQ5:Q7/nQ7 outputs. LVCMOS/LVTTL interface levels. |
| 30, 31 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 32 | OE1 | Input | Pullup | Output enable for Q0/nQ0:Q4/nQ4 outputs. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{PULLUP} | Input PullUP Resistor | | | 51 | | kΩ |

TABLE 3A. OE1 FUNCTION TABLE

| Input | Outputs |
|------------|------------------------------|
| OE1 | Q0:Q4, nQ0:nQ4 |
| 0 | Places outputs in Hi-Z state |
| 1 | Normal operation |

TABLE 3B. OE2 FUNCTION TABLE

| Input | Outputs |
|------------|------------------------------|
| OE2 | Q5:Q7, nQ5:nQ7 |
| 0 | Places outputs in Hi-Z state |
| 1 | Normal operation |



ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_i | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_o | |
| Continuous Current | 10mA |
| Surge Current | 15mA |
| Package Thermal Impedance, θ_{JA} | 47.9°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | | | 122 | | mA |
| I_{DDA} | Analog Supply Current | | | 11 | | mA |

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{DD} = 3.3V$ | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 3.3V$ | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | MR, nPLL_SEL | $V_{DD} = V_{IN} = 3.465$ | | 150 | μA |
| | | OE1, OE2, F_SEL | $V_{DD} = V_{IN} = 3.465$ | | 5 | μA |
| I_{IL} | Input Low Current | MR, nPLL_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| | | OE1, OE2, F_SEL | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | | 350 | | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | 40 | | mV |
| V_{OS} | Offset Voltage | | | 1.25 | | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | 50 | | mV |



TABLE 5. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 22.4 | 25 | 27.2 | MHz |
| Parts per Million (ppm); NOTE 1 | | | | 100 | ppm |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 100 | μ W |

NOTE: Characterized using an 18pF parallel resonant crystal.

NOTE 1: When used with recommended 50ppm crystal and external trim caps adjusted for user PC board.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------|--------------------------------------|----------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | FSEL = 0 | | 125 | | MHz |
| | | FSEL = 1 | | 100 | | MHz |
| $t_{sk(o)}$ | Output Skew; NOTE 1, 2 | | | TBD | 50 | ps |
| $f_{jit(cc)}$ | Cycle-to-Cycle Jitter | | | 25 | 50 | ps |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 3 | 125MHz, (1.875MHz - 20MHz) | | 0.42 | 1 | ps |
| | | 100MHz, (1.875MHz - 20MHz) | | 0.46 | 1 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 200 | 330 | 650 | ps |
| odc | Output Duty Cycle | | 48 | 50 | 52 | % |

Minimum and Maximum values are design target specs.

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions.

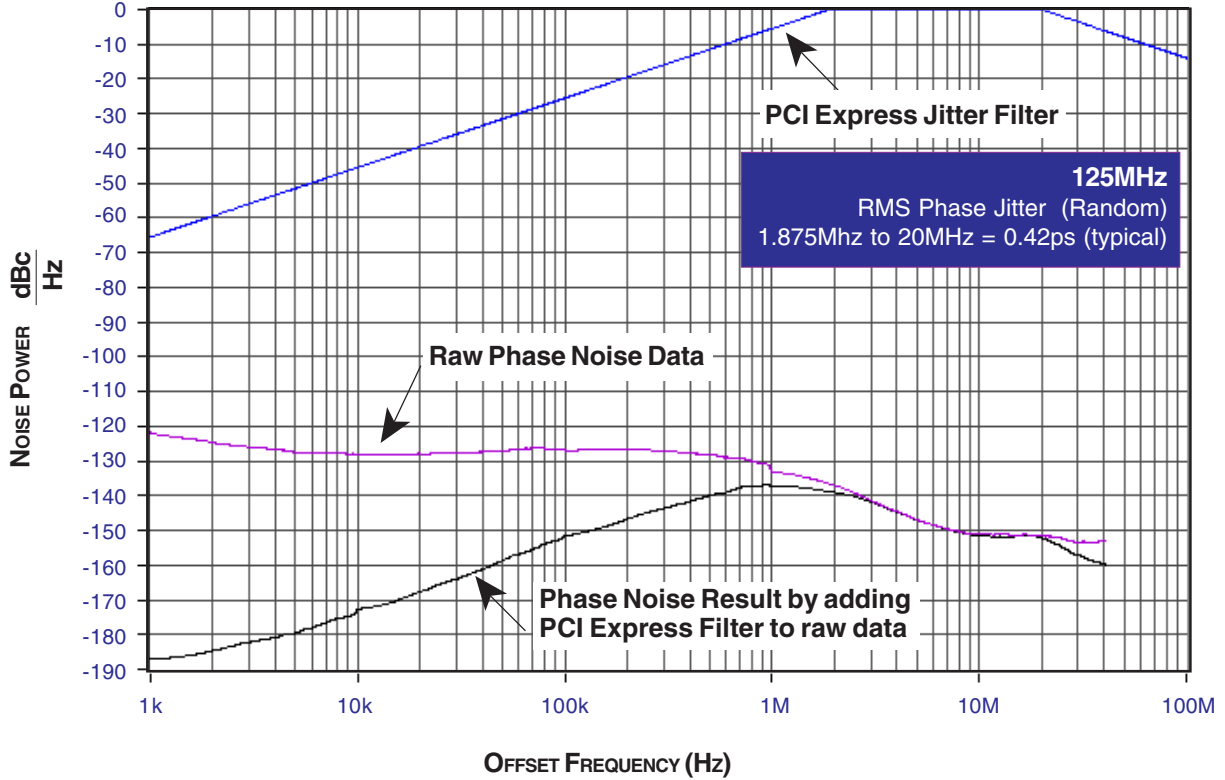
Measured at $V_{DD}/2$.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plot.

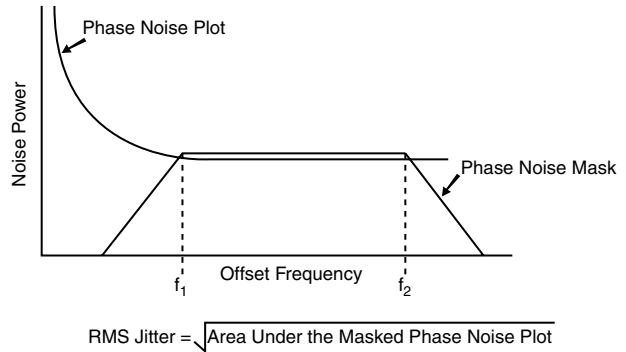
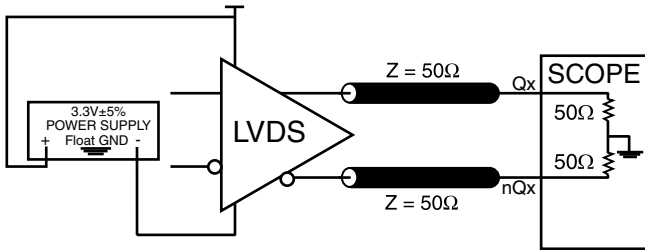


TYPICAL PHASE NOISE AT 125MHz AT 3.3V



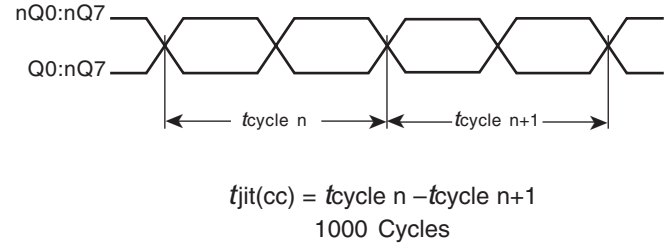
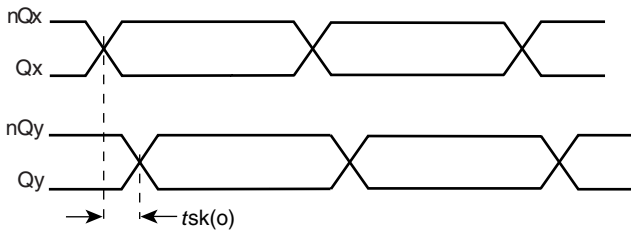


PARAMETER MEASUREMENT INFORMATION



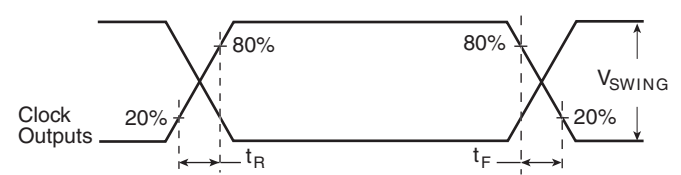
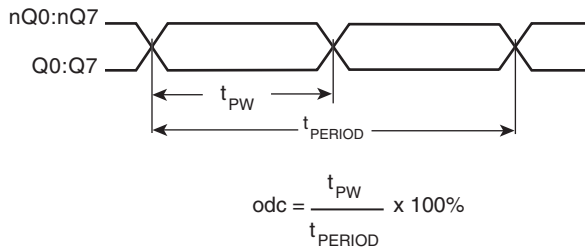
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

RMS PHASE JITTER



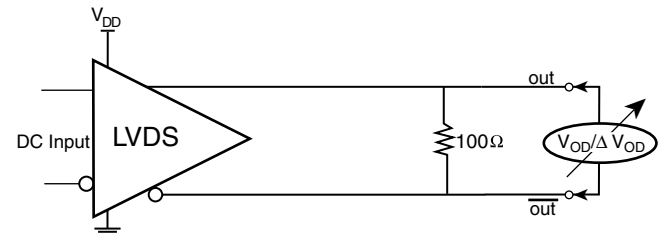
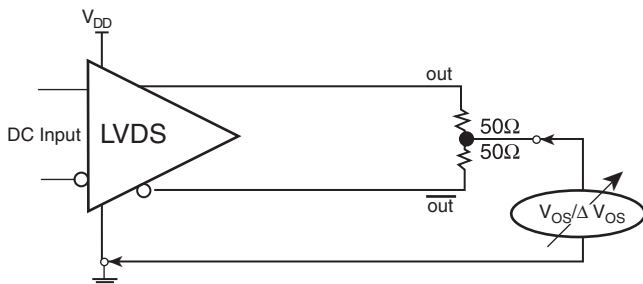
OUTPUT SKEW

CYCLE-TO-CYCLE JITTER



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP



APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844008I-15 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} .

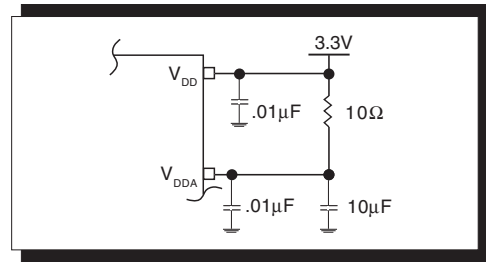


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844008I-15 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in

Figure 2 below were determined using a 25MHz parallel resonant crystal and were chosen to minimize the ppm error.

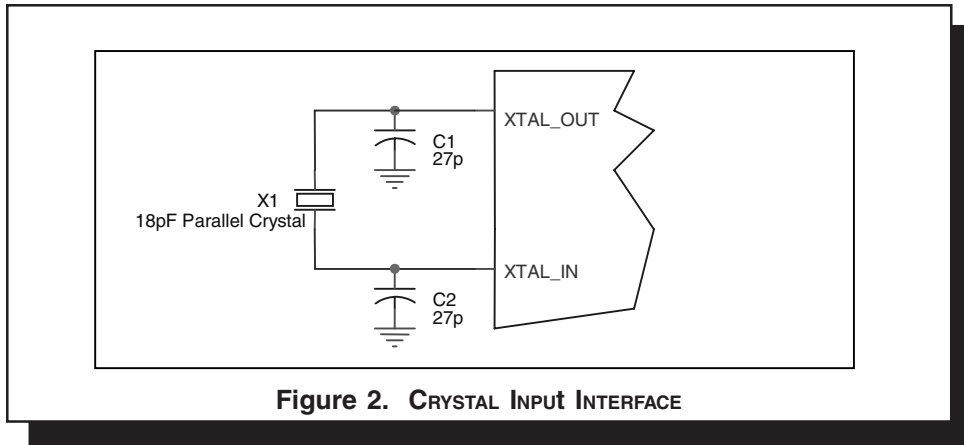


Figure 2. CRYSTAL INPUT INTERFACE



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVDS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

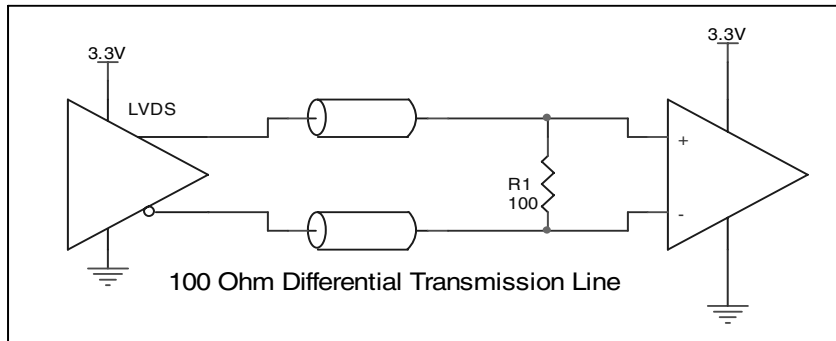


FIGURE 3. TYPICAL LVDS DRIVER TERMINATION



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844008I-15. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS844008I-15 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (122mA + 11mA) = 460.85mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.461W * 42.1^\circ C/W = 104.4^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD LQFP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



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RELIABILITY INFORMATION

TABLE 8. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD LQFP

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------|----------|----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 47.9°C/W | 42.1°C/W | 39.4°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS844008I-15 is: TBD



PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

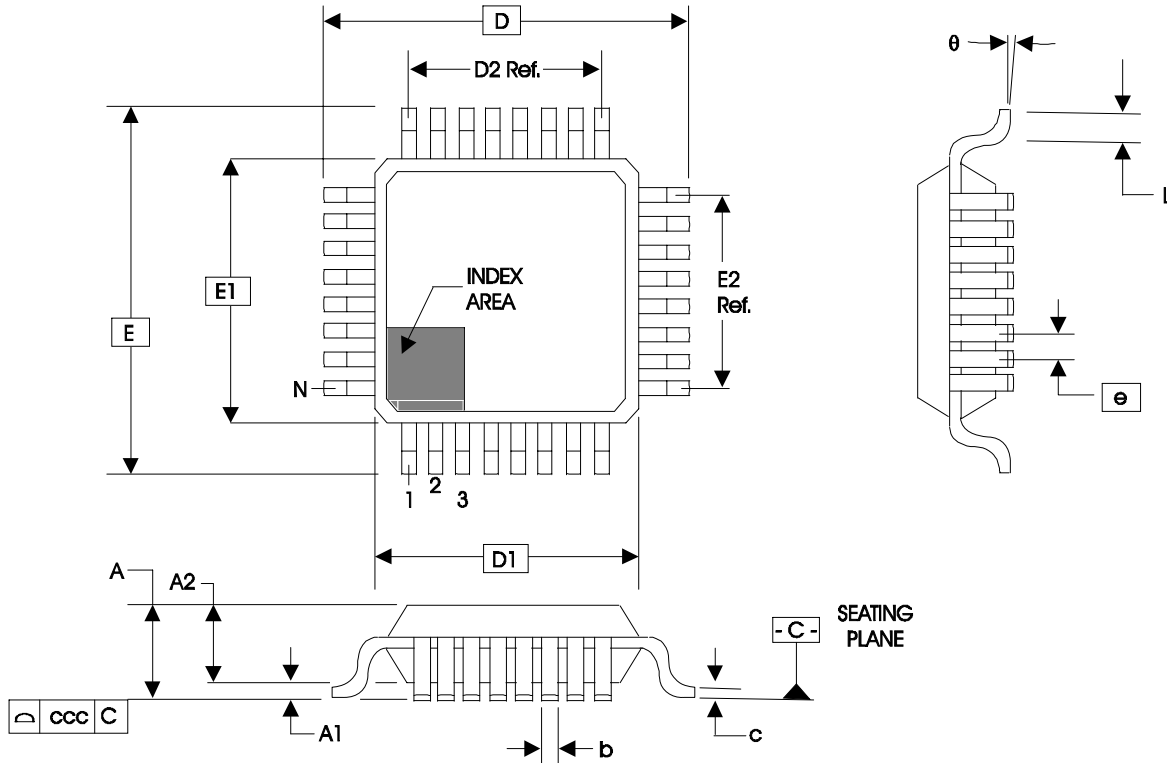


TABLE 9. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBA | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 32 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.60 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.60 Ref. | | |
| e | 0.80 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.10 |

Reference Document: JEDEC Publication 95, MS-026



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FEMTOCLOCKS™ CRYSTAL-TO-
LVDS FREQUENCY SYNTHESIZER

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|--------------------|--------------|--------------------------|--------------------|---------------|
| ICS844008AYI-15 | ICS44008AI15 | 32 Lead LQFP | tube | -40°C to 85°C |
| ICS844008AYI-15T | ICS44008AI15 | 32 Lead LQFP | 1000 tape & reel | -40°C to 85°C |
| ICS844008AYI-15LF | TBD | 32 Lead "Lead-Free" LQFP | tube | -40°C to 85°C |
| ICS844008AYI-15LFT | TBD | 32 Lead "Lead-Free" LQFP | 1000 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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